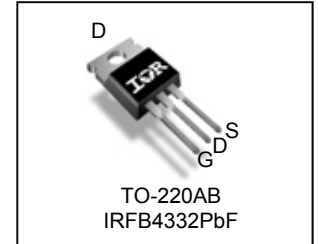
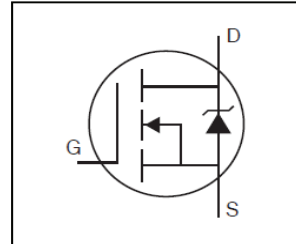


HEXFET® Power MOSFET

Feature

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low E_{PULSE} Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low Q_G for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 175°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

Key Parameters		
$V_{DS\ min}$	250	V
$V_{DS(Avalanche)\ typ.}$	300	V
$R_{DS(on)\ typ.\ @\ 10V}$	29	mΩ
$T_J\ max$	175	°C



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB4332PbF	TO-220	Tube	50	IRFB4332PbF

Description

This HEXFET® Power MOSFET is specifically designed for Sustain; Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low EPULSE rating. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications.

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 30	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	60	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	42	
I_{DM}	Pulsed Drain Current ①	230	
$I_{RP} @ T_C = 100^\circ C$	Repetitive Peak Current ⑤⑥	120	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	390	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	200	W
	Linear Derating Factor	2.6	W/°C
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf·in (1.1N·m)	

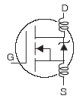
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	0.38	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Notes ① through ⑥ are on page 2.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	170	—	mV/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	29	33	mΩ	V _{GS} = 10V, I _D = 35A
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	—	-14	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 250V, V _{GS} = 0V
		—	—	1.0	mA	V _{DS} = 250V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Trans conductance	100	—	—	S	V _{DS} = 25V, I _D = 35A
Q _g	Total Gate Charge	—	99	150	nC	V _{DD} = 125V, I _D = 35A, V _{GS} = 10V ^③
Q _{gd}	Gate-to-Drain Charge	—	35	—		
t _{st}	Shoot Through Blocking Time	100	—	—	ns	V _{DD} = 200V, V _{GS} = 15V, R _G = 4.7Ω
E _{PULSE}	Energy per Pulse	—	520	—	μJ	L = 220nH, C = 0.3μF, V _{GS} = 15V V _{DS} = 200V, R _G = 5.1Ω, T _J = 25°C
		—	920	—		L = 220nH, C = 0.3μF, V _{GS} = 15V V _{DS} = 200V, R _G = 5.1Ω, T _J = 100°C
C _{iss}	Input Capacitance	—	5860	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	530	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz,
C _{oss eff.}	Effective Output Capacitance	—	360	—		V _{GS} = 0V, V _{DS} = 0V to 200V
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		


Avalanche Characteristics

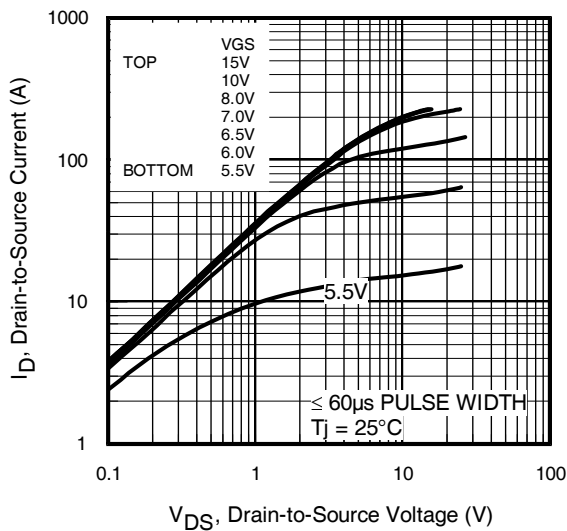
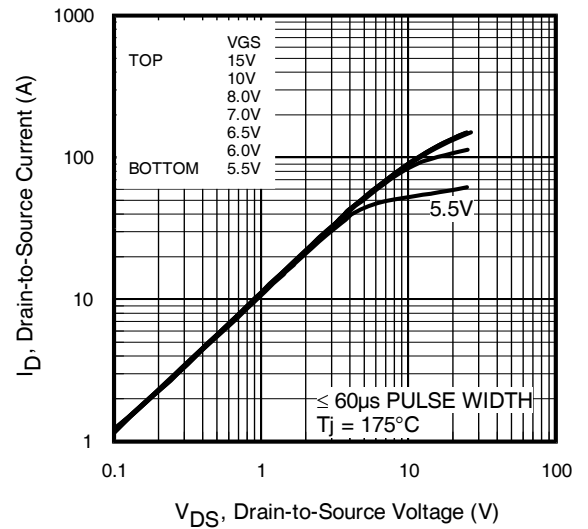
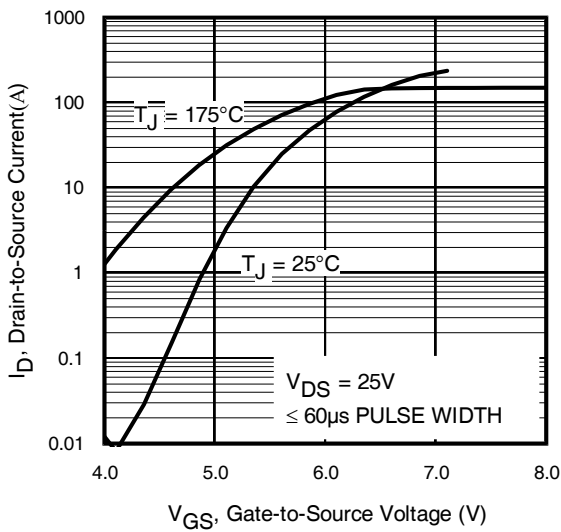
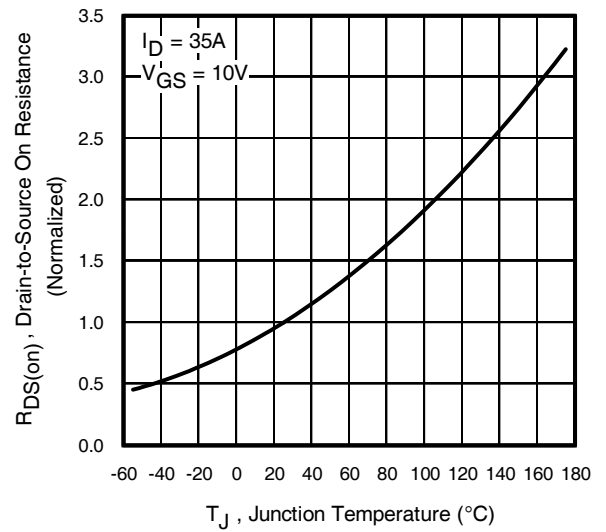
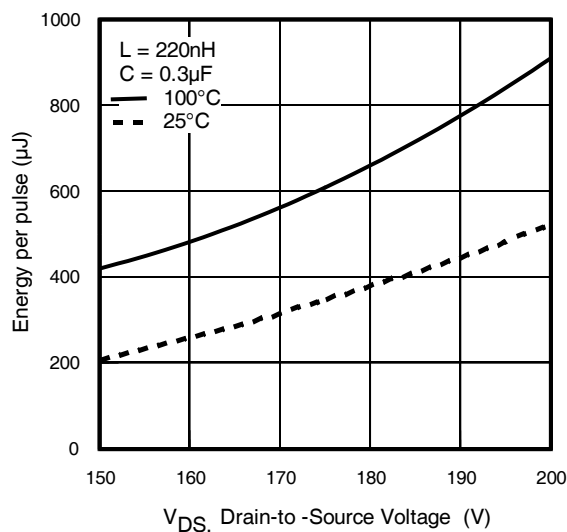
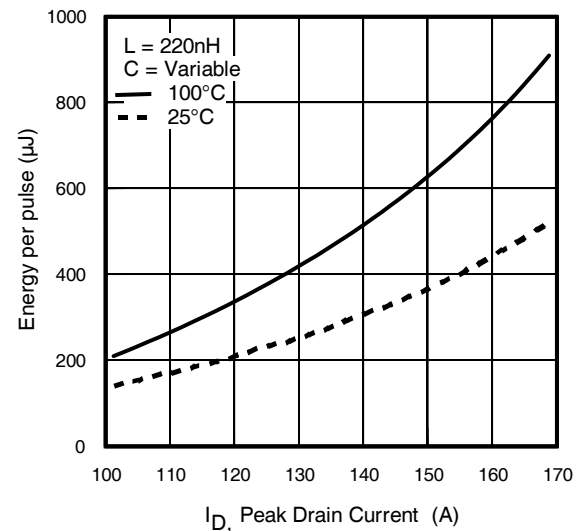
	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ^②	—	230	mJ
E _{AR}	Repetitive Avalanche Energy ^①	300	39	mJ
V _{DS (Avalanche)}	Repetitive Avalanche Voltage ^①	—	—	V
I _{AS}	Avalanche Current ^②	—	35	A

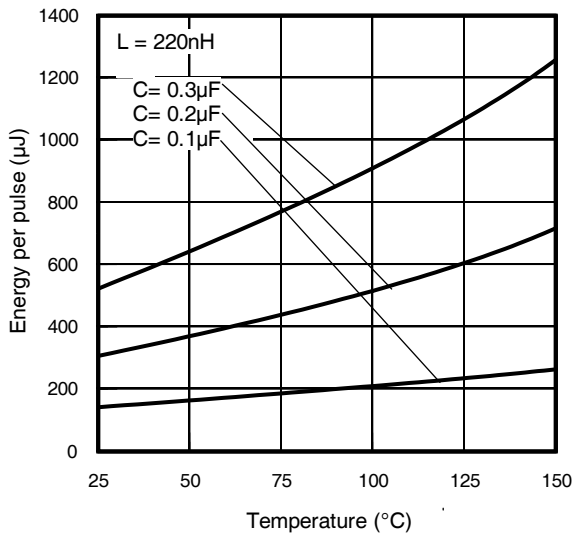
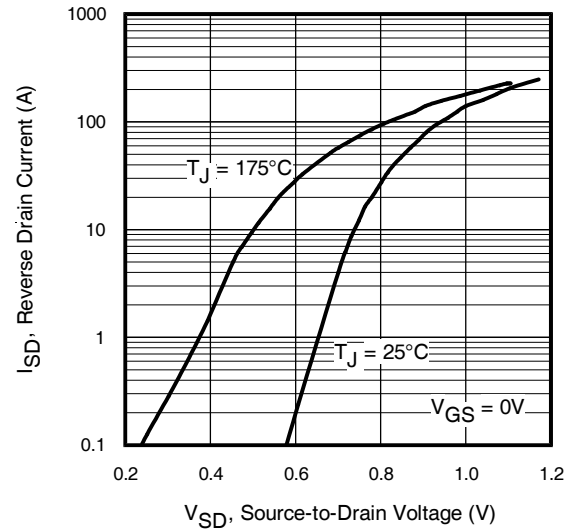
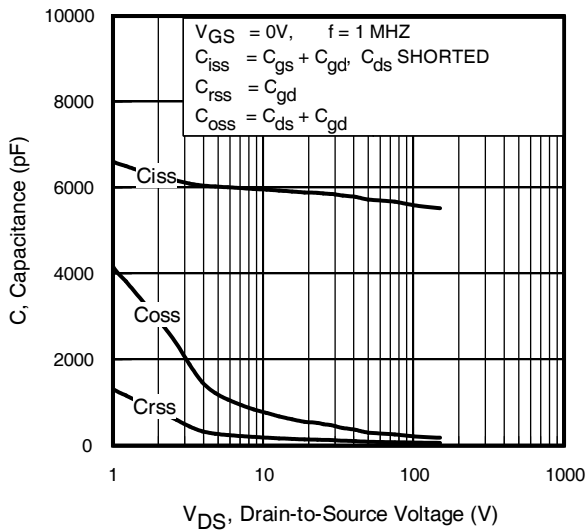
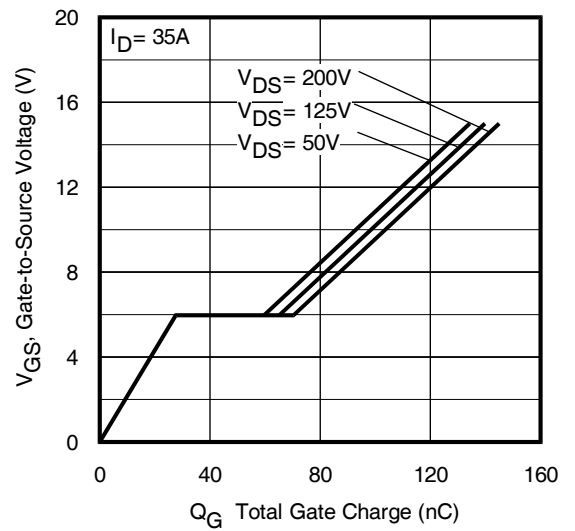
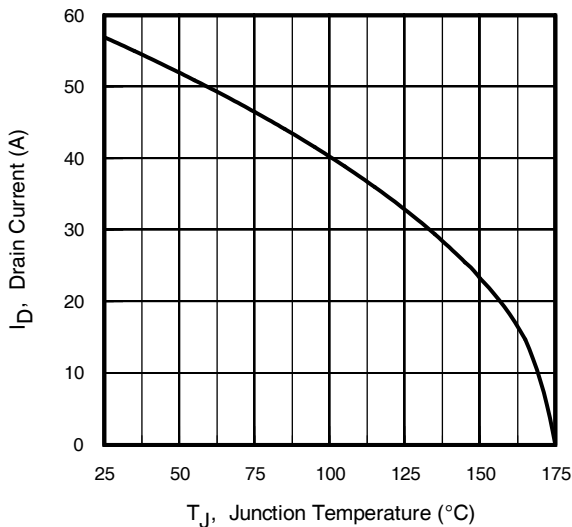
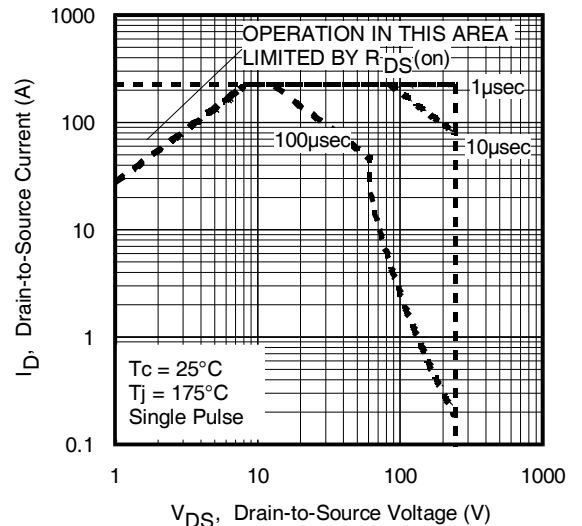
Diode Characteristics

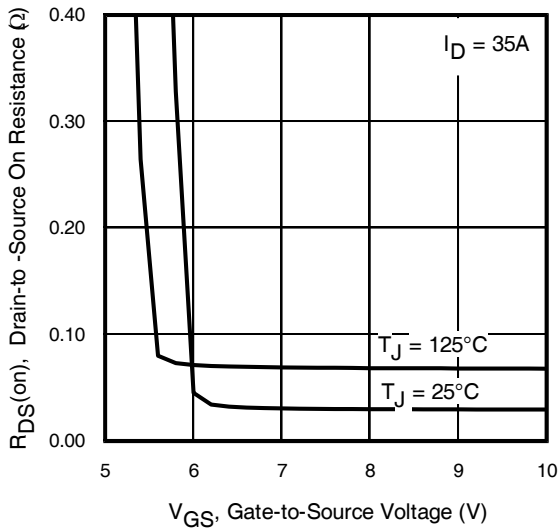
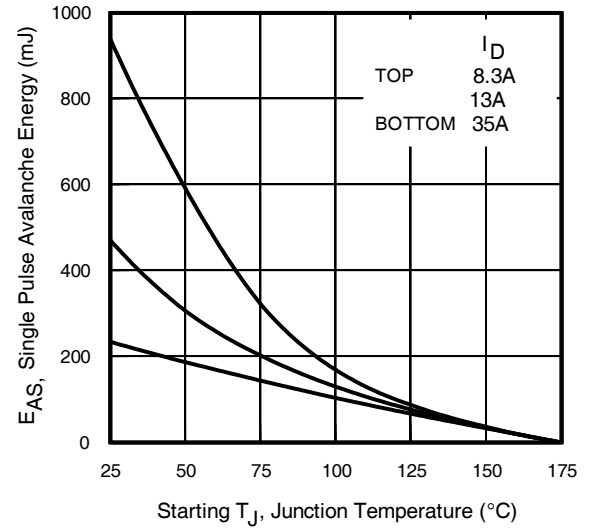
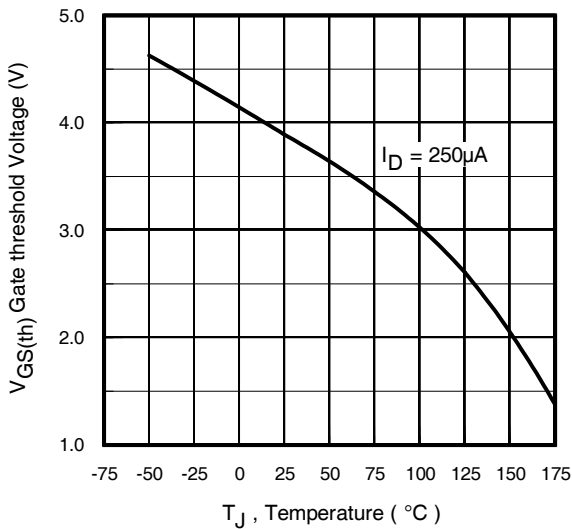
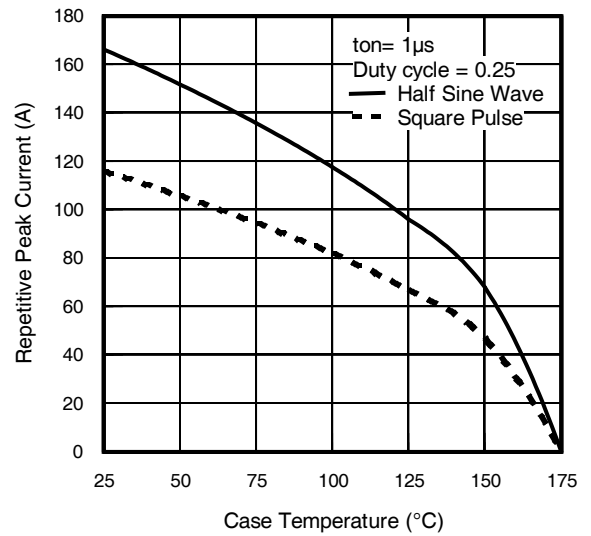
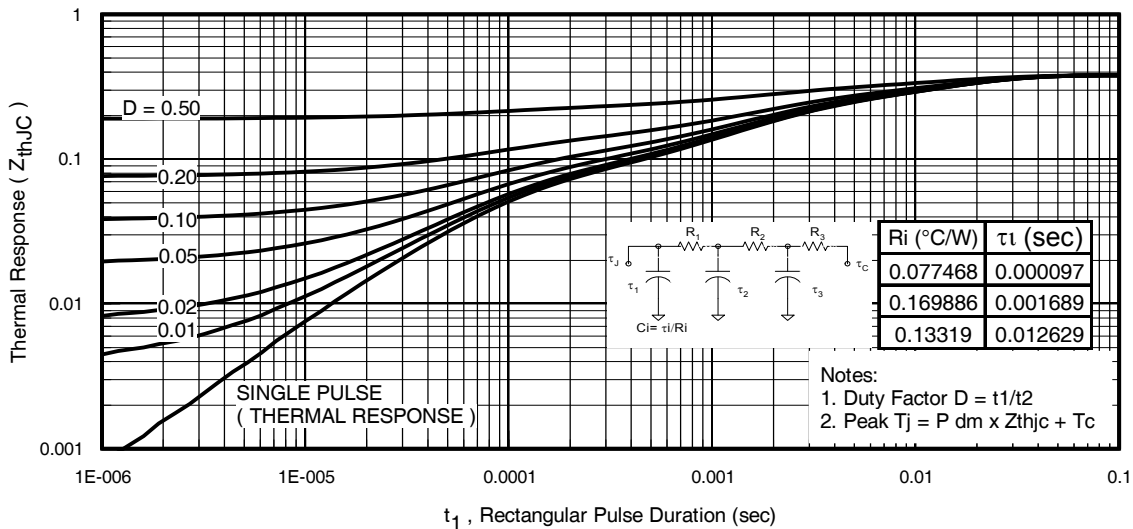
	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S @ T _C = 25°C	Continuous Source Current (Body Diode)	—	—	60	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	230		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 35A, V _{GS} = 0V ^③
t _{rr}	Reverse Recovery Time	—	190	290	ns	T _J = 25°C, I _F = 35A, V _{DD} = 50V
Q _{rr}	Reverse Recovery Charge	—	820	1230	nC	di/dt = 100A/μs ^③

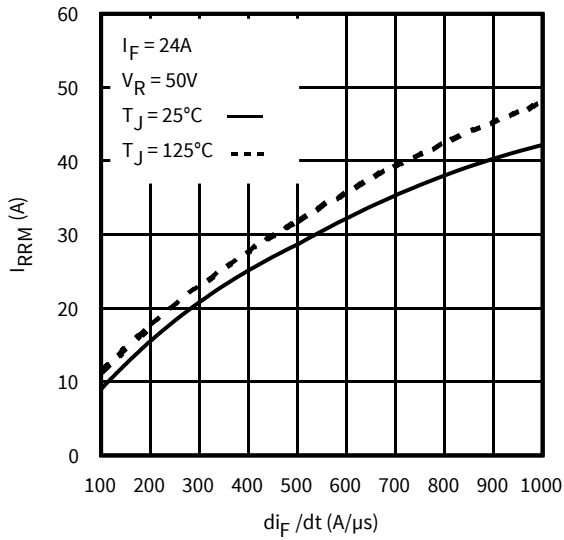
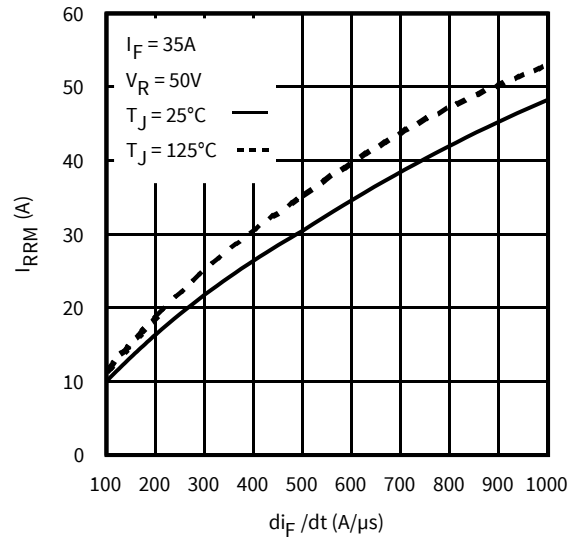
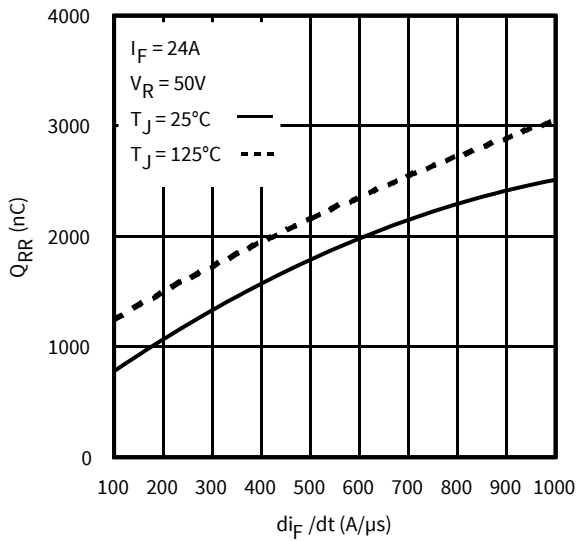
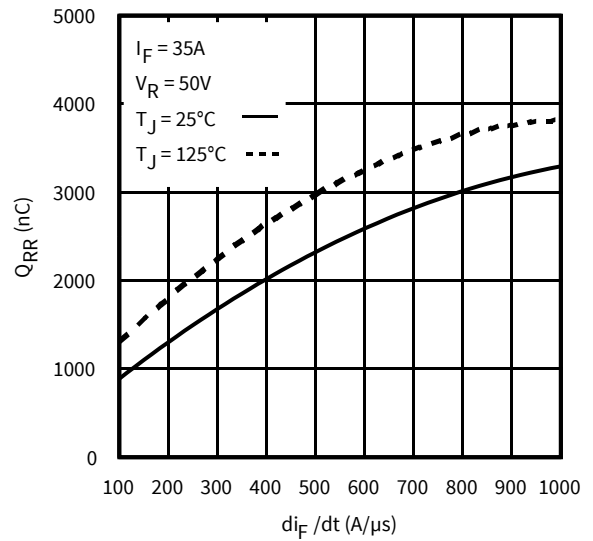

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② starting T_J = 25°C, L = 0.39mH, R_G = 25Ω, I_{AS} = 35A.
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ④ R_θ is measured at T_J of approximately 90°C.
- ⑤ Half sine wave with duty cycle = 0.25, ton=1μsec.
- ⑥ Applicable to Sustain and Energy Recovery applications.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical E_{PULSE} vs. Drain-to-Source Voltage

Fig 6. Typical E_{PULSE} vs. Drain Current


Fig 7. Typical EPULSE vs. Temperature

Fig 8. Typical Source-Drain Diode Forward Voltage

Fig 9. Typical Capacitance vs. Drain-to-Source Voltage

Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

Fig 11. Maximum Drain Current vs. Case Temperature

Fig 12. Maximum Safe Operating Area


Fig 13. On-Resistance Vs. Gate Voltage

Fig 14. Maximum Avalanche Energy Vs. Temperature

Fig 15. Threshold Voltage vs. Temperature

Fig 16. Typical Repetitive peak Current vs. Case temperature

Fig 17. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 18 - Typical Recovery Current vs. di/dt

Fig. 19 - Typical Recovery Current vs. di/dt

Fig. 20 - Typical Stored Charge vs. di/dt

Fig. 21 - Typical Stored Charge vs. di/dt

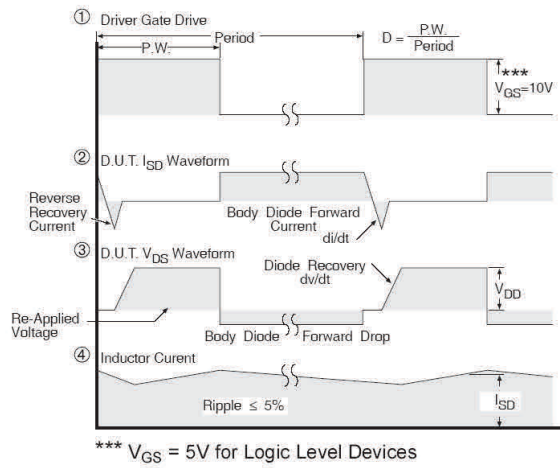
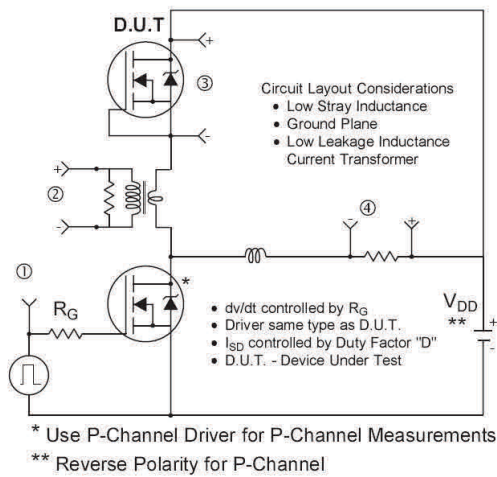
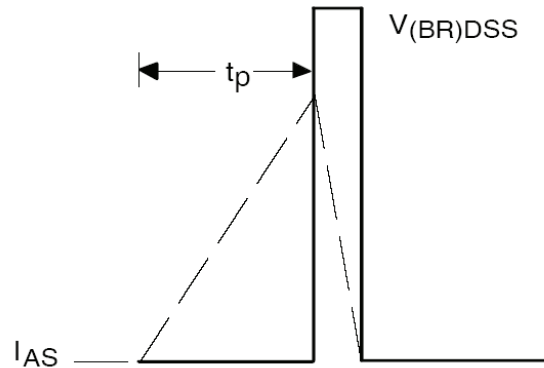
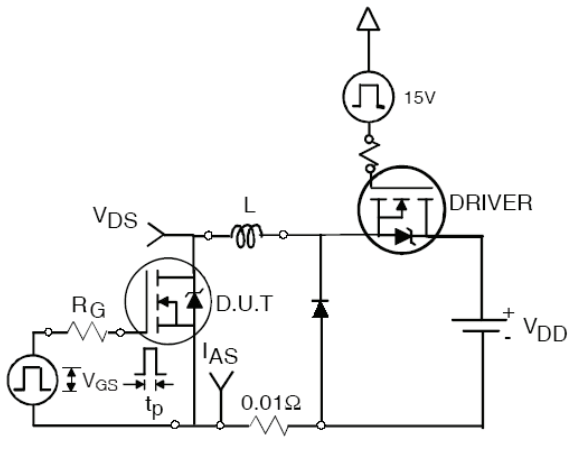

Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

Fig 19a. Unclamped Inductive Test Circuit

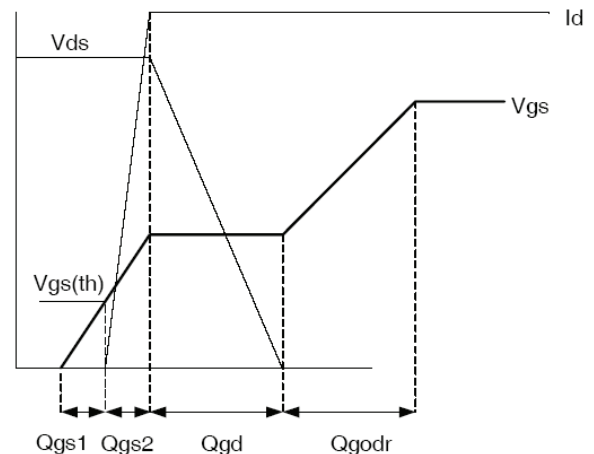
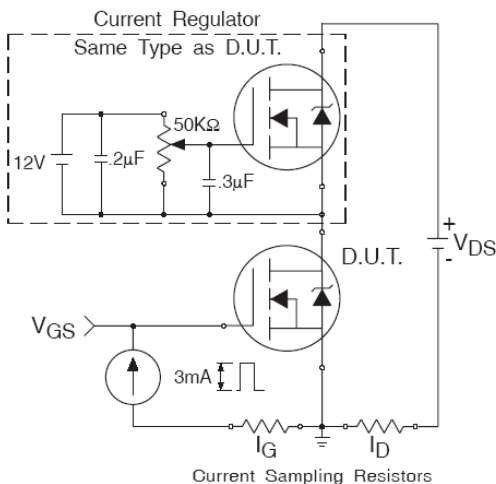
Fig 19b. Unclamped Inductive Waveforms

Fig 20b. Gate Charge Waveform

Fig 20a. Gate Charge Test Circuit

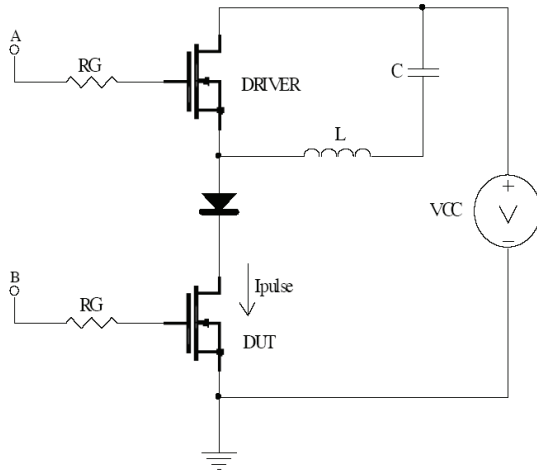
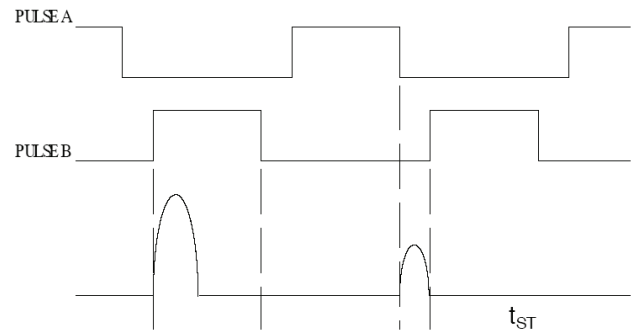
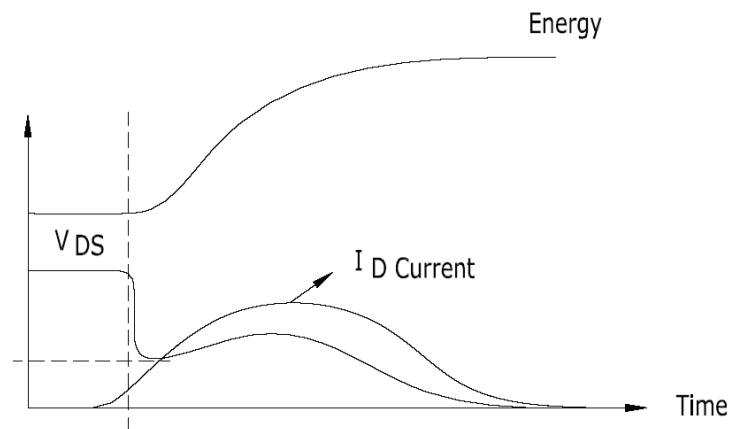
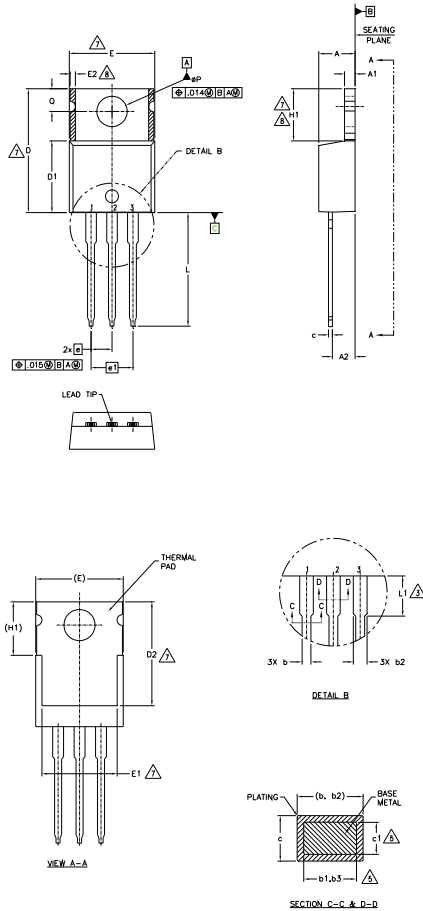

Fig 21a. tst and EPULSE Test Circuit

Fig 21b. tst Test Waveforms

Fig 21c. EPULSE Test Waveforms

Fig 21c. EPULSE Test Waveforms

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		100 BSC		
e1	5.08 BSC		200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ϕP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS
HEMFEET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

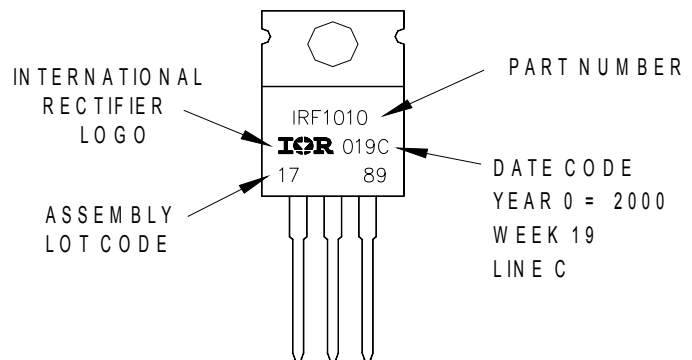
DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 2000
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
 indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	TO-220AB	N/A
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
10/24/2016	<ul style="list-style-type: none"> Changed datasheet with Infineon logo - all pages. Corrected Absolute Maximum table-Storage Temperature range from “-40C” to “-55C” on page1. Corrected Package Outline on page 8. Added disclaimer on last page.
01/11/2018	<ul style="list-style-type: none"> Added typical “Irr”, “Qrr” curves (Fig 18 to Fig 21) on page 6.
08/16/2019	<ul style="list-style-type: none"> Correct typo on Rdson units from “Ω” to “mΩ”-page2

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