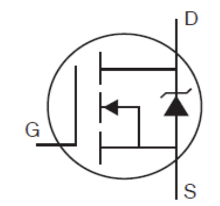
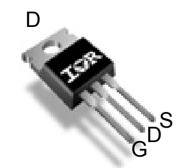
HEXFET® Power MOSFET

Feature

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low E_{PULSE} Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low Q_G for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 175°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

Key Parameters		
V_{DS} min	**250**	**V**
$V_{DS(Avalanche)}$ typ.	**300**	**V**
$R_{DS(on)}$ typ. @ 10V	**29**	**mΩ**
T_J max	**175**	**°C**





TO-220AB
IRFB4332PbF

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB4332PbF	TO-220	Tube	50	IRFB4332PbF

Description

This HEXFET® Power MOSFET is specifically designed for Sustain; Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low EPULSE rating. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications.

Absolute Maximum Ratings

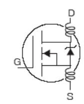
Symbol	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 30	V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	60	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	42	
I_{DM}	Pulsed Drain Current ①	230	
I_{RP} @ T_C = 100°C	Repetitive Peak Current ⑤⑥	120	
P_D @T_C = 25°C	Maximum Power Dissipation	390	W
P_D @T_C = 100°C	Maximum Power Dissipation	200	W
	Linear Derating Factor	2.6	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	——	0.38	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Notes ① through ⑥ are on page 2.

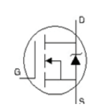
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	170	—	mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	29	33	mΩ	V_{GS} = 10V, I_D = 35A
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient		-14		mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V_{DS} =250 V, V_{GS} = 0V
		—	—	1.0	mA	V_{DS} = 250V,V_{GS} = 0V,T_J =150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—		-100		V_{GS} = -20V
gfs	Forward Trans conductance	100	—	—	S	V_{DS} = 25V, I_D = 35A
Q_g	Total Gate Charge	—	99	150	nC	V_{DD} = 125V, I_D = 35A, V_{GS} = 10V ③
Q_{gd}	Gate-to-Drain Charge	—	35	—		
t_{st}	Shoot Through Blocking Time	100	—	—	ns	V_{DD} = 200V, V_{GS} = 15V, R_G= 4.7Ω
E_{PULSE}	Energy per Pulse	—	520	—	μJ	L = 220nH, C= 0.3μF, V_{GS} = 15V V_{DS} = 200V, R_G= 5.1Ω, T_J = 25°C
		—	920	—		L = 220nH, C= 0.3μF, V_{GS} = 15V V_{DS} = 200V, R_G= 5.1Ω, T_J = 100°C
C_{iss}	Input Capacitance	—	5860	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	530	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	130	—		ƒ = 1.0MHz,
$C_{oss\ eff.}$	Effective Output Capacitance	—	360	—		V_{GS} = 0V, V_{DS} = 0V to 200V
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	230	mJ
E_{AR}	Repetitive Avalanche Energy ①	300	39	mJ
$V_{DS\ (Avalanche)}$	Repetitive Avalanche Voltage①	—	—	V
I_{AS}	Avalanche Current ②	—	35	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S @ T_C = 25°C	Continuous Source Current (Body Diode)	—	—	60	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	230		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 35A,V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	190	290	ns	T_J = 25°C ,I_F = 35A, V_{DD} = 50V
Q_{rr}	Reverse Recovery Charge	—	820	1230	nC	di/dt = 100A/μs ③

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② starting T_J = 25°C, L = 0.39mH, R_G = 25Ω, I_{AS} = 35A.
③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
④ R_θ is measured at T_J of approximately 90°C.
⑤ Half sine wave with duty cycle = 0.25, ton=1μsec.
⑥ Applicable to Sustain and Energy Recovery applications.

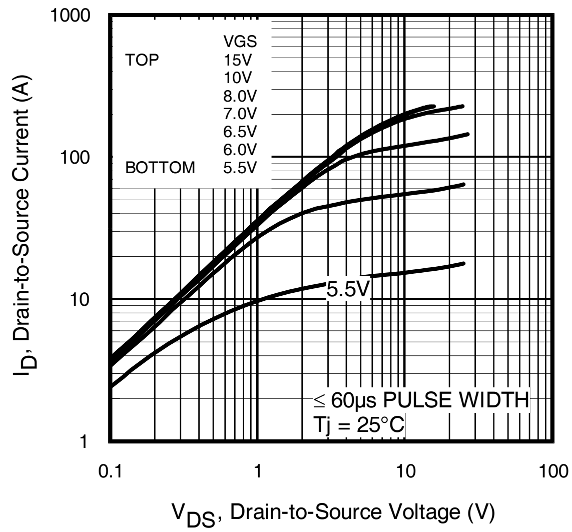


Fig 1. Typical Output Characteristics

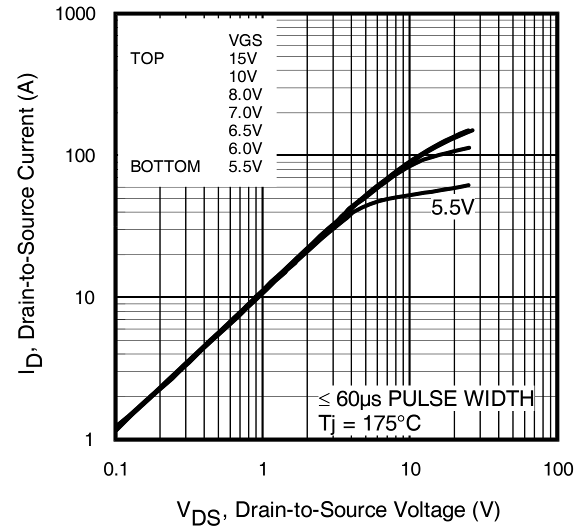


Fig 2. Typical Output Characteristics

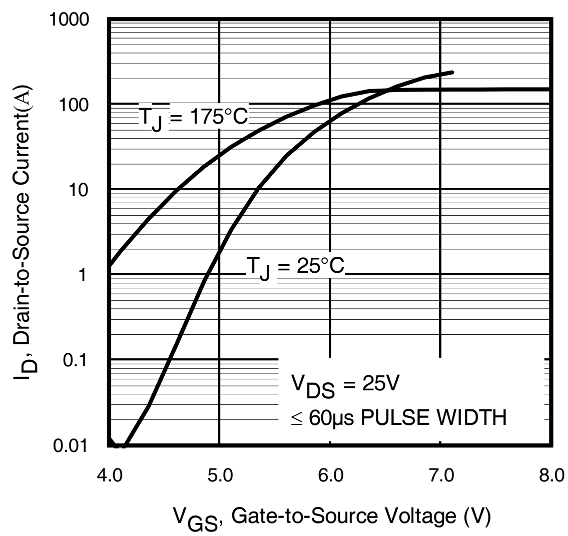


Fig 3. Typical Transfer Characteristics

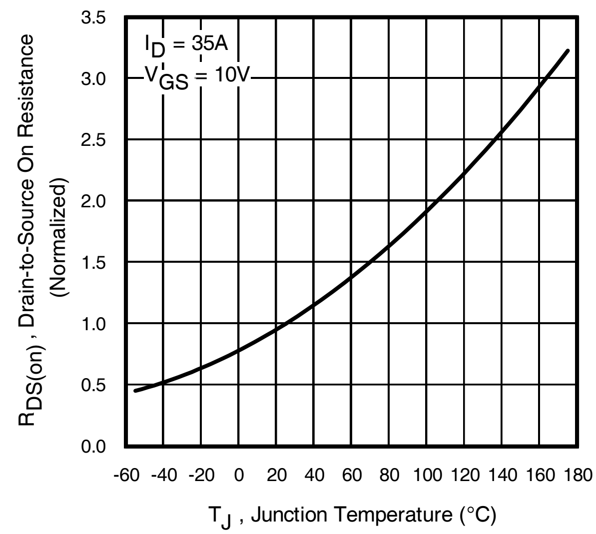


Fig 4. Normalized On-Resistance vs. Temperature

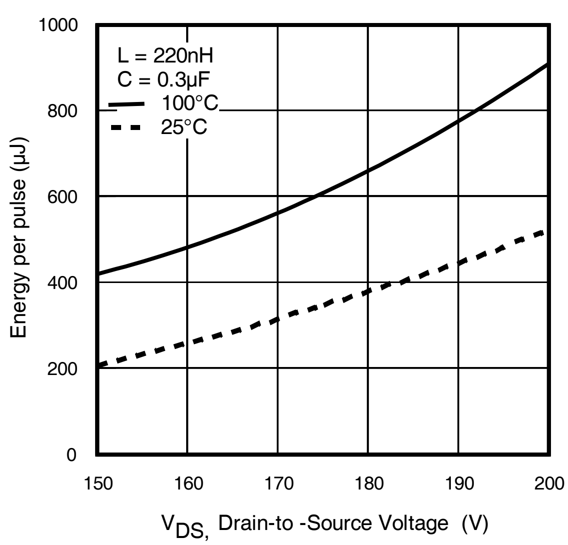


Fig 5. Typical E_{PULSE} vs. Drain-to-Source Voltage

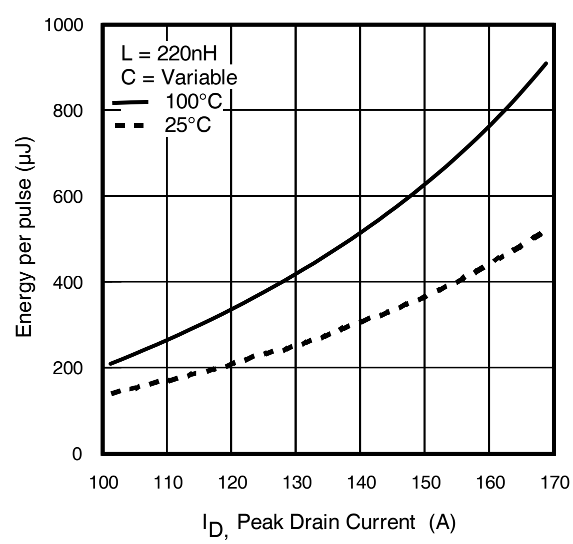


Fig 6. Typical E_{PULSE} vs. Drain Current

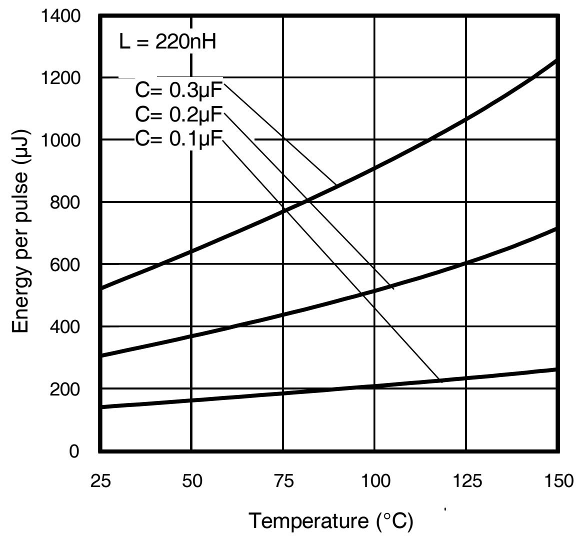


Fig 7. Typical EPULSE vs. Temperature

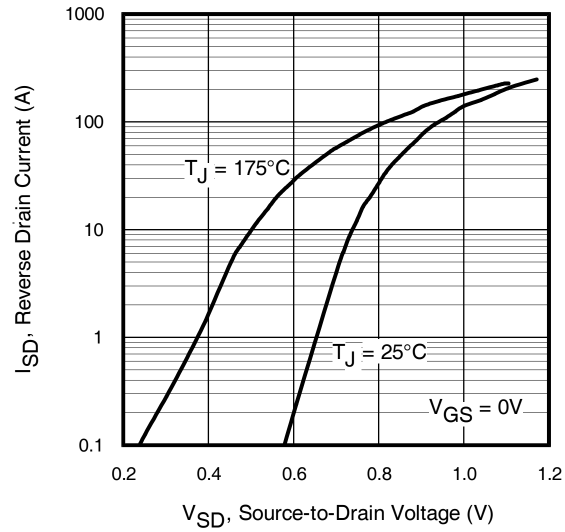


Fig 8. Typical Source-Drain Diode Forward Voltage

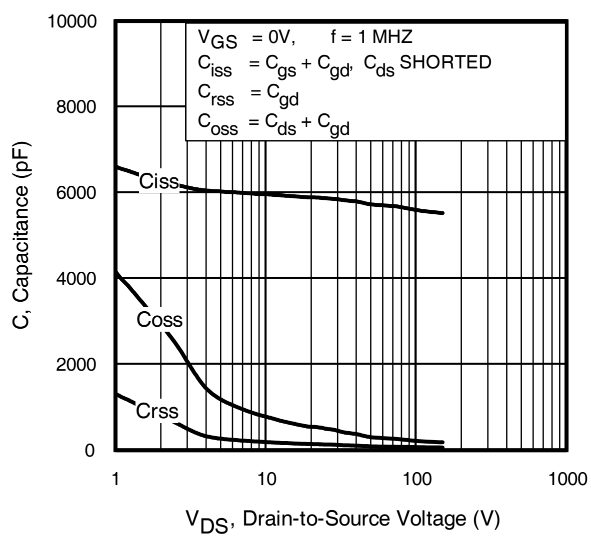


Fig 9. Typical Capacitance vs.Drain-to-Source Voltage

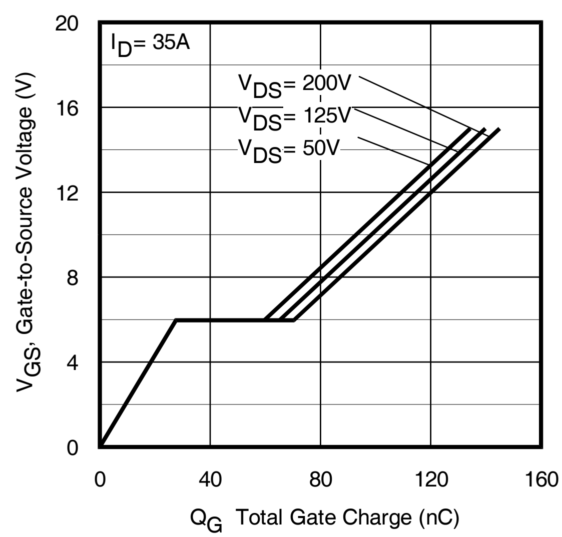


Fig 10. Typical Gate Charge vs.Gate-to-Source Voltage

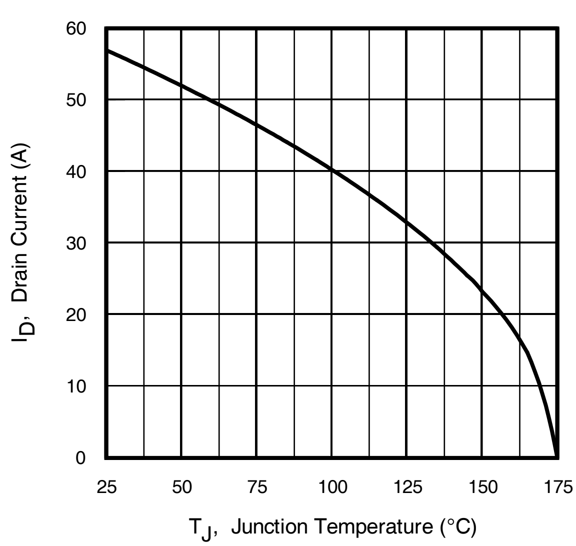


Fig 11. Maximum Drain Current vs. Case Temperature

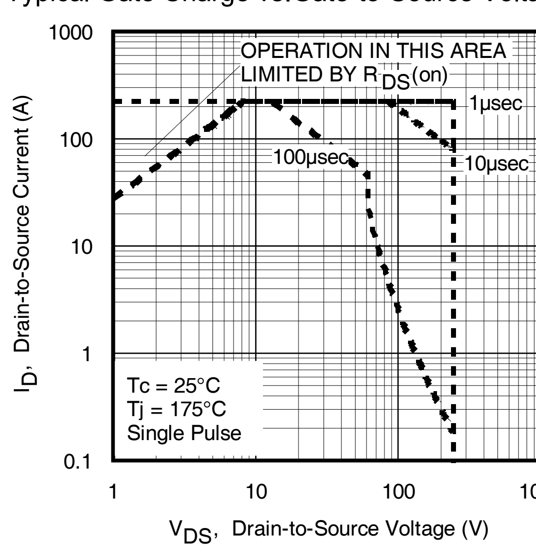


Fig 12. Maximum Safe Operating Area

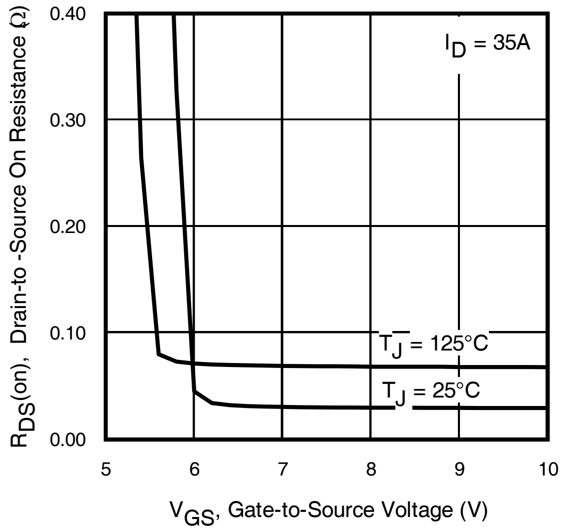


Fig 13. On-Resistance Vs. Gate Voltage

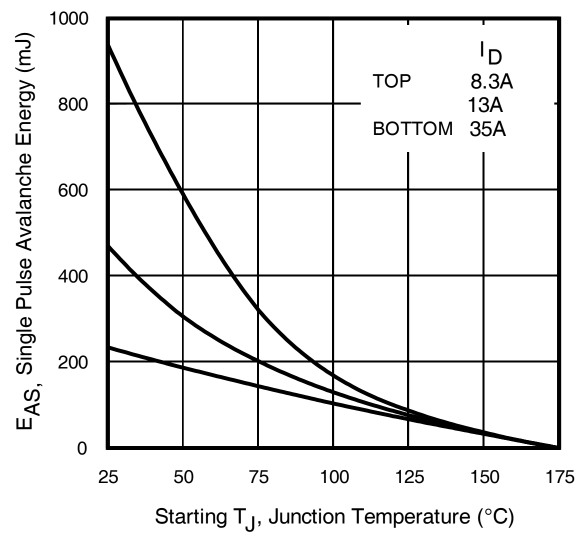


Fig 14. Maximum Avalanche Energy Vs. Temperature

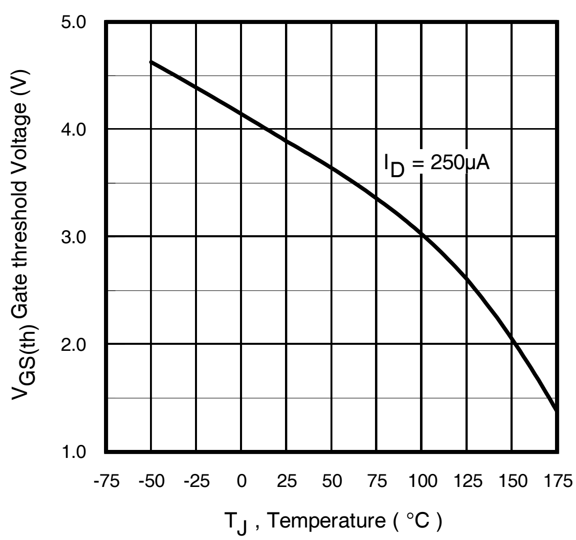


Fig 15. Threshold Voltage vs. Temperature

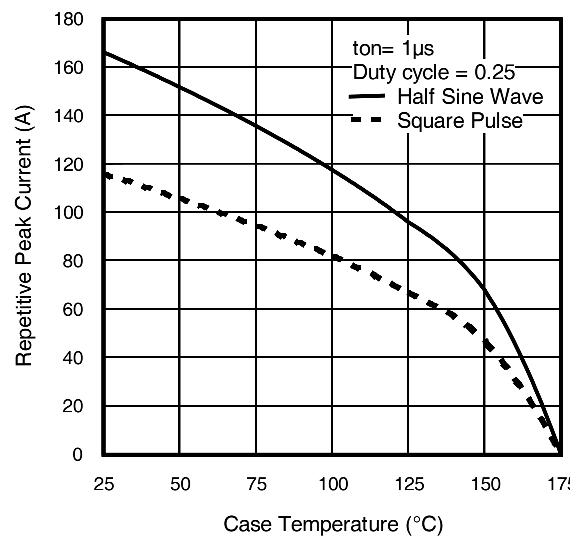
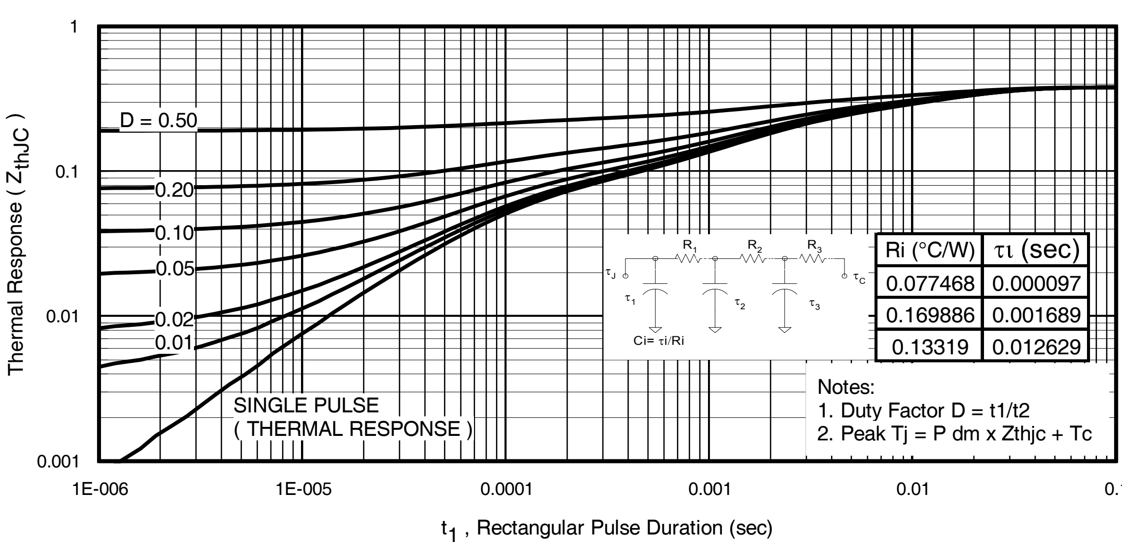


Fig 16. Typical Repetitive peak Current vs. Case temperature



Ri (°C/W)	τι (sec)
0.077468	0.000097
0.169886	0.001689
0.13319	0.012629

Fig 17. Maximum Effective Transient Thermal Impedance, Junction-to-Case

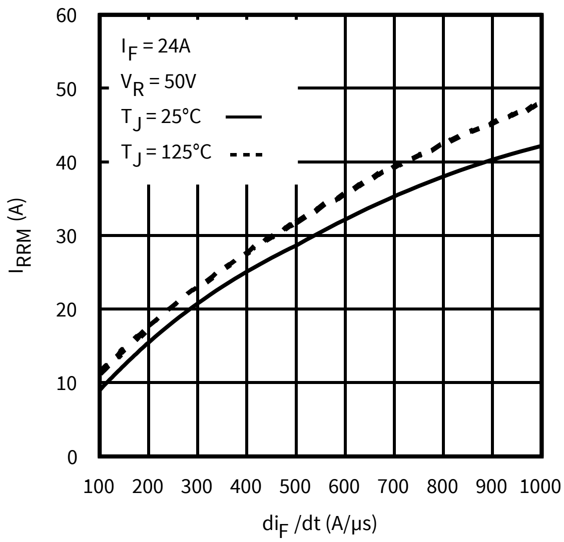


Fig. 18 - Typical Recovery Current vs. dif/dt

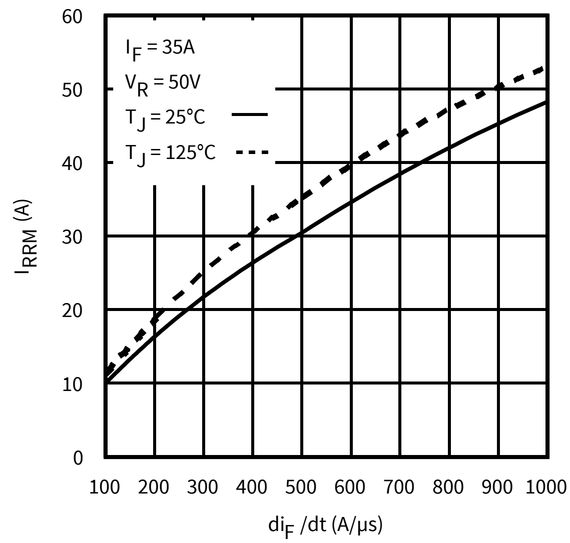


Fig. 19 - Typical Recovery Current vs. dif/dt

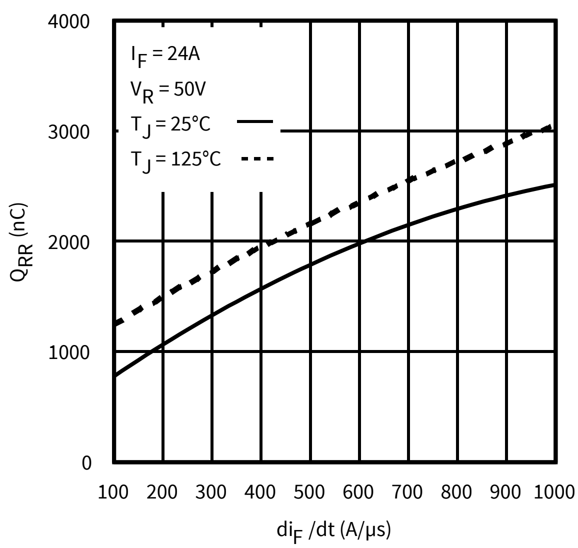


Fig. 20 - Typical Stored Charge vs. dif/dt

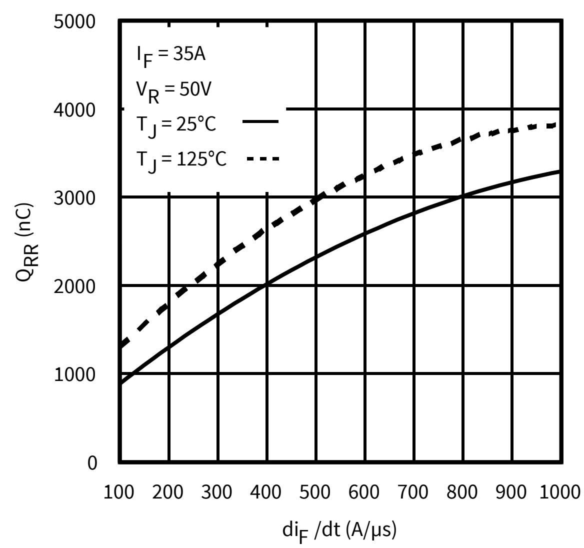


Fig. 21 - Typical Stored Charge vs. dif/dt

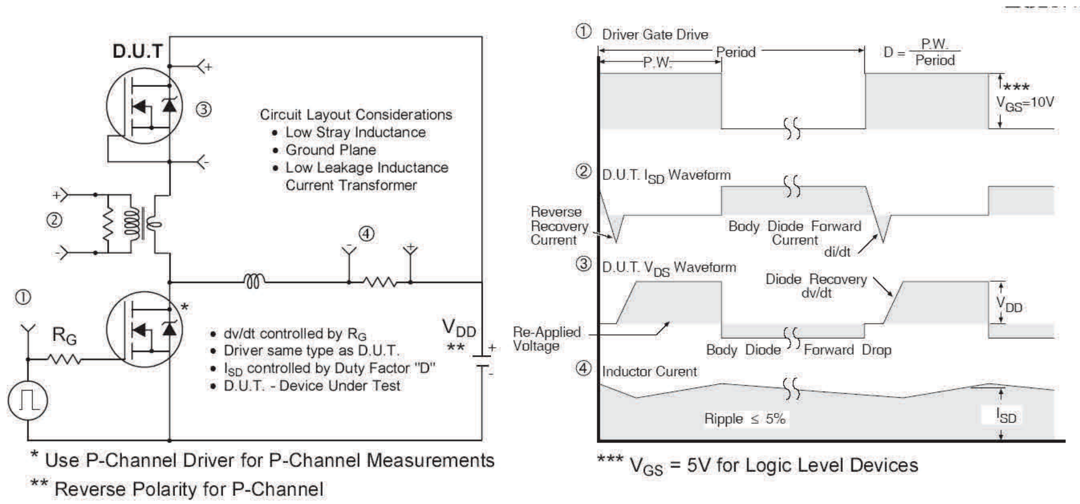


Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

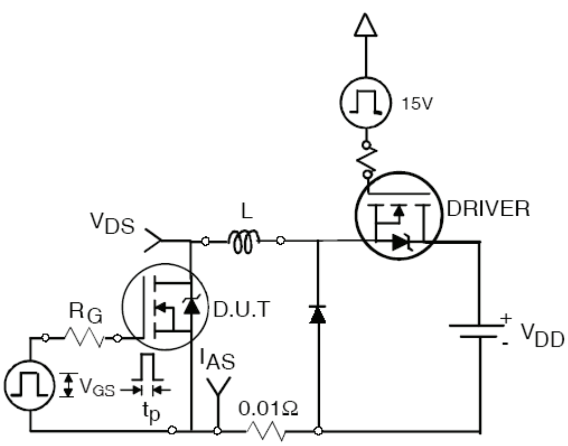


Fig 19a. Unclamped Inductive Test Circuit

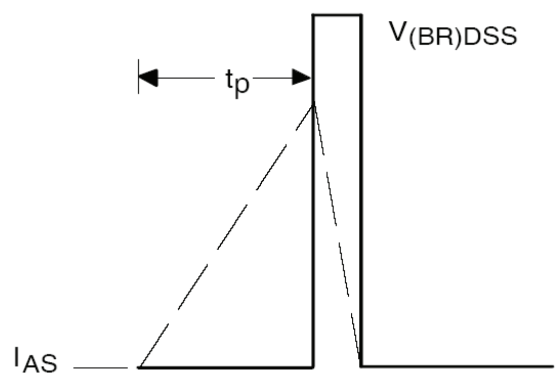


Fig 19b. Unclamped Inductive Waveforms

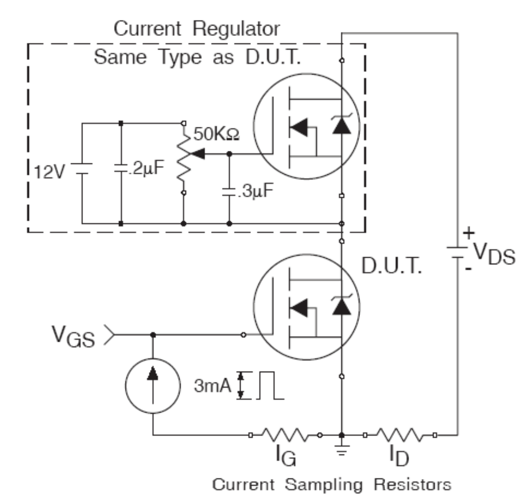


Fig 20b. Gate Charge Waveform

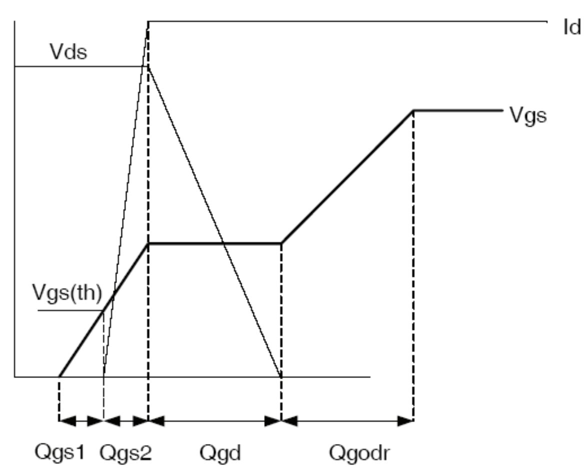


Fig 20a. Gate Charge Test Circuit

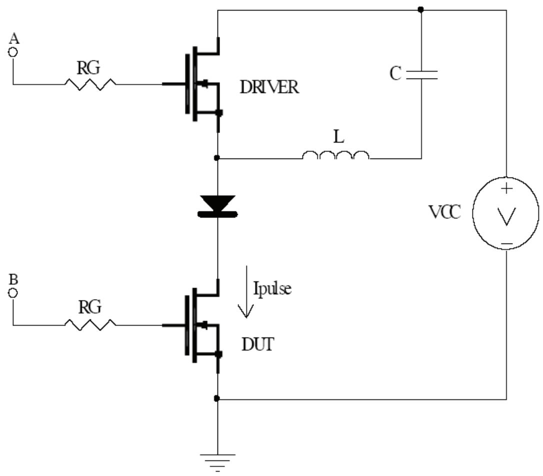


Fig 21a. tst and EPULSE Test Circuit

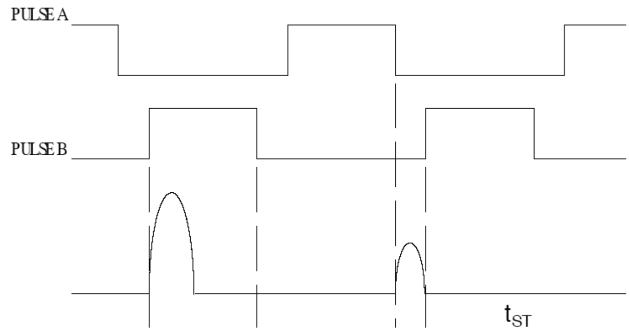


Fig 21b. tst Test Waveforms

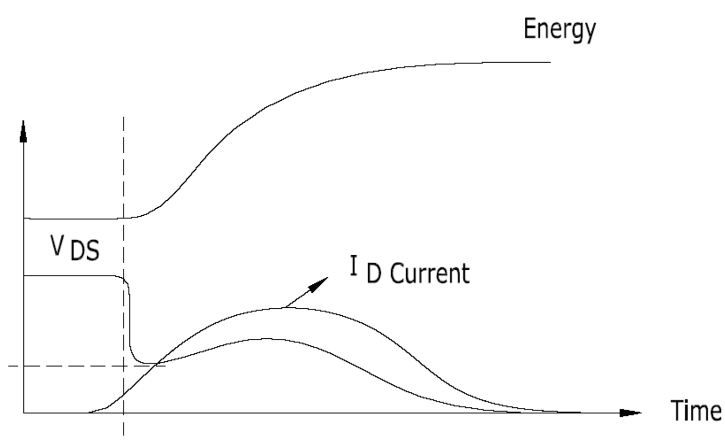
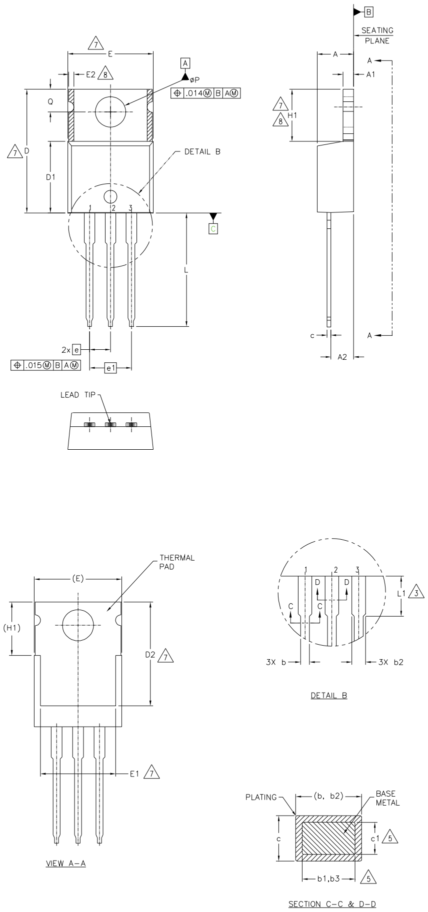


Fig 21c. E_{PULSE} Test Waveforms

Fig 21c. EPULSE Test Waveforms

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.- CONTROLLING DIMENSION : INCHES.
7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE

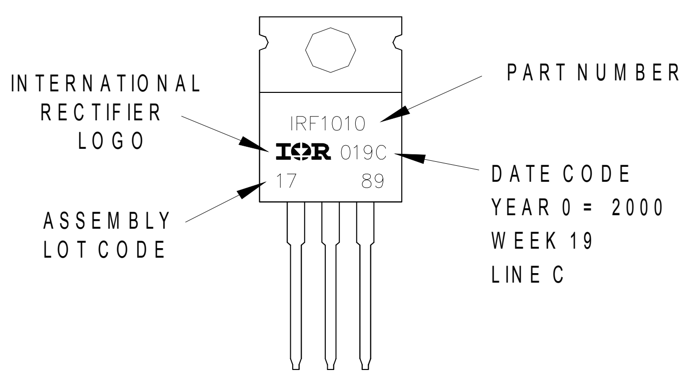
IGBTs, CoPACK
1.- GATE
2.- COLLECTOR
3.- EMITTER

DIODES
1.- ANODE
2.- CATHODE
3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	TO-220AB	N/A
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
10/24/2016	• Changed datasheet with Infineon logo - all pages. • Corrected Absolute Maximum table-Storage Temperature range from "-40C" to "-55C" on page1. • Corrected Package Outline on page 8. • Added disclaimer on last page.
01/11/2018	• Added typical "Irr", "Qrr" curves (Fig 18 to Fig 21) on page 6.
08/16/2019	• Correct typo on Rdson units from "Ω" to "mΩ"-page2

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Do you have a question about this document?
Email: erratum@infineon.com

Document reference
ifx1

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