

# IRFB4321PbF

HEXFET® Power MOSFET

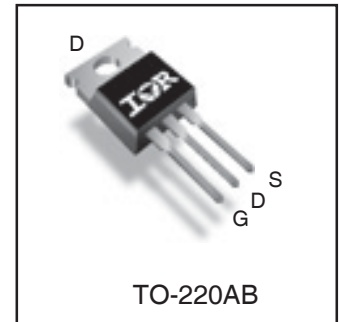
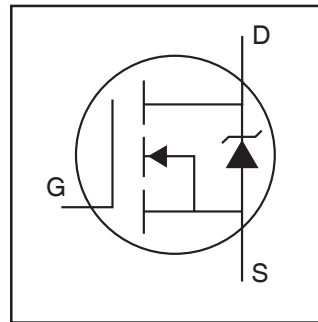
## Applications

- Motion Control Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- Hard Switched and High Frequency Circuits

## Benefits

- Low  $R_{DS(on)}$  Reduces Losses
- Low Gate Charge Improves the Switching Performance
- Improved Diode Recovery Improves Switching & EMI Performance
- 30V Gate Voltage Rating Improves Robustness
- Fully Characterized Avalanche SOA

$V_{DSS}$	<b>150V</b>
$R_{DS(on)}$ <b>typ. max.</b>	<b>12mΩ</b>
	<b>15mΩ</b>
$I_D$	<b>85A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	85 ①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	60	
$I_{DM}$	Pulsed Drain Current ②	330	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	350	W
	Linear Derating Factor	2.3	W/°C
$V_{GS}$	Gate-to-Source Voltage	±30	V
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	120	mJ
$T_J$	Operating Junction and	-55 to +175	
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.43	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	62	

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

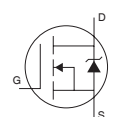
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	150	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	150	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA <sup>②</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	12	15	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 33A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V
		—	—	1.0	mA	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
R <sub>G(int)</sub>	Internal Gate Resistance	—	0.8	—	Ω	

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	130	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 50A
Q <sub>g</sub>	Total Gate Charge	—	71	110	nC	I <sub>D</sub> = 50A V <sub>DS</sub> = 75V V <sub>GS</sub> = 10V <sup>④</sup>
Q <sub>gs</sub>	Gate-to-Source Charge	—	24	—	nC	
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	21	—	nC	
t <sub>d(on)</sub>	Turn-On Delay Time	—	18	—	ns	V <sub>DD</sub> = 98V I <sub>D</sub> = 50A R <sub>G</sub> = 2.5Ω V <sub>GS</sub> = 10V <sup>④</sup>
t <sub>r</sub>	Rise Time	—	60	—	ns	
t <sub>d(off)</sub>	Turn-Off Delay Time	—	25	—	ns	
t <sub>f</sub>	Fall Time	—	35	—	ns	
C <sub>iss</sub>	Input Capacitance	—	4460	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	390	—	pF	V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	82	—	pF	f = 1.0MHz

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	85 <sup>①</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	330	A	
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 50A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	89	130	ns	I <sub>D</sub> = 50A
Q <sub>rr</sub>	Reverse Recovery Charge	—	300	450	nC	V <sub>R</sub> = 128V, di/dt = 100A/μs <sup>④</sup>
I <sub>RRM</sub>	Reverse Recovery Current	—	6.5	—	A	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.095mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 50A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.

- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C

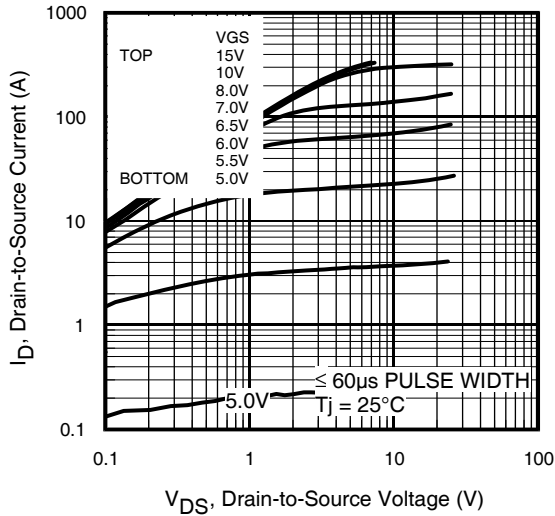


Fig 1. Typical Output Characteristics

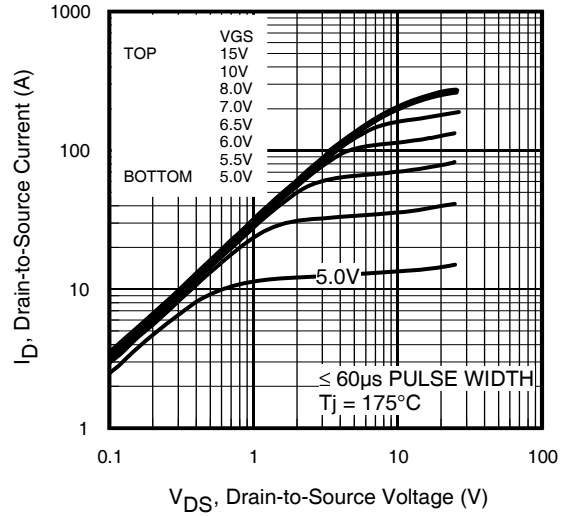


Fig 2. Typical Output Characteristics

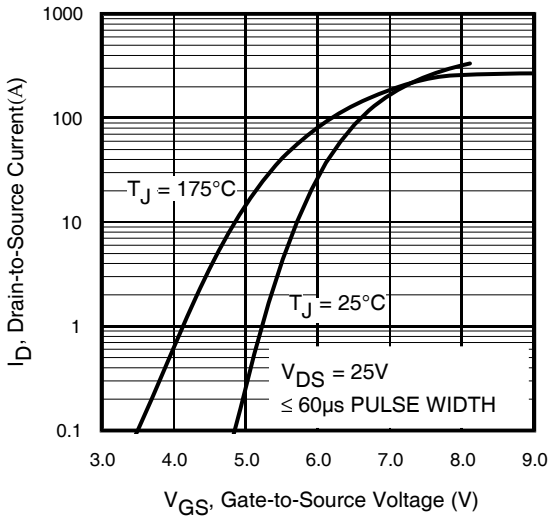


Fig 3. Typical Transfer Characteristics

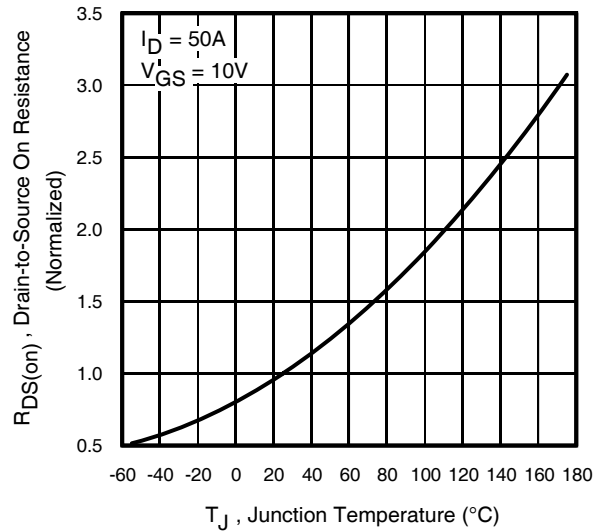


Fig 4. Normalized On-Resistance vs. Temperature

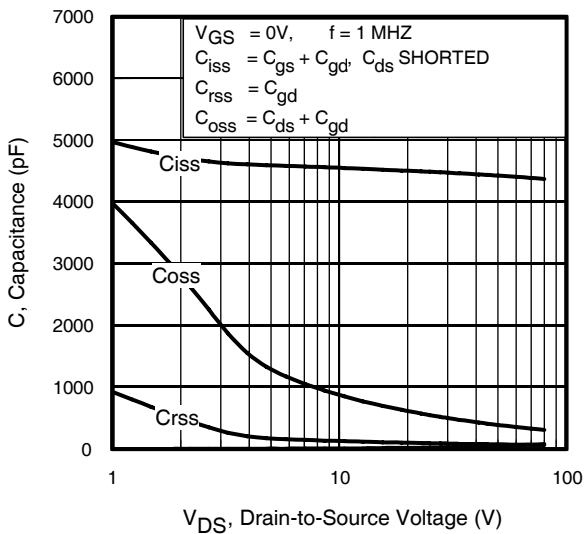


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

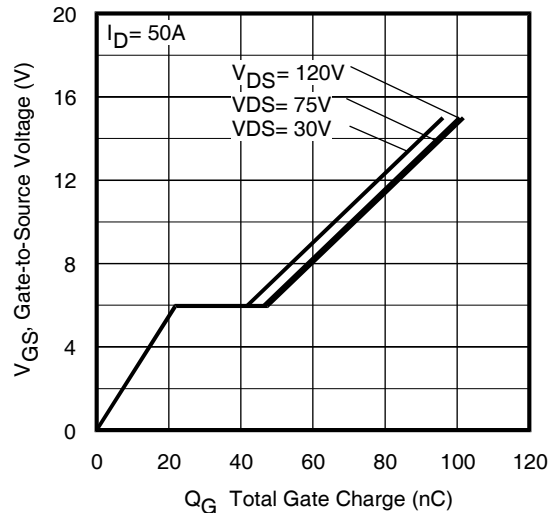
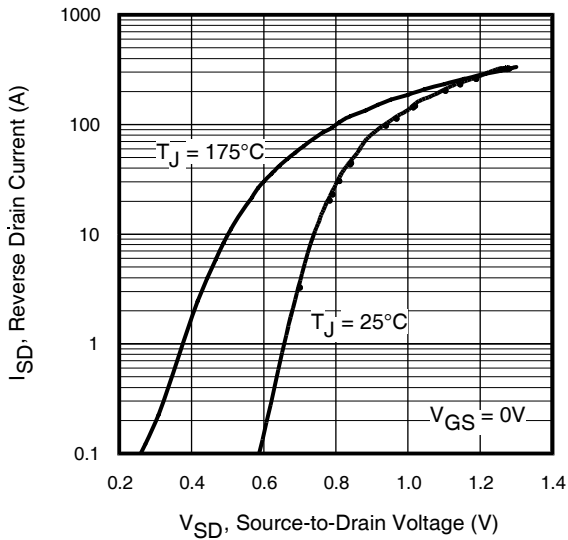
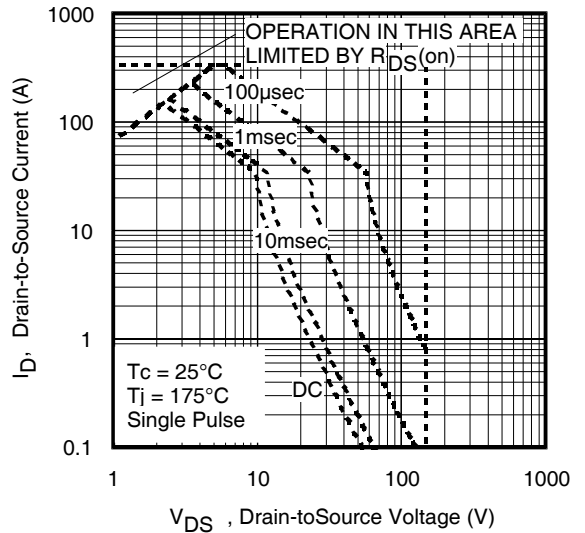


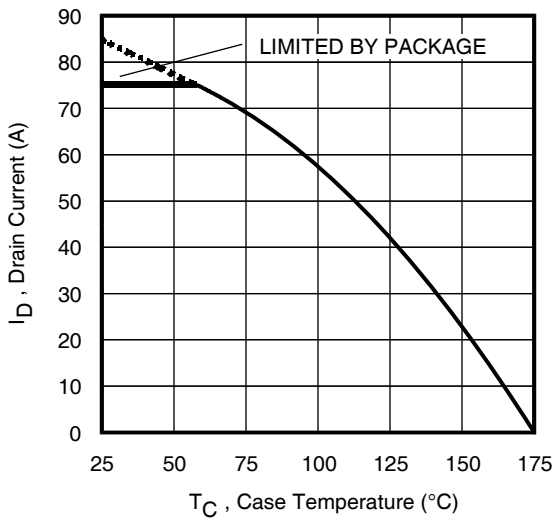
Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



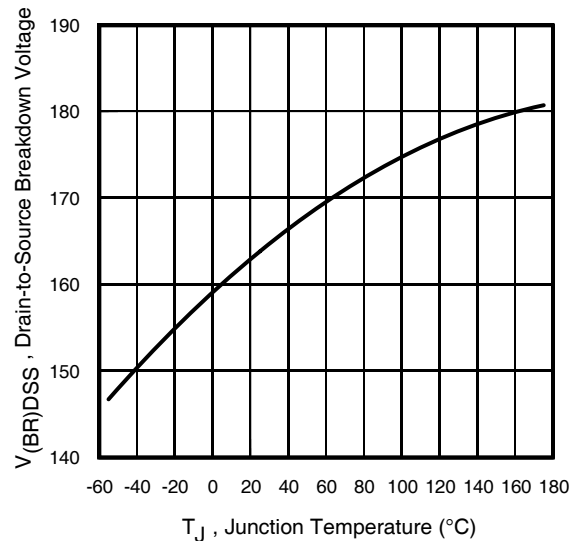
**Fig 7.** Typical Source-Drain Diode Forward Voltage



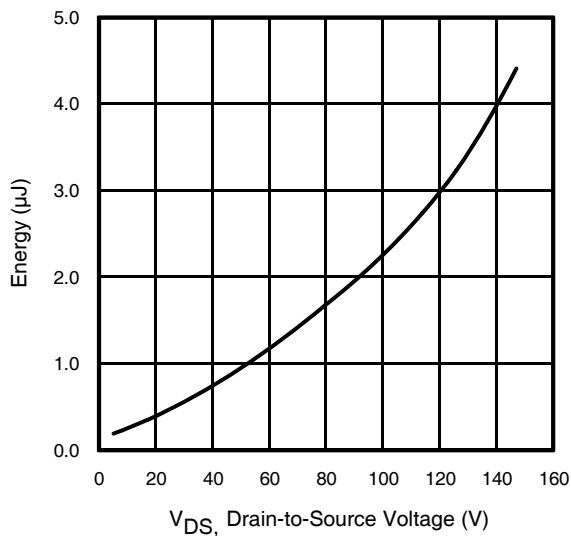
**Fig 8.** Maximum Safe Operating Area



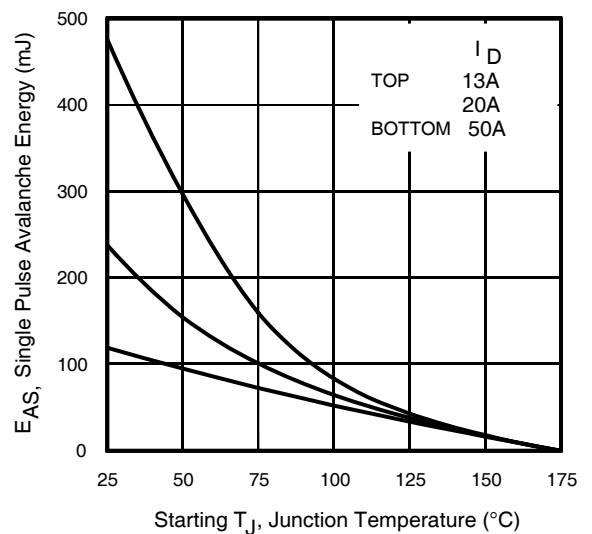
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy Vs. Drain Current

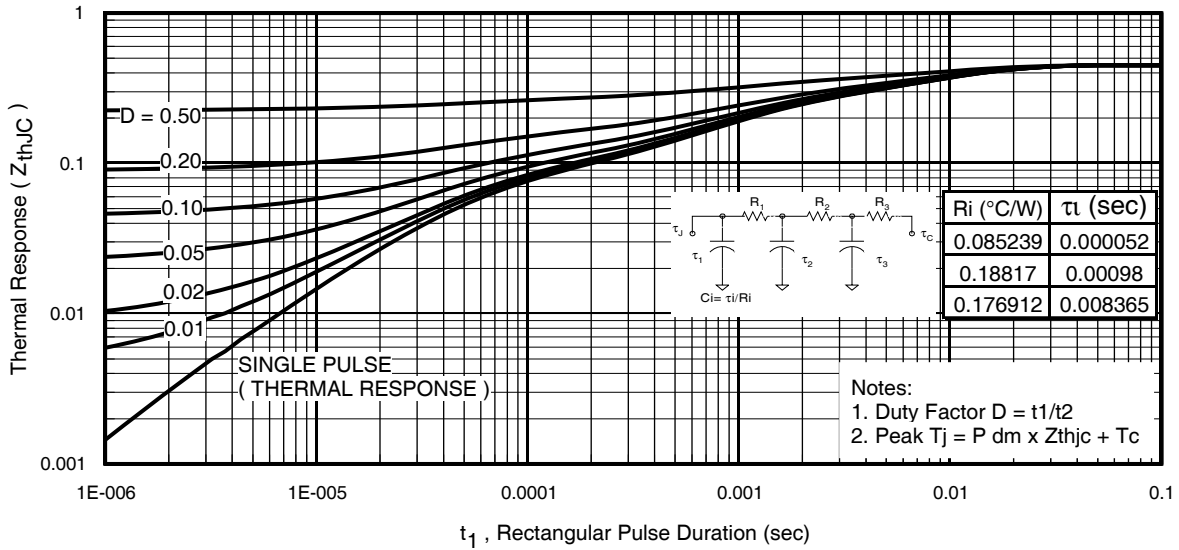


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

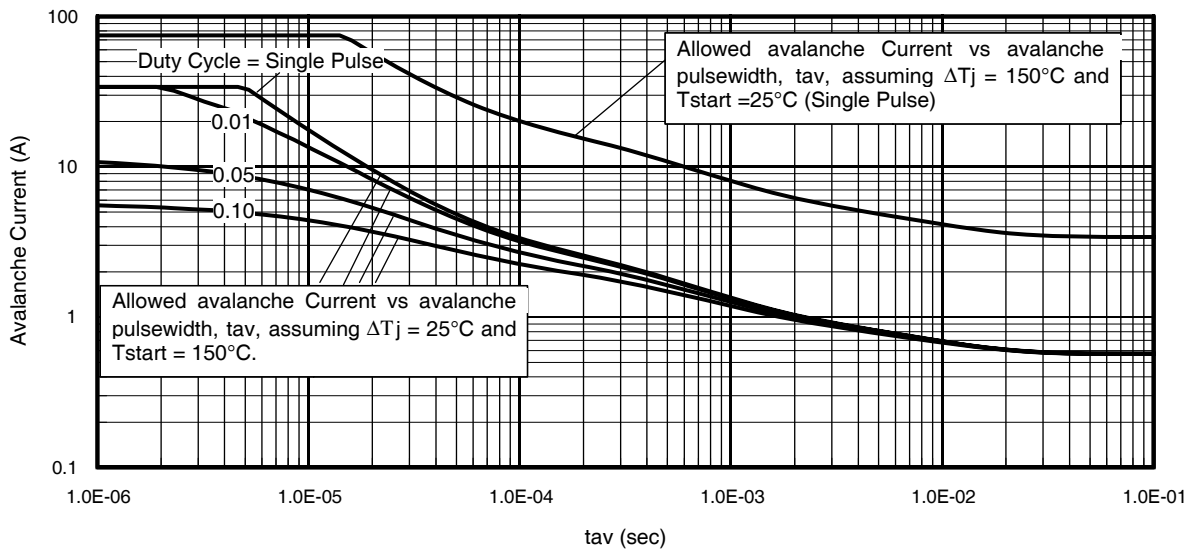
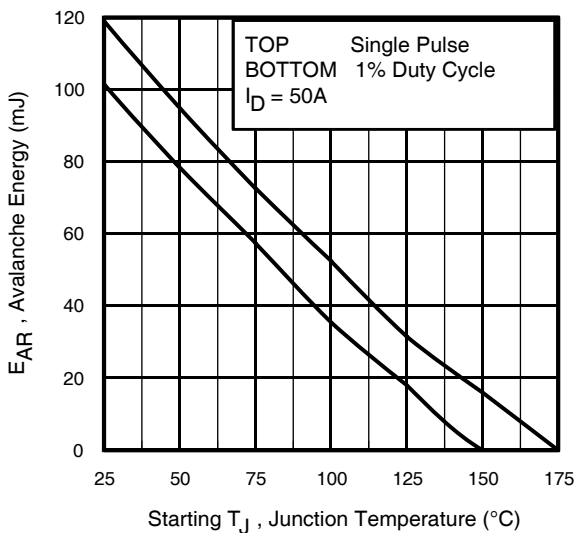


Fig 14. Typical Avalanche Current vs. Pulsewidth



**Notes on Repetitive Avalanche Curves, Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

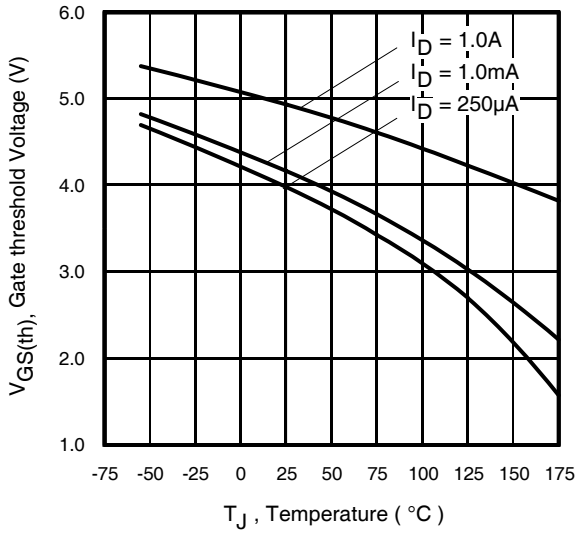


Fig 16. Threshold Voltage Vs. Temperature

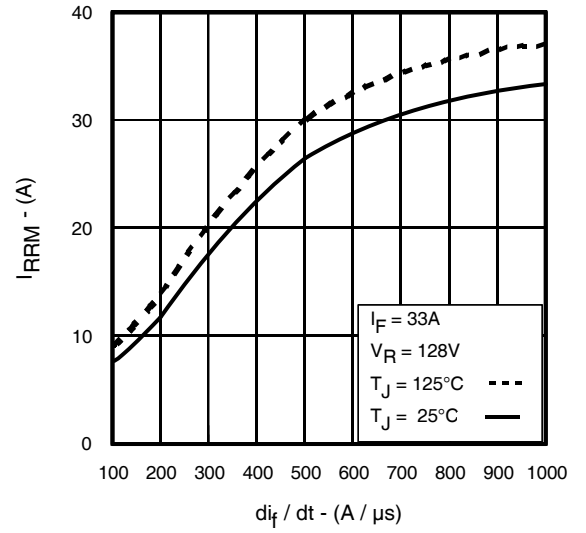


Fig. 17 - Typical Recovery Current vs.  $di_f/dt$

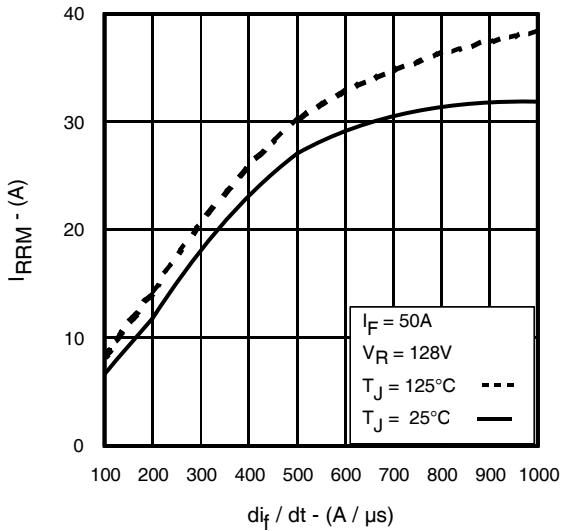


Fig. 18 - Typical Recovery Current vs.  $di_f/dt$

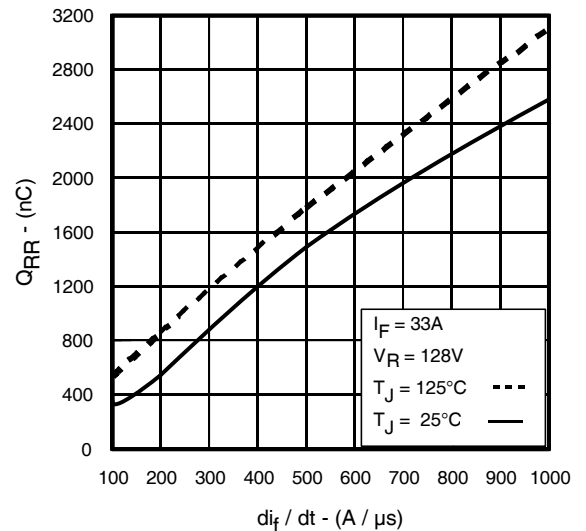


Fig. 19 - Typical Stored Charge vs.  $di_f/dt$

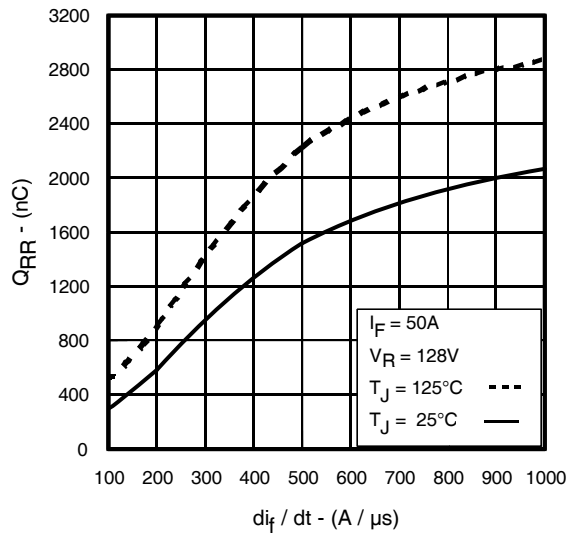
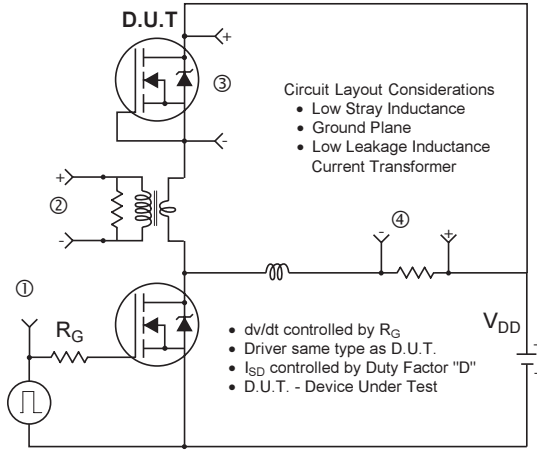
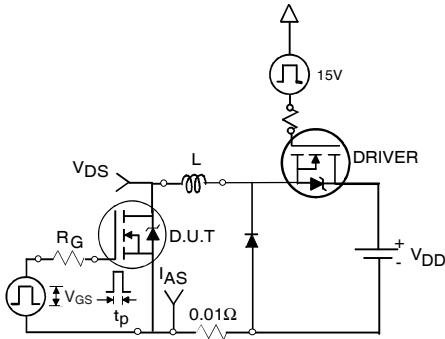


Fig. 20 - Typical Stored Charge vs.  $di_f/dt$



\*  $V_{GS} = 5V$  for Logic Level Devices

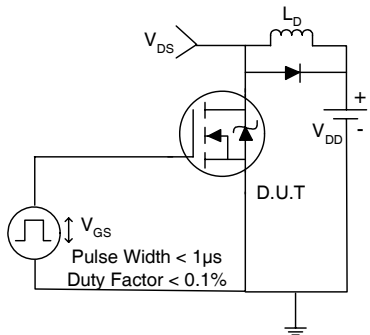
**Fig 21.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs



**Fig 22a.** Unclamped Inductive Test Circuit



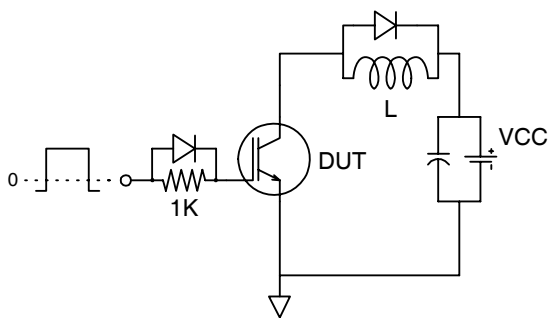
**Fig 22b.** Unclamped Inductive Waveforms



**Fig 23a.** Switching Time Test Circuit



**Fig 23b.** Switching Time Waveforms

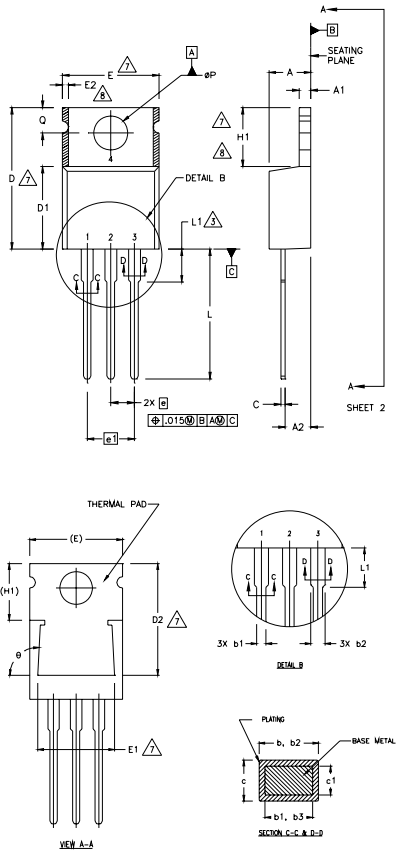


**Fig 24a.** Gate Charge Test Circuit



**Fig 24b.** Gate Charge Waveform

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS).
- 3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5 DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
- 6 CONTROLLING DIMENSION : INCHES.
- 7 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8 DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

LEAD ASSIGNMENTS

HEXLET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

DIODES

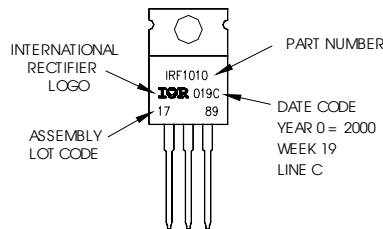
- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	3.56	4.82	.140	.190	5	
A1	0.51	1.40	.020	.055		
A2	2.04	2.92	.080	.115		
b	0.38	1.01	.015	.040		
b1	0.38	0.96	.015	.038		
b2	1.15	1.77	.045	.070		
b3	1.15	1.73	.045	.068		
c	0.36	0.61	.014	.024		
c1	0.36	0.56	.014	.022		
D	14.22	16.51	.560	.650		4
D1	8.38	9.02	.330	.365		4,7
D2	12.19	12.88	.480	.507		
E	9.66	10.66	.380	.420		7
E1	8.38	8.89	.330	.350	7	
e	2.54 BSC		.100 BSC		7,8	
e1	5.08		.200 BSC			
H1	5.85	6.55	.230	.270	3	
L	12.70	14.73	.500	.580		
L1	-	6.35	-	.250	3	
ϕP	3.54	4.08	.139	.161		
O	2.54	3.42	.100	.135	90°-93°	
ϕ						

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 2000  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position  
 indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.



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