**Applications**
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

**Benefits**
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D$ @ $T_J = 25°C$</td>
<td>Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)</td>
<td>210A</td>
<td>A</td>
</tr>
<tr>
<td>$I_D$ @ $T_J = 100°C$</td>
<td>Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)</td>
<td>150A</td>
<td>A</td>
</tr>
<tr>
<td>$I_D$ @ $T_J = 25°C$</td>
<td>Continuous Drain Current, $V_{GS} @ 10V$ (Wire Bond Limited)</td>
<td>120</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DM}$</td>
<td>Pulsed Drain Current</td>
<td>840</td>
<td>A</td>
</tr>
<tr>
<td>$P_D$ @ $T_J = 25°C$</td>
<td>Maximum Power Dissipation</td>
<td>300</td>
<td>W</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate-to-Source Voltage</td>
<td>$\pm 20$</td>
<td>V</td>
</tr>
<tr>
<td>$dV/dt$</td>
<td>Peak Diode Recovery</td>
<td>5.0</td>
<td>V/ns</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating Junction Temperature</td>
<td>-55 to +175</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature Range</td>
<td>-55 to +175</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Soldering Temperature, for 10 seconds (1.6mm from case)</td>
<td>300</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Mounting torque, 6-32 or M3 screw</td>
<td>10lbf-in (1.1N-m)</td>
<td></td>
</tr>
</tbody>
</table>

### Avalanche Characteristics

- Single Pulse Avalanche Energy $E_{AS}$ (Thermal limited) | 170 | mJ |
- Avalanche Current $I_{AR}$ | See Fig. 14, 15, 22a, 22b, | A |
- Repetitive Avalanche Energy $E_{AR}$ | |

### Thermal Resistance

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JUC}$</td>
<td>Junction-to-Case</td>
<td></td>
<td>0.50</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JCS}$</td>
<td>Case-to-Sink, Flat Greased Surface, TO-220</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{JUA}$</td>
<td>Junction-to-Ambient, TO-220</td>
<td></td>
<td>62</td>
<td></td>
</tr>
</tbody>
</table>

**www.irf.com**
Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

Repetitive rating; pulse width limited by max. junction temperature.

Limited by $T_{j,max}$, starting $T_j = 25^\circ C$, $L = 0.023mH$

$R_G = 25\Omega$, $I_{AS} = 120A$, $V_{GS} = 10V$. Part not recommended for use above this value.

Notes:

1. Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

2. Repetitive rating; pulse width limited by max. junction temperature.

3. Limited by $T_{j,max}$, starting $T_j = 25^\circ C$, $L = 0.023mH$

$R_G = 25\Omega$, $I_{AS} = 120A$, $V_{GS} = 10V$. Part not recommended for use above this value.

\[ V_{BSR} \]
\[ \Delta V_{BR} \]
\[ R_D S_{(on)} \]
\[ V_{GS(th)} \]
\[ I_{DSS} \]
\[ I_{GSS} \]
\[ R_I \]

\[ V_{\text{DR}S} \]
\[ V_{\text{BSR}} \]
\[ I_{\text{DSS}} \]
\[ I_{\text{GSS}} \]
\[ R_I \]

\[ I_{\text{DS}} \]
\[ I_{\text{MS}} \]
\[ V_{\text{SD}} \]
\[ I_{\text{R}} \]
\[ O_{\text{R}} \]
\[ I_{\text{RMM}} \]
\[ t_{\text{on}} \]
Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage
**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical $C_{oss}$ Stored Energy

**Fig 12.** Maximum Avalanche Energy Vs. DrainCurrent
Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{j\text{max}}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{j\text{max}}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(\text{ave})}$ = Average power dissipation per single avalanche pulse.
5. $BV$ = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{j\text{max}}$ (assumed as 25°C in Figure 14, 15).
   $t_{av}$ = Average time in avalanche.
   $D$ = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{\text{thJC}}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$P_{D(\text{ave})} = \frac{1}{2} (1.3 \cdot BV \cdot I_{av}) = \frac{\Delta T}{Z_{\text{thJC}}}$

$I_{av} = 2 \frac{\Delta T}{[1.3 \cdot BV \cdot Z_{n}]}$

$E_{AS (AR)} = P_{D(\text{ave})} \cdot t_{av}^2$
IRFB3206GpbF

Fig 16. Threshold Voltage Vs. Temperature

-75 -50 -25 0 25 50 75 100 125 150 175
TJ , Temperature (ºC)

1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5
VGS(th) Gate threshold Voltage (V)

ID = 1.0A
ID = 1.0mA
ID = 250µA
ID = 150µA

Fig. 17 - Typical Recovery Current vs. di/dt

100 200 300 400 500 600 700 800 900 1000
di/dt - (A / µs)

0 2 4 6 8 10 12 14 16 18
I_RRM - (A)

IF = 30A
VR = 51V
TJ = 125°C
TJ = 25°C

Fig. 18 - Typical Recovery Current vs. di/dt

0 2 4 6 8 10 12 14 16 18
I_RRM - (A)

IF = 45A
VR = 51V
TJ = 125°C
TJ = 25°C

Fig. 19 - Typical Stored Charge vs. di/dt

0 50 100 150 200 250 300 350
QRR - (nC)

IF = 30A
VR = 51V
TJ = 125°C
TJ = 25°C

Fig. 20 - Typical Stored Charge vs. di/dt

0 50 100 150 200 250 300 350
QRR - (nC)

IF = 45A
VR = 51V
TJ = 125°C
TJ = 25°C
Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 22a. Unclamped Inductive Test Circuit

Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit

Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform
TO-220AB Package Outline
Dimensions are shown in millimeters (inches)

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRFB4310GPBF

Note: "G" suffix in part number indicates "Halogen - Free"

Note: "P" in assembly line position indicates "Lead - Free"

TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

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