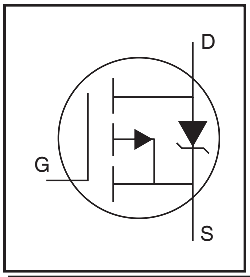
International
IOR Rectifier

PD - 96030

IRF9540NSPbF
IRF9540NLPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Some Parameters are Different from IRF9540NS/L
- P-Channel
- Lead-Free



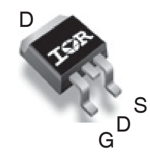
V_{DSS} = -100V

$R_{DS(on)}$ = 117mΩ

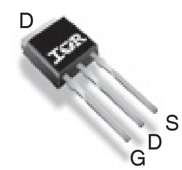
I_D = -23A

Description

Features of this design are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in a wide variety of other applications.



D^2Pak
IRF9540NSPbF



TO-262
IRF9540NLPbF

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

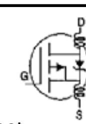
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-23	A
I_D @ T_C = 100°C	Continuous Drain Current, VGS @ -10V	-14	
I_{DM}	Pulsed Drain Current ①	-92	
P_D @T_A = 25°C	Maximum Power Dissipation	3.1	W
P_D @T_C = 25°C	Maximum Power Dissipation	110	
	Linear Derating Factor	0.9	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	84	mJ
I_{AR}	Avalanche Current ①	-14	A
E_{AR}	Repetitive Avalanche Energy ①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-13	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

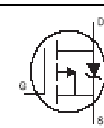
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑤	——	40	

09/30/05

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	–––	–––	V	V_{GS} = 0V, I_D = -250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	-0.11	–––	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	117	mΩ	V_{GS} = -10V, I_D = -14A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	–––	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
gfs	Forward Transconductance	5.6	–––	–––	S	V_{DS} = -50V, I_D = -14A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	-50	µA	V_{DS} = -100V, V_{GS} = 0V
		–––	–––	-250		V_{DS} = -80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = 20V
Q_g	Total Gate Charge	–––	73	110	nC	I_D = -14A
Q_{gs}	Gate-to-Source Charge	–––	13	20		V_{DS} = -80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	38	57		V_{GS} = -10V ④
$t_{d(on)}$	Turn-On Delay Time	–––	13	–––	ns	V_{DD} = -50V
t_r	Rise Time	–––	64	–––		I_D = -14A
$t_{d(off)}$	Turn-Off Delay Time	–––	40	–––		R_G = 5.1Ω
t_f	Fall Time	–––	45	–––		V_{GS} = -10V ④
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.) 
L_S	Internal Source Inductance	–––	7.5	–––		from package and center of die contact
C_{iss}	Input Capacitance	–––	1450	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	430	–––		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	–––	230	–––		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	-23	A	MOSFET symbol showing the 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	-92		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	–––	–––	-1.6	V	T_J = 25°C, I_S = -14A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	140	210	ns	T_J = 25°C, I_F = -14A, V_{DD} = -25V
Q_{rr}	Reverse Recovery Charge	–––	890	1340	nC	di/dt = -100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.88mH R_G = 25Ω, I_{AS} = -14A. (See Figure 12)

③ $I_{SD} \leq$ -14A, di/dt $\leq$ -620A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C.

④ Pulse width $\leq$ 300µs; duty cycle $\leq$ 2%.

⑤ When mounted on 1" square PCB (FR-4or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

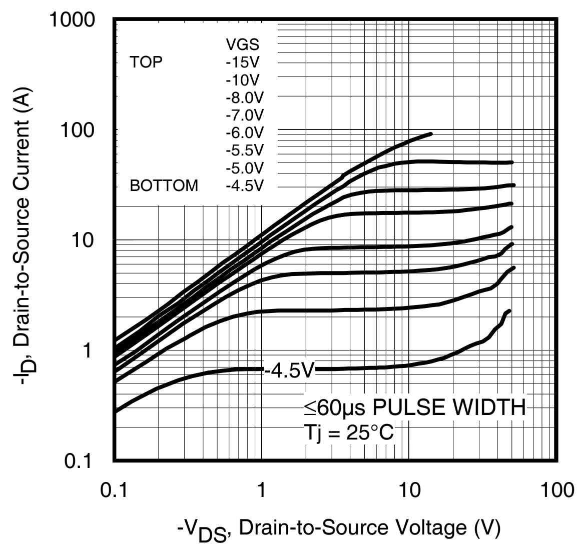


Fig 1. Typical Output Characteristics

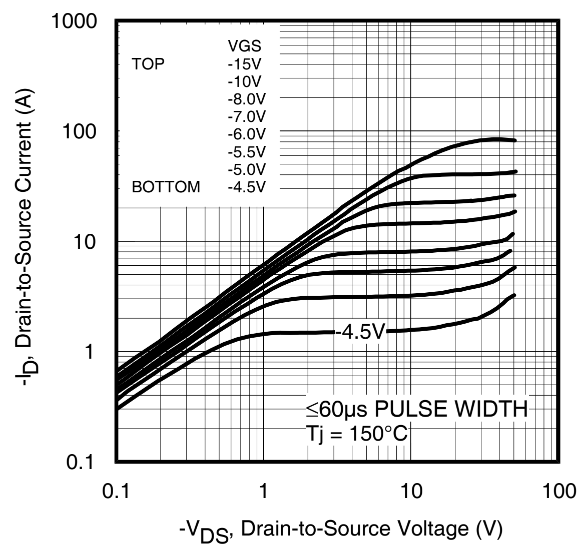


Fig 2. Typical Output Characteristics

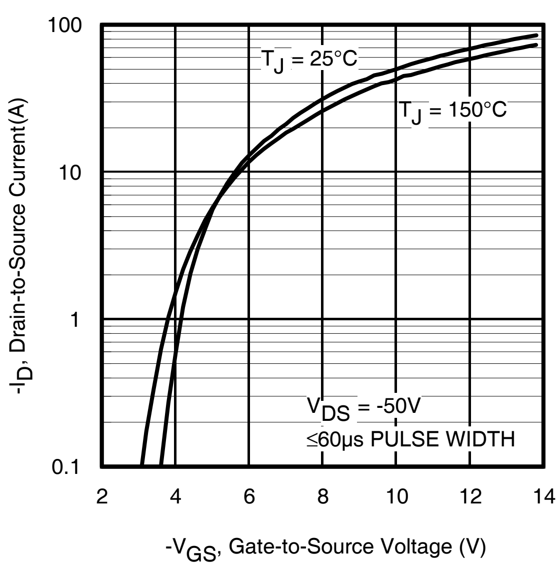


Fig 3. Typical Transfer Characteristics

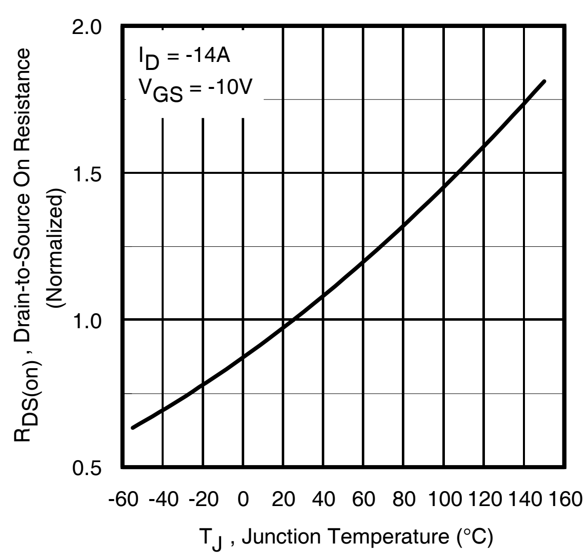


Fig 4. Normalized On-Resistance vs. Temperature

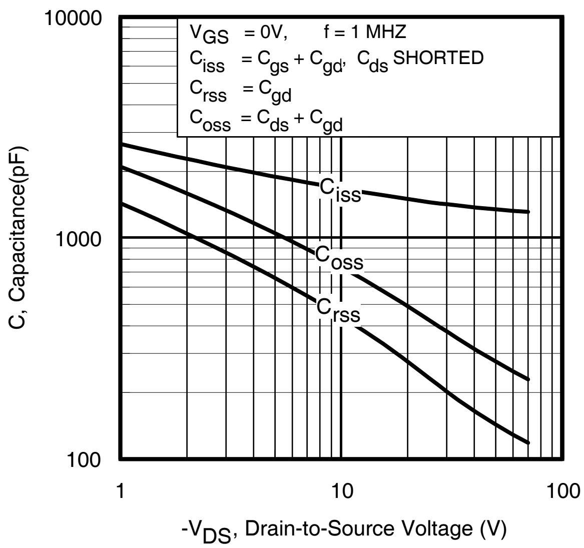


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

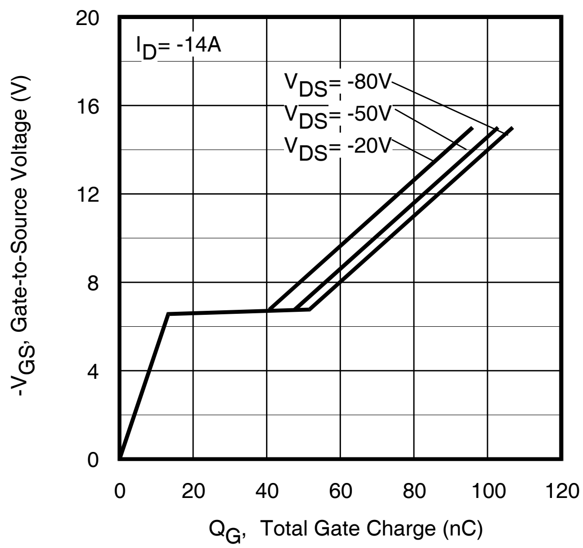


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

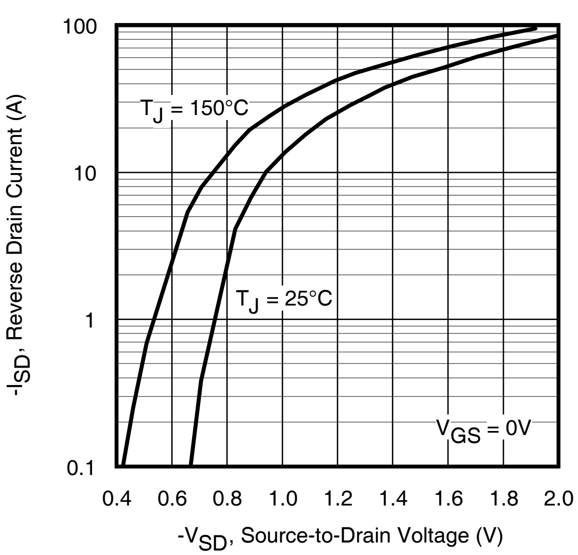


Fig 7. Typical Source-Drain Diode Forward Voltage

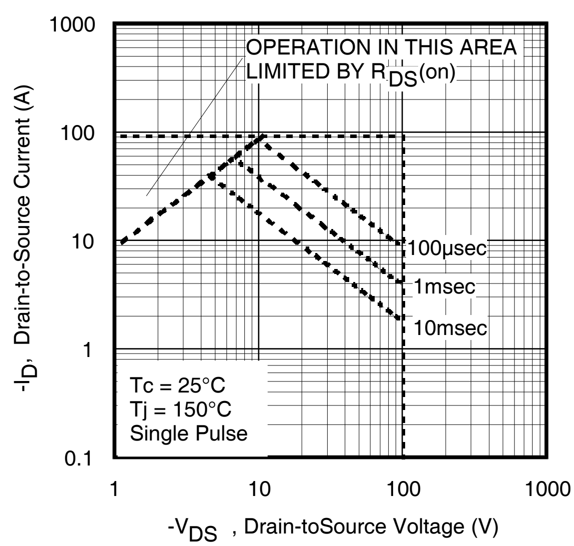


Fig 8. Maximum Safe Operating Area

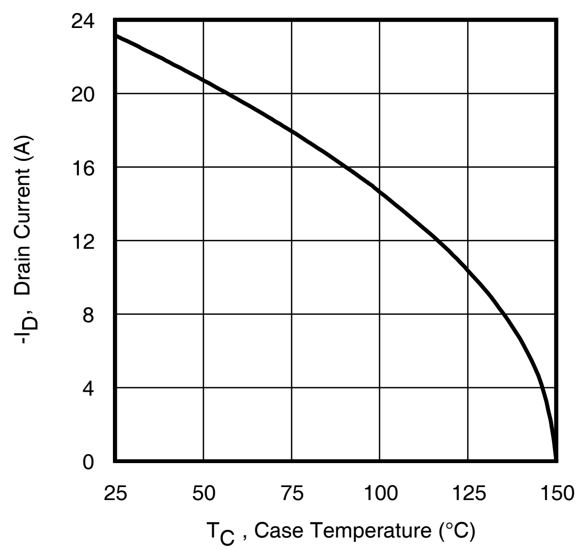


Fig 9. Maximum Drain Current vs. Case Temperature

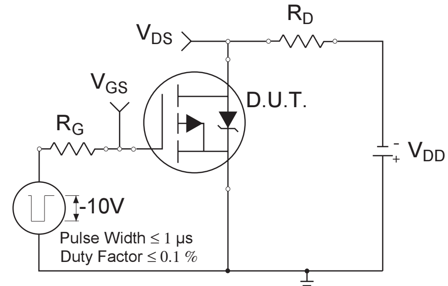


Fig 10a. Switching Time Test Circuit

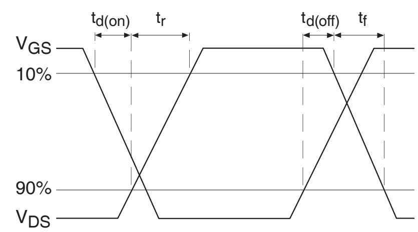
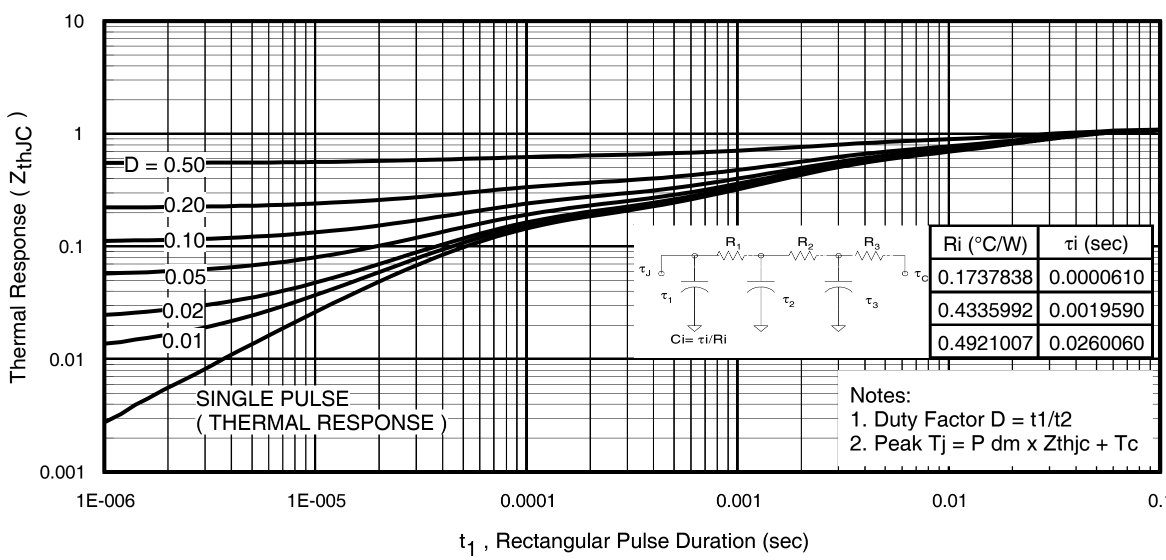


Fig 10b. Switching Time Waveforms



Ri (°C/W)	τi (sec)
0.1737838	0.0000610
0.4335992	0.0019590
0.4921007	0.0260060

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

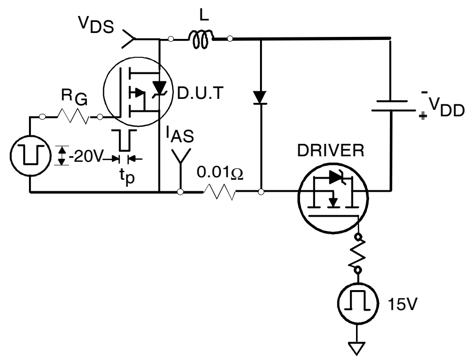


Fig 12a. Unclamped Inductive Test Circuit

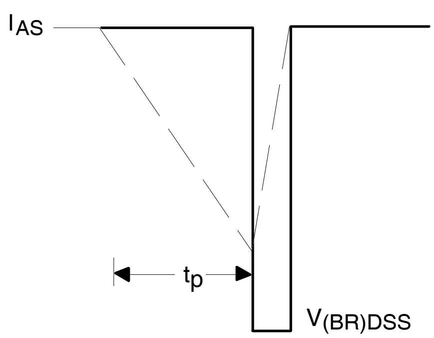


Fig 12b. Unclamped Inductive Waveforms

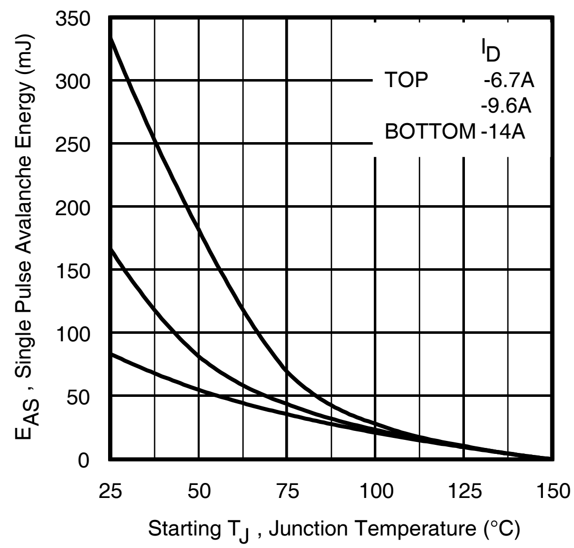


Fig 13. Maximum Avalanche Energy vs. Drain Current

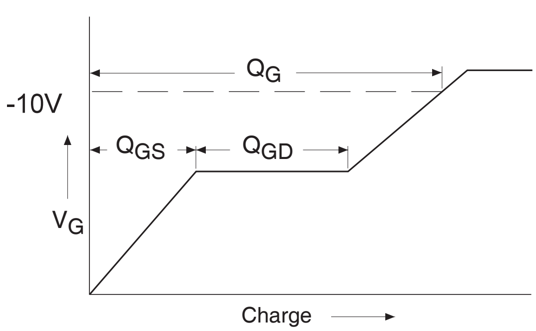


Fig 14a. Basic Gate Charge Waveform

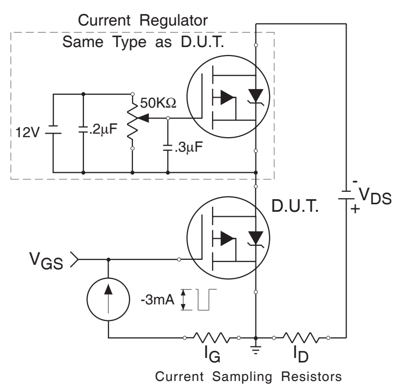
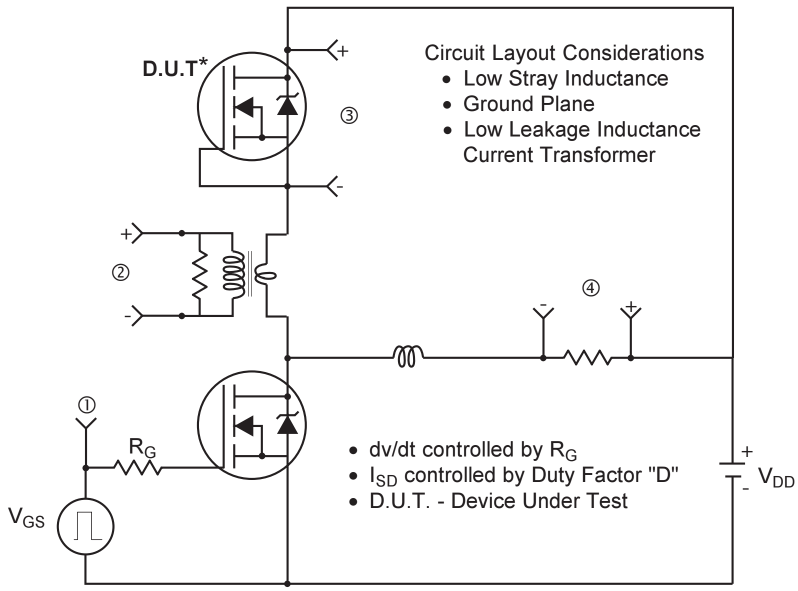
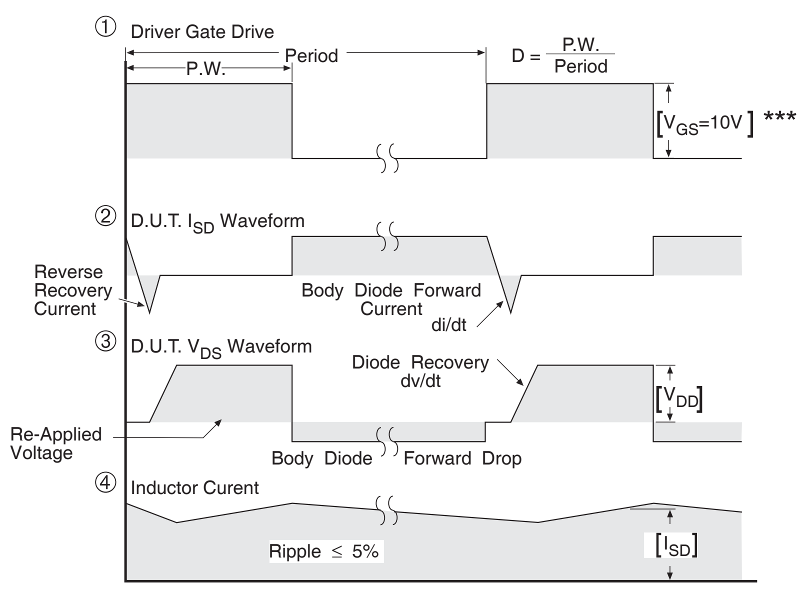


Fig 14b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

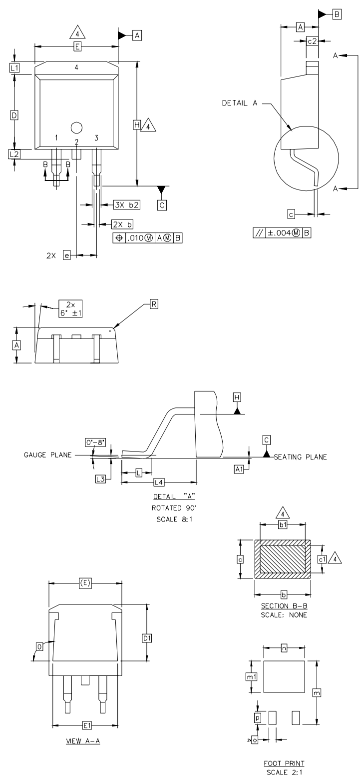


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 15. For P-Channel HEXFETS

D²Pak Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.78	.045	.070	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	4
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86		.270		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1		1.65		.065	
L2	1.27	1.78	.050	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
R	0.51	0.71	.020	.028	
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET
1.- GATE
2, 4.- DRAIN
3.- SOURCE

IGBTs, CoPACK
1.- GATE
2, 4.- COLLECTOR
3.- EMITTER

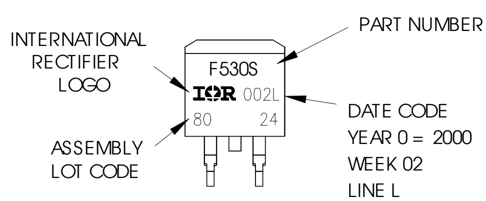
DIODES
1.- ANODE *
2, 4.- CATHODE
3.- ANODE

* PART DEPENDENT.

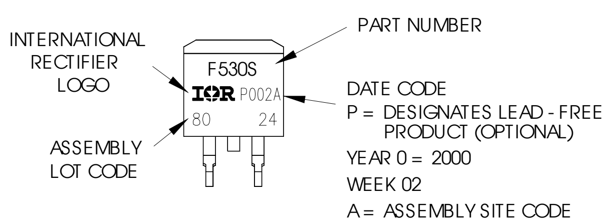
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead - Free"

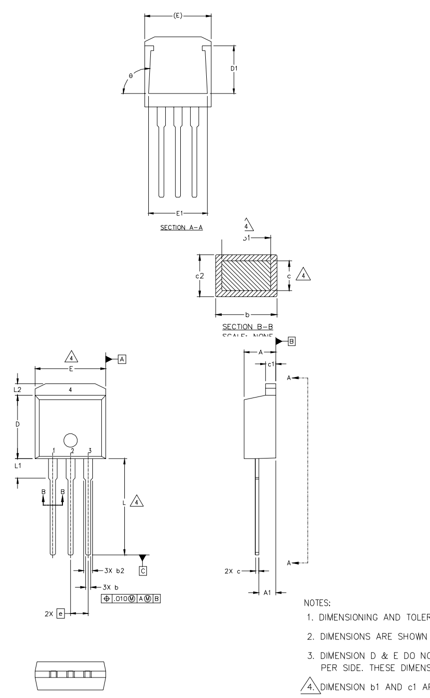


OR



TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
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	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
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b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET	IGBT
1.– GATE	1 - GATE
2.– DRAIN	2 - COLLECTOR
3.– SOURCE	3 - EMITTER
4.– DRAIN	

NOTES:

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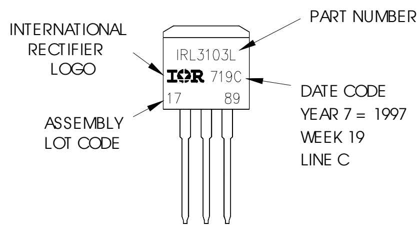
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

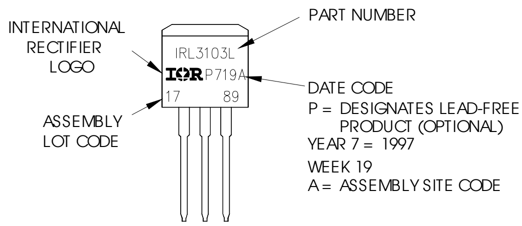
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



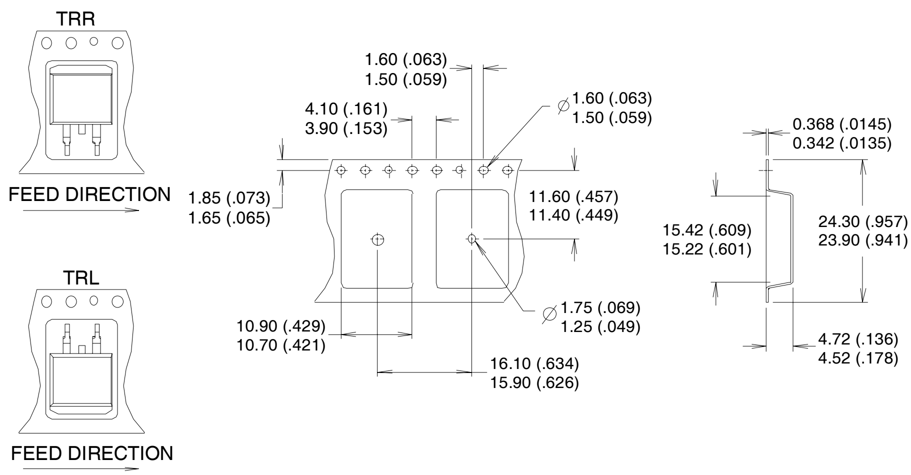
OR

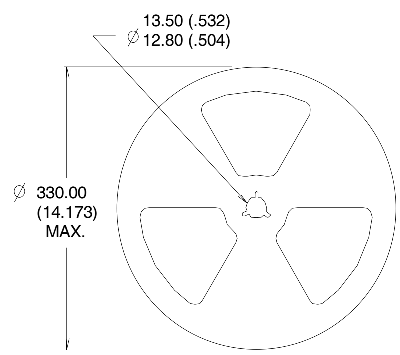


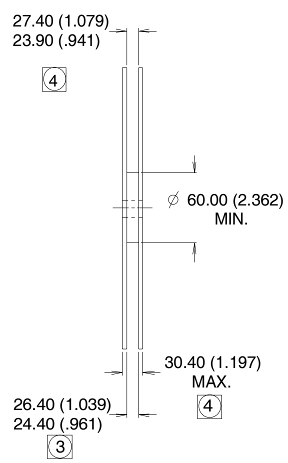
International
IOR Rectifier

D^2Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 09/05

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/