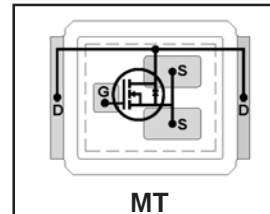


### DirectFET™ Power MOSFET ②

Typical values (unless otherwise specified)

V <sub>DSS</sub>	V <sub>GS</sub>	R <sub>DS(on)</sub>	R <sub>DS(on)</sub>
30V max	±20V max	1.3mΩ@10V	1.9mΩ@4.5V

- Ultra-low R<sub>DS(on)</sub>
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible ①
- Ultra-low Package Inductance
- Optimized for high speed switching or high current switch (Power Tool)
- Low Conduction and Switching Losses
- Compatible with existing Surface Mount Techniques ①



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST		MQ	MX	<b>MT</b>	MP			
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### Description

The IRF8301MPbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve very low on-state resistance in a package that has the footprint of an SO-8 or a PQFN 5x6mm and only 0.7mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF8301MPbF balances both low resistance and low charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced total losses and very high current carrying capability make this product ideal for power tools.

### Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF8301MPbF	DirectFET MT	Tape and Reel	4800	IRF8301MTRPbF

### Absolute Maximum Ratings

	Parameter	Max.	Units
V <sub>GS</sub>	Gate-to-Source Voltage	±20	
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V ③	34	A
I <sub>D</sub> @ T <sub>A</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V ③	27	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V ④	192	
I <sub>DM</sub>	Pulsed Drain Current ⑤	250	
E <sub>AS</sub>	Single Pulse Avalanche Energy ⑥	260	mJ
I <sub>AR</sub>	Avalanche Current ⑤	25	A

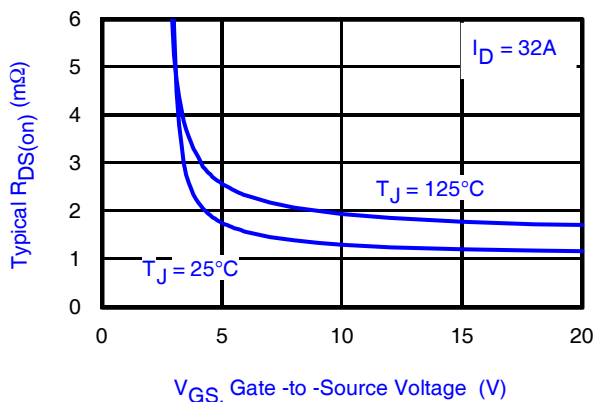


Fig 1. Typical On-Resistance vs. Gate Voltage

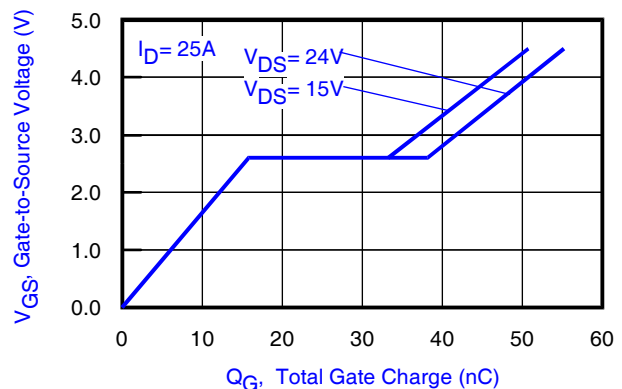


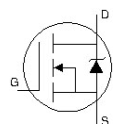
Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	21	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	1.3	1.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 32A ⑦
		—	1.9	2.4		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 25A ⑦
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.7	2.35	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-6.0	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	150	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 25A
Q <sub>g</sub>	Total Gate Charge	—	51	77	nC	V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 25A See Fig. 15
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	12	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	5.4	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	16	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	18	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	21	—		
Q <sub>oss</sub>	Output Charge	—	28	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	1.0	3.0	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	20	—	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V ⑦ I <sub>D</sub> = 25A R <sub>G</sub> = 1.8Ω See Fig. 17
t <sub>r</sub>	Rise Time	—	30	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	25	—		
t <sub>f</sub>	Fall Time	—	17	—		
C <sub>iss</sub>	Input Capacitance	—	6140	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 15V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1270	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	590	—		

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	110	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ⑤	—	—	250		
V <sub>SD</sub>	Diode Forward Voltage	—	0.77	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 25A, V <sub>GS</sub> = 0V ⑦
t <sub>rr</sub>	Reverse Recovery Time	—	27	41	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 25A
Q <sub>rr</sub>	Reverse Recovery Charge	—	45	68	nC	di/dt = 500A/μs ⑦


**Notes:**

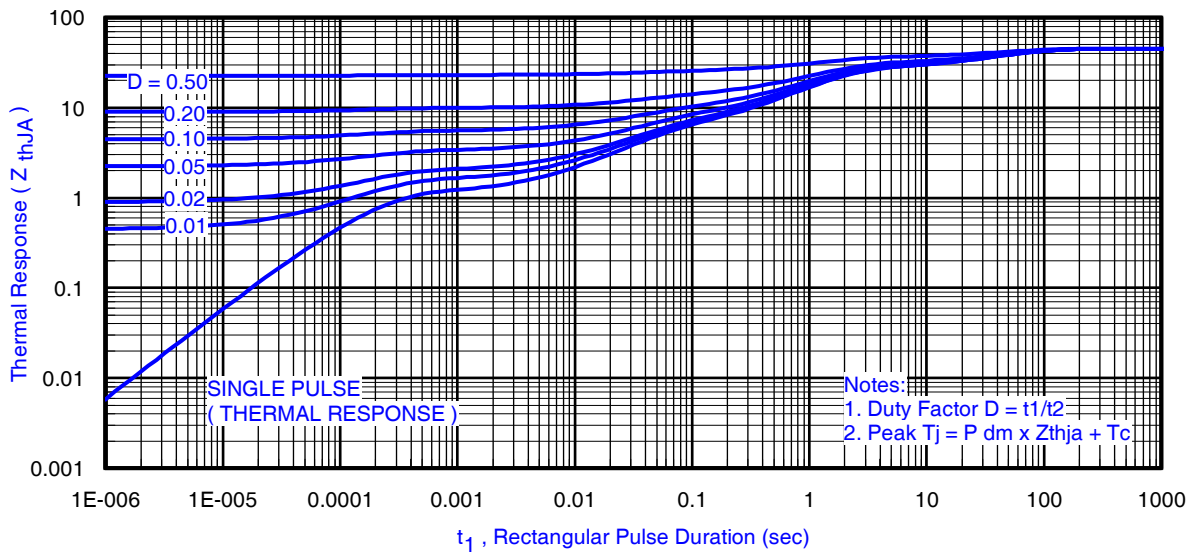
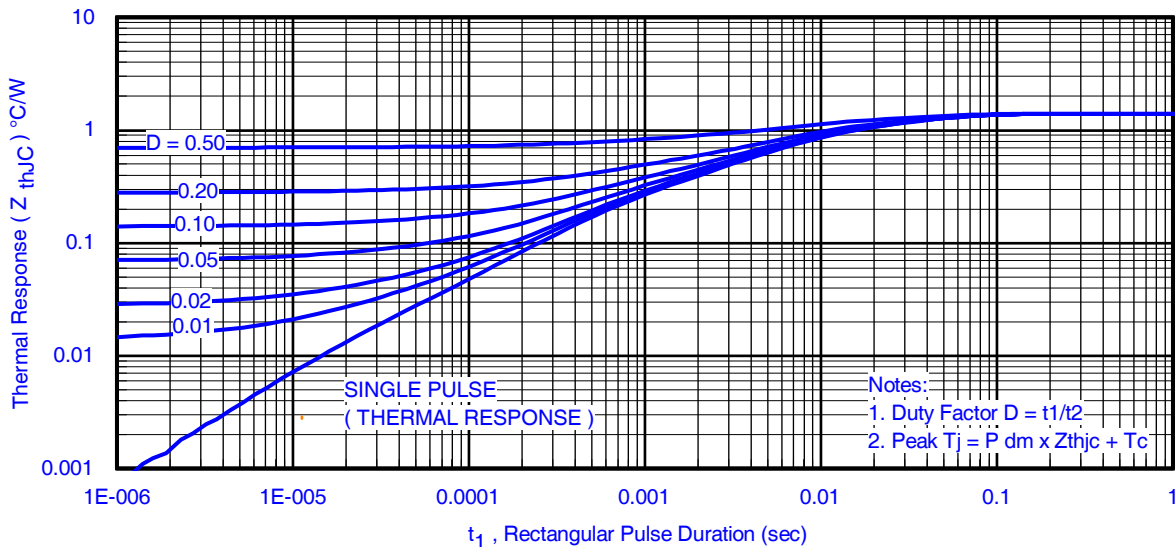
- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④ T<sub>C</sub> measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting T<sub>J</sub> = 25°C, L = 0.82mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 25A.
- ⑦ Pulse width ≤ 400μs; duty cycle ≤ 2%.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	2.8	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③	1.8	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	89	
$T_P$	Peak Soldering Temperature	270	°C
$T_J$	Operating Junction and	-40 to + 150	
$T_{STG}$	Storage Temperature Range		

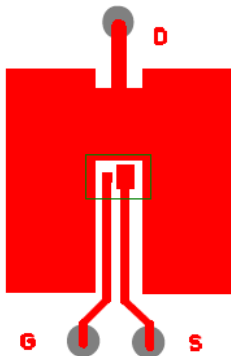
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③⑩	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑧⑩	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨⑩	20	—	
$R_{\theta JC}$	Junction-to-Case ④⑩	—	1.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.022		W/°C

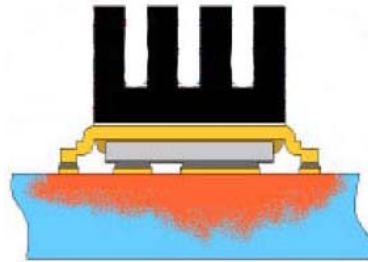

**Fig 3.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ③

**Fig 4.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Notes:**

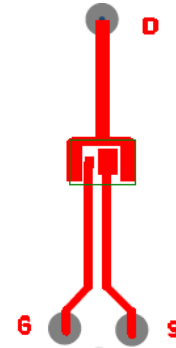
- ③ Used double sided cooling , mounting pad with large heatsink.
- ④ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑩  $R_{\theta}$  is measured at  $T_J$  of approximately 90°C.



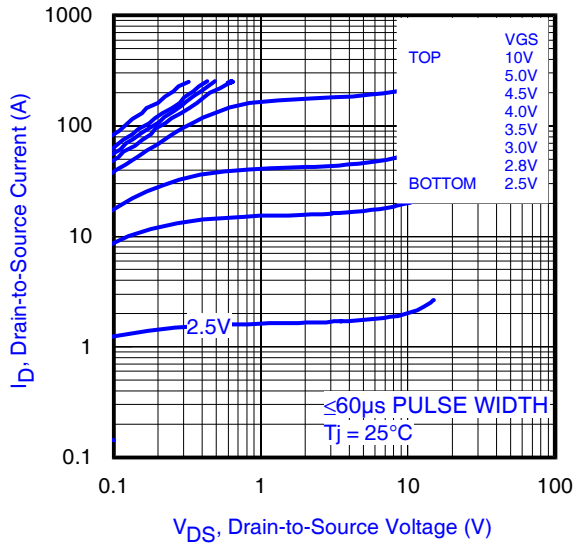
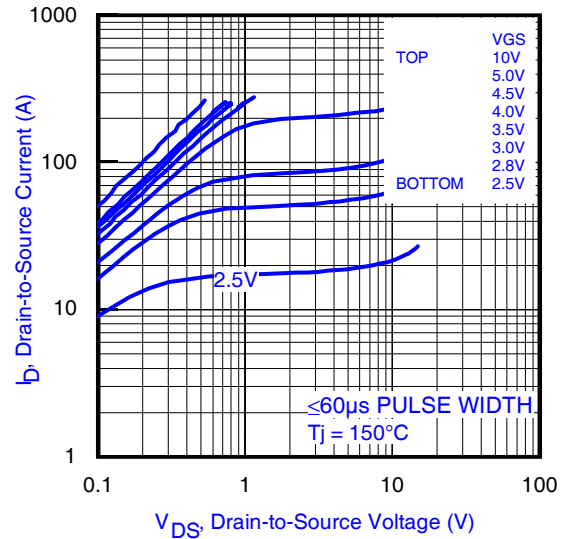
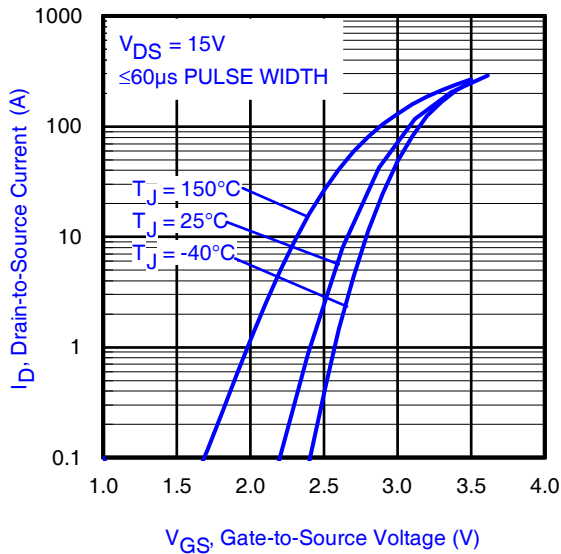
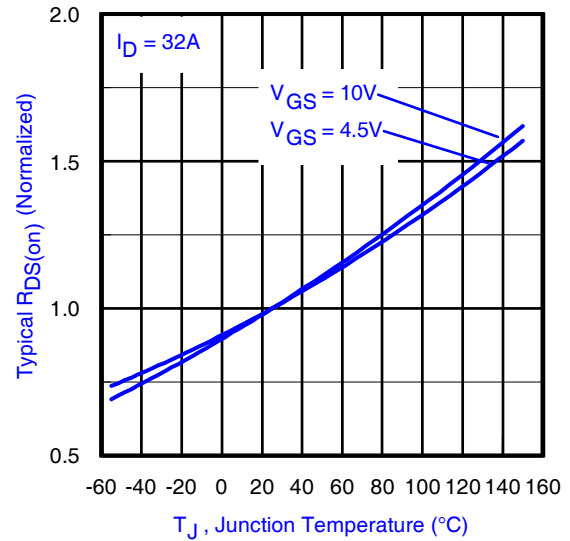
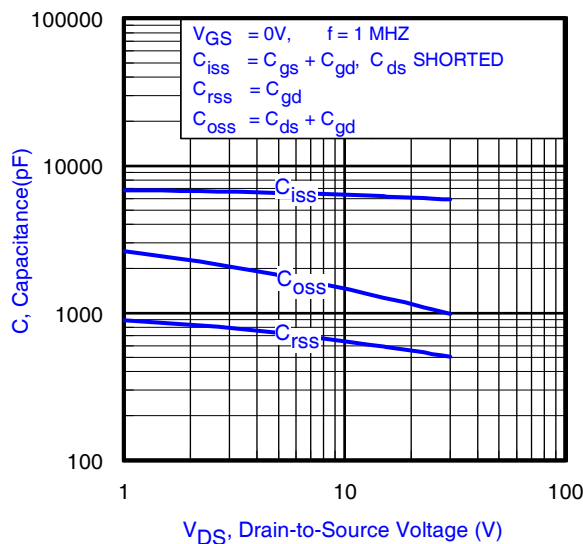
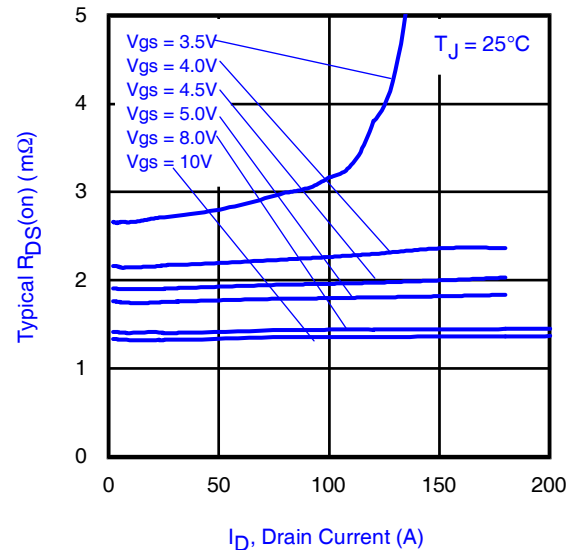
③ Surface mounted on 1 in. square Cu (still air).

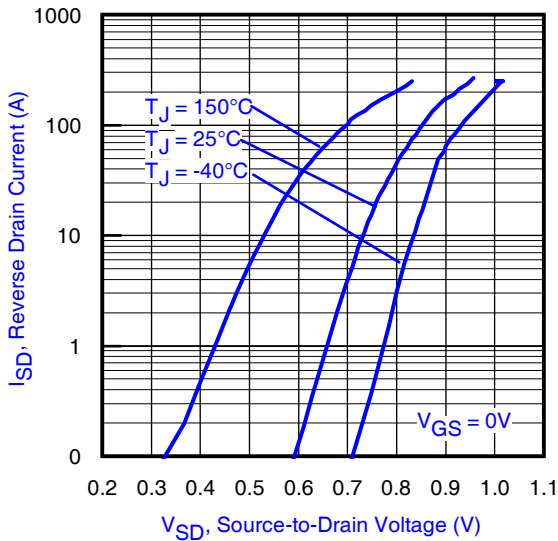
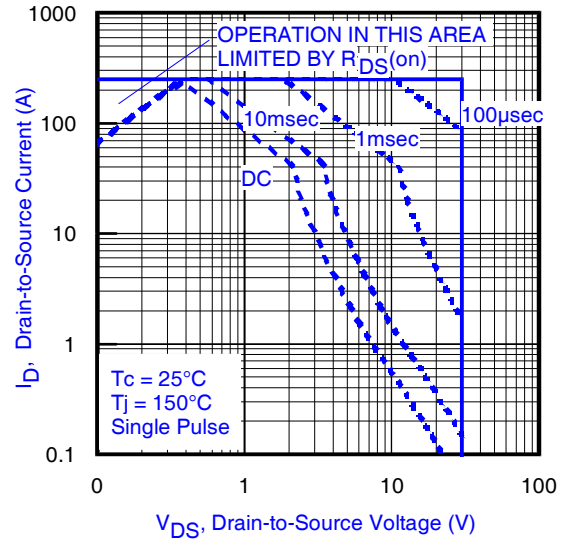
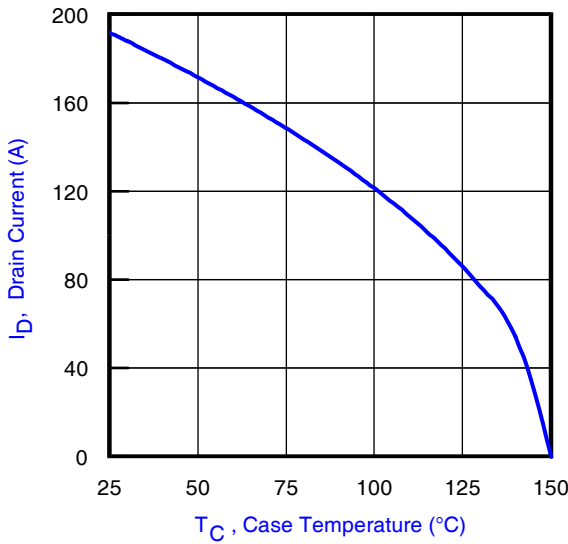
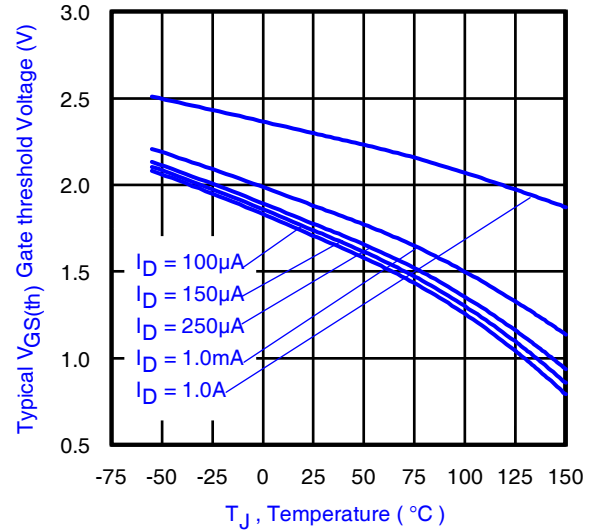
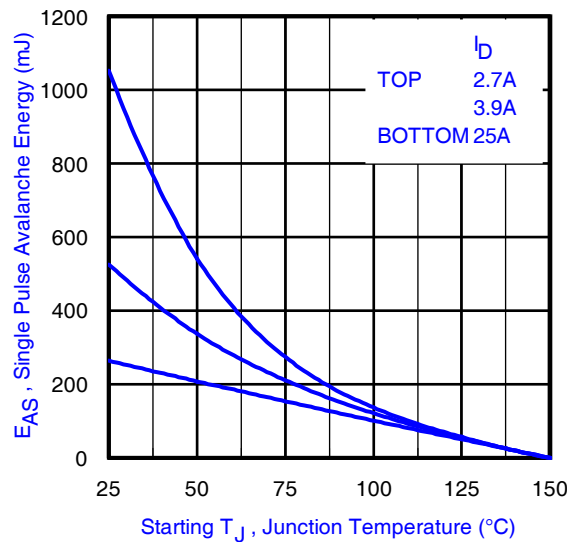


④ Mounted to a PCB with small clip heatsink (still air)



⑤ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)


**Fig 5.** Typical Output Characteristics

**Fig 6.** Typical Output Characteristics

**Fig 7.** Typical Transfer Characteristics

**Fig 8.** Normalized On-Resistance vs. Temperature

**Fig 9.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 10.** Typical On-Resistance vs. Drain Current and Gate Voltage


**Fig 11.** Typical Source-Drain Diode Forward Voltage

**Fig 12.** Maximum Safe Operating Area

**Fig 13.** Maximum Drain Current vs. Case Temperature

**Fig 14.** Typical Threshold Voltage vs. Junction Temperature

**Fig 15.** Maximum Avalanche Energy vs. Drain Current

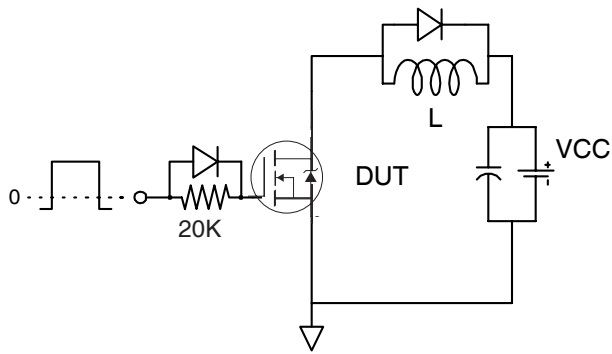


Fig 16a. Gate Charge Test Circuit

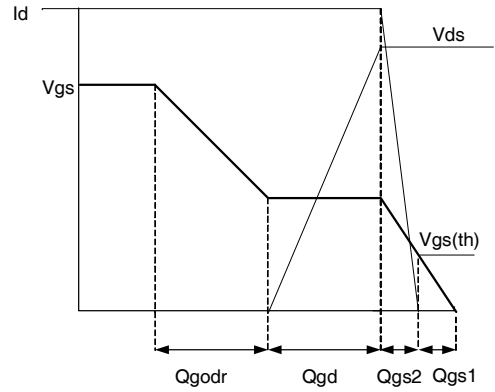


Fig 16b. Gate Charge Waveform

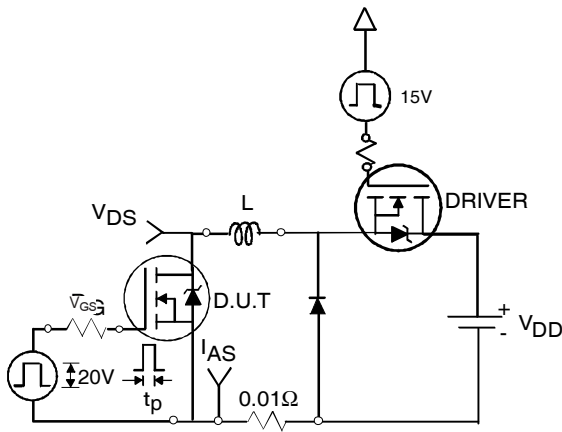


Fig 17a. Unclamped Inductive Test Circuit

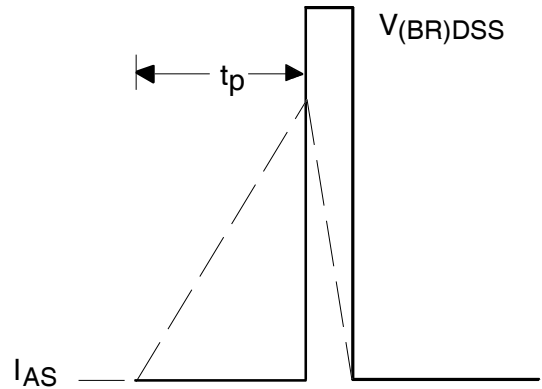


Fig 17b. Unclamped Inductive Waveforms

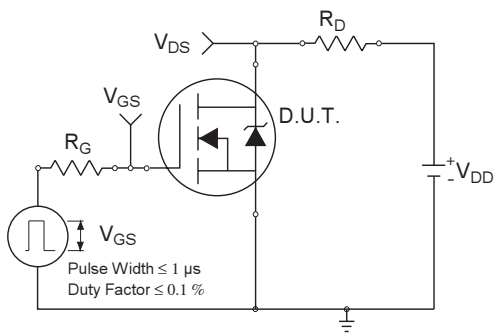


Fig 18a. Switching Time Test Circuit

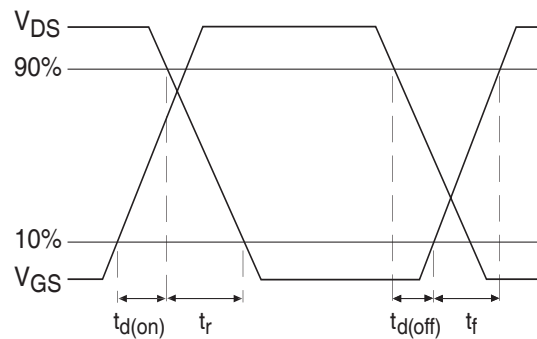
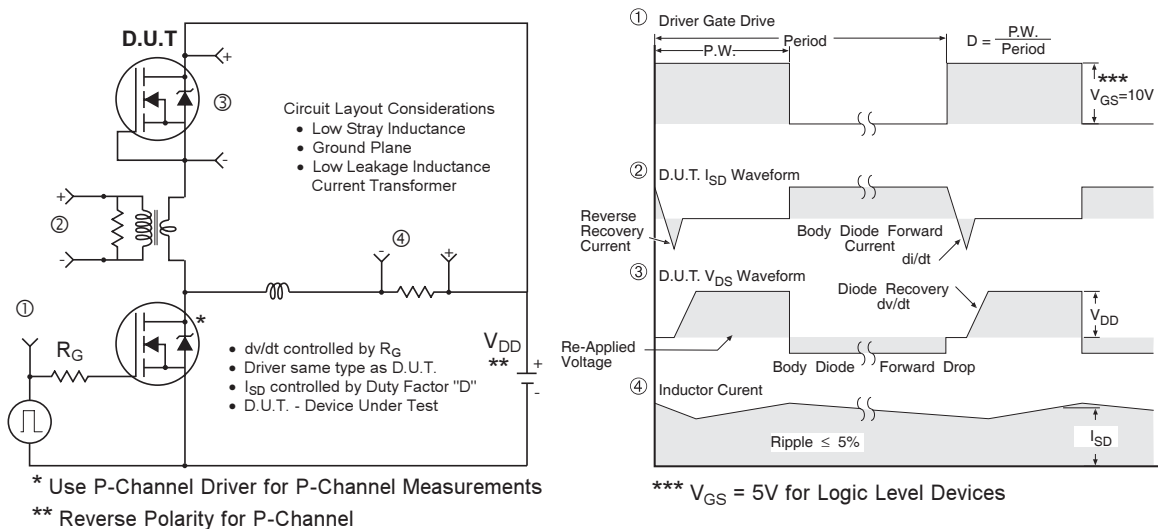


Fig 18b. Switching Time Waveforms

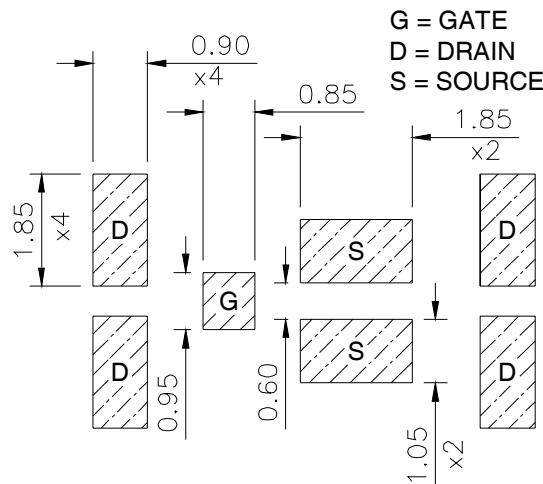
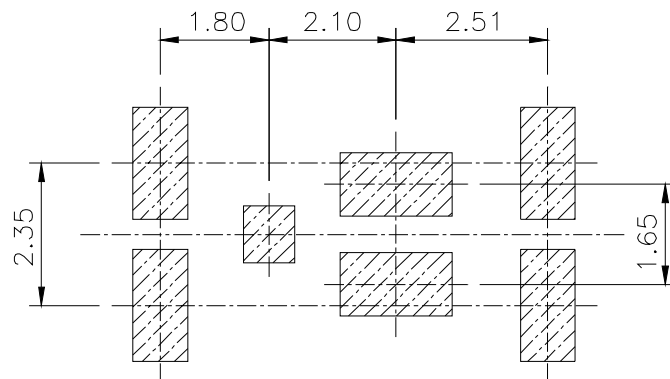


**Fig 19. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs**

### DirectFET™ Board Footprint, MT Outline (Medium Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.

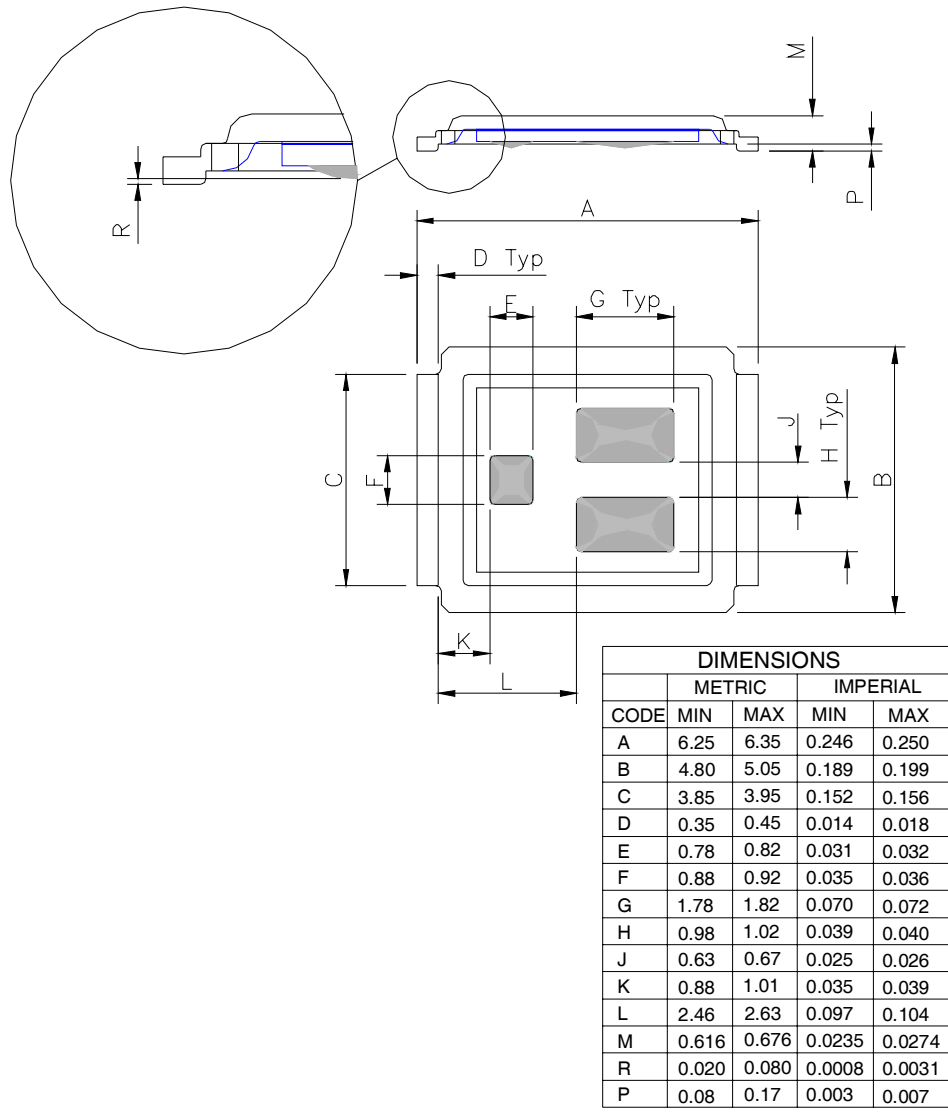


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

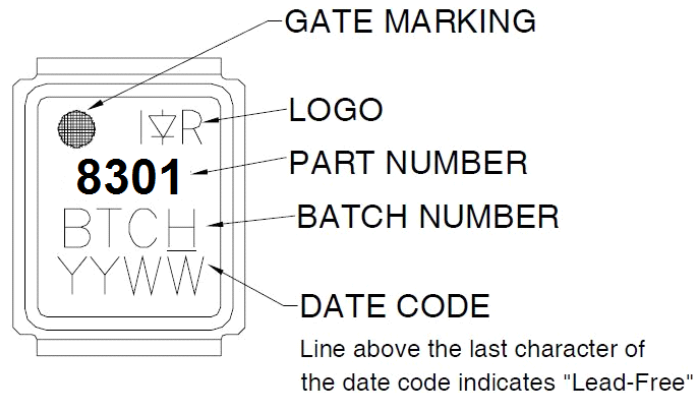


**DirectFET™ Outline Dimension, MT Outline (Medium Size Can, T-Designation).**

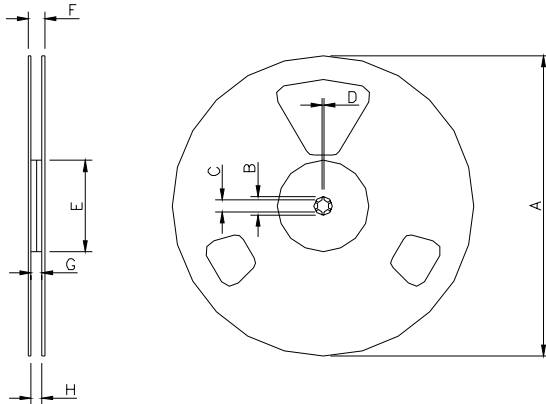
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



**DirectFET™ Part Marking**

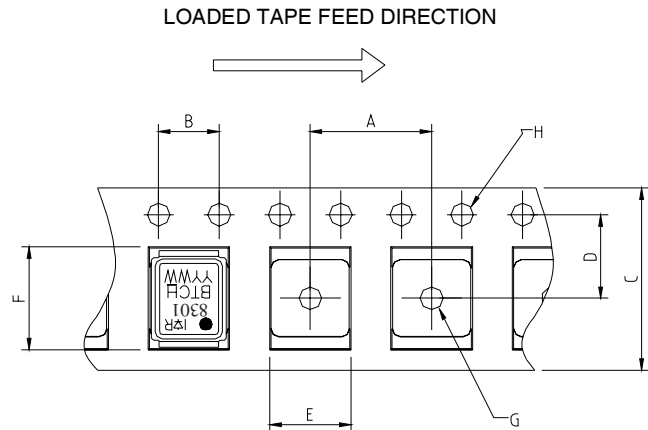


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**DirectFET™ Tape & Reel Dimension (Showing component orientation).**


NOTE: Controlling dimensions in mm  
Std reel quantity is 4800 parts. (ordered as IRF8301MTRPbF ).

CODE	REEL DIMENSIONS			
	STANDARD OPTION (QTY 4000)			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Revision History**

Date	Comments
09/05/2013	• Added the StrongIRFET logo on the top of the part number, on page 1.

## **IMPORTANT NOTICE**

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