

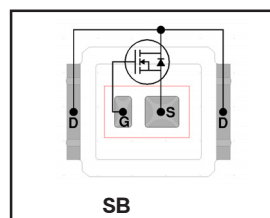
# IRF7665S2TRPbF

## IRF7665S2TR1PbF

### Features

- Key parameters optimized for Class-D audio amplifier applications
- Low  $R_{DS(on)}$  for improved efficiency
- Low  $Q_g$  for better THD and improved efficiency
- Low  $Q_{rr}$  for better THD and lower EMI
- Low package stray inductance for reduced ringing and lower EMI
- Can deliver up to 100W per channel into  $8\Omega$  with no heatsink ⑩
- Dual sided cooling compatible
- Compatible with existing surface mount technologies
- RoHS compliant containing no lead or bromide
- Lead-Free (Qualified up to 260°C Reflow)
- Industrial Qualified

Key Parameters		
$V_{DS}$	100	V
$R_{DS(on)}$ typ. @ $V_{GS} = 10V$	51	m $\Omega$
$Q_g$ typ.	8.3	nC
$R_{G(int)}$ typ.	3.5	$\Omega$



Applicable DirectFET Outline and Substrate Outline (see p. 6, 7 for details)

SB	SC		M2	M4		L4	L6	L8	
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### Description

This Digital Audio MOSFET is specifically designed for Class-D audio amplifier applications. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, gate charge, body-diode reverse recovery and internal gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD, and EMI.

The IRF7665S2TR/TR1PbF device utilizes DirectFET™ packaging technology. DirectFET™ packaging technology offers lower parasitic inductance and resistance when compared to conventional wirebonded SOIC packaging. Lower inductance improves EMI performance by reducing the voltage ringing that accompanies fast current transients. The DirectFET™ package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing method and processes. The DirectFET™ package also allows dual sided cooling to maximize thermal transfer in power systems, improving thermal resistance and power dissipation. These features combine to make this MOSFET a highly efficient, robust and reliable device for Class-D audio amplifier applications.

### Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	14.4	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	10.2	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	4.1	
$I_{DM}$	Pulsed Drain Current ①	58	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	30	W
$P_D @ T_C = 100^\circ C$	Power Dissipation ②	15	
$P_D @ T_A = 25^\circ C$	Power Dissipation ③	2.4	
	Linear Derating Factor ③	0.2	W/°C
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ④	—	63	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦	20	—	
$R_{\theta J-Can}$	Junction-to-Can ⑧ ⑨	—	5.0	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.4	—	

Notes ① through ⑩ are on page 2

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	51	62	m $\Omega$	$V_{GS} = 10V, I_D = 8.9A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	4.0	5.0	V	$V_{DS} = V_{GS}, I_D = 25\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$R_{G(int)}$	Internal Gate Resistance	—	3.5	5.0	$\Omega$	

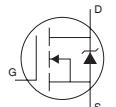
## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	8.8	—	—	S	$V_{DS} = 25V, I_D = 8.9A$
$Q_g$	Total Gate Charge	—	8.3	13	nC	$V_{DS} = 50V$ $V_{GS} = 10V$ $I_D = 8.9A$ See Fig. 6 and 17
$Q_{gs1}$	Pre-V <sub>th</sub> Gate-to-Source Charge	—	1.9	—		
$Q_{gs2}$	Post-V <sub>th</sub> Gate-to-Source Charge	—	0.77	—		
$Q_{gd}$	Gate-to-Drain Charge	—	3.2	—		
$Q_{godr}$	Gate Charge Overdrive	—	2.4	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	4.0	—		
$t_{d(on)}$	Turn-On Delay Time	—	3.8	—	ns	$V_{DD} = 50V$ $I_D = 8.9A$ $R_G = 6.8\Omega$ $V_{GS} = 10V$ ④
$t_r$	Rise Time	—	6.4	—		
$t_{d(off)}$	Turn-Off Delay Time	—	7.1	—		
$t_f$	Fall Time	—	3.6	—		
$C_{iss}$	Input Capacitance	—	515	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 80V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 0V$ to $80V$ ⑤
$C_{oss}$	Output Capacitance	—	112	—		
$C_{rss}$	Reverse Transfer Capacitance	—	30	—		
$C_{oss}$	Output Capacitance	—	533	—		
$C_{oss}$	Output Capacitance	—	67	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	115	—		

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	37	mJ
$I_{AR}$	Avalanche Current ①	—	8.9	A

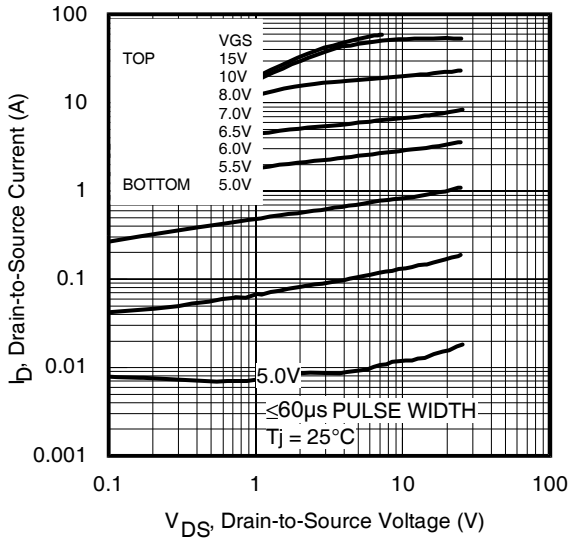
## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	14.4	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	58		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 8.9A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	33	—	ns	$T_J = 25^\circ\text{C}, I_F = 8.9A, V_{DD} = 25V$
$Q_{rr}$	Reverse Recovery Charge	—	38	—	nC	$di/dt = 100A/\mu s$ ④

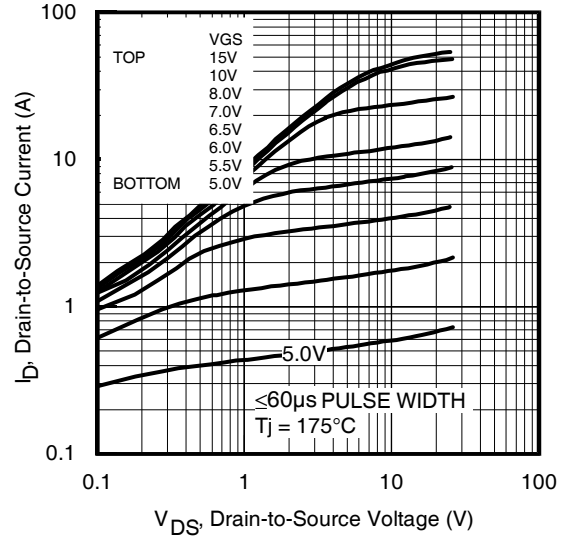
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.944\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 8.9A$ .
- ③ Surface mounted on 1 in. square Cu board.
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

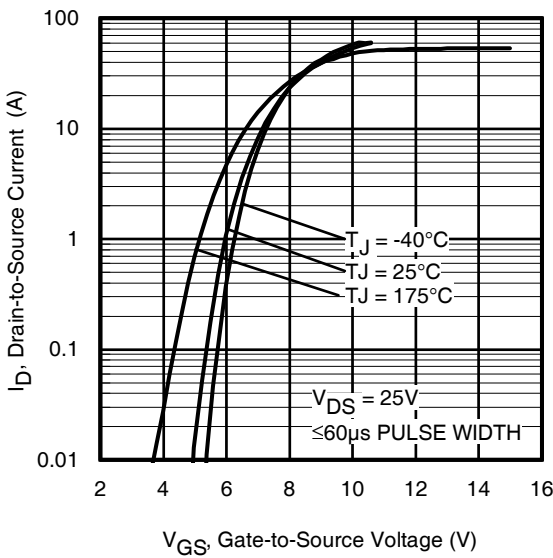
- ⑥ Used double sided cooling, mounting pad.
- ⑦ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑧  $T_C$  measured with thermal couple mounted to top (Drain) of part.
- ⑨  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑩ Based on testing done using a typical device & evaluation board at  $V_{bus} = \pm 45V$ ,  $f_{SW} = 400\text{kHz}$ , and  $T_A = 25^\circ\text{C}$ . The delta case temperature  $\Delta T_C$  is  $55^\circ\text{C}$ .



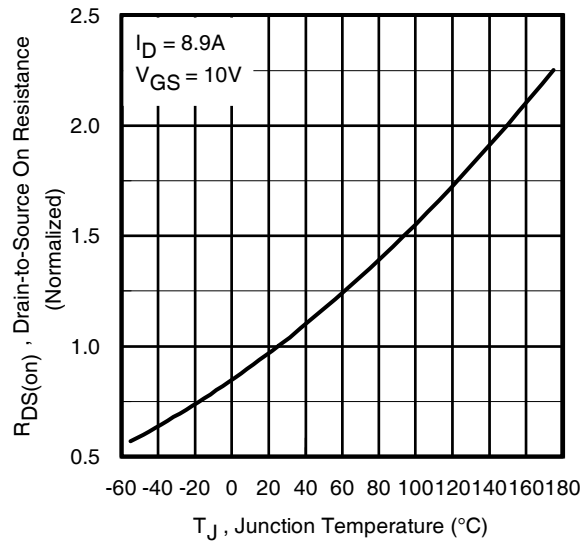
**Fig 1.** Typical Output Characteristics



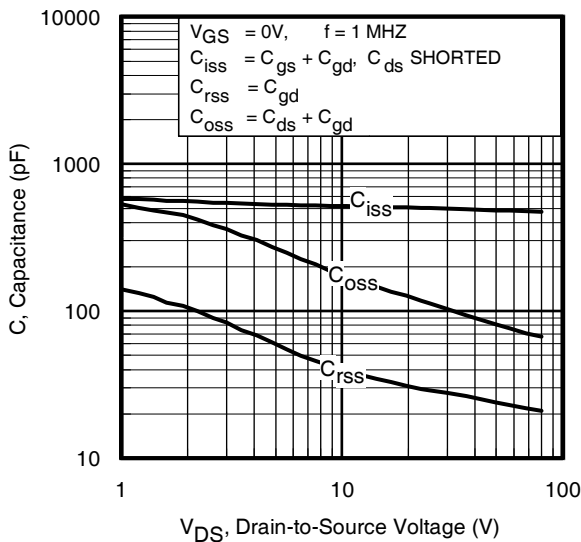
**Fig 2.** Typical Output Characteristics



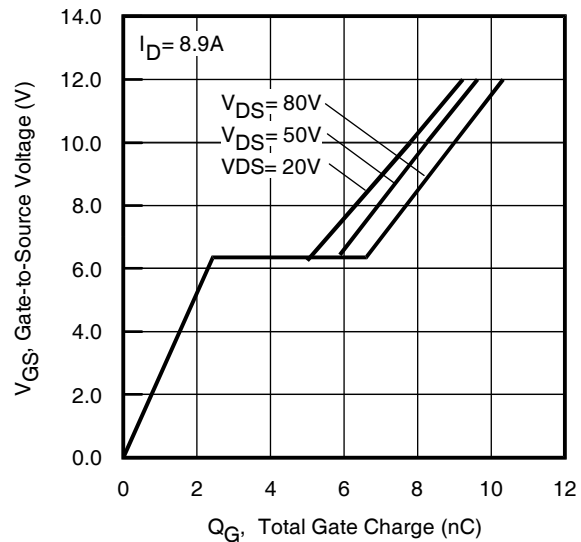
**Fig 3.** Typical Transfer Characteristics



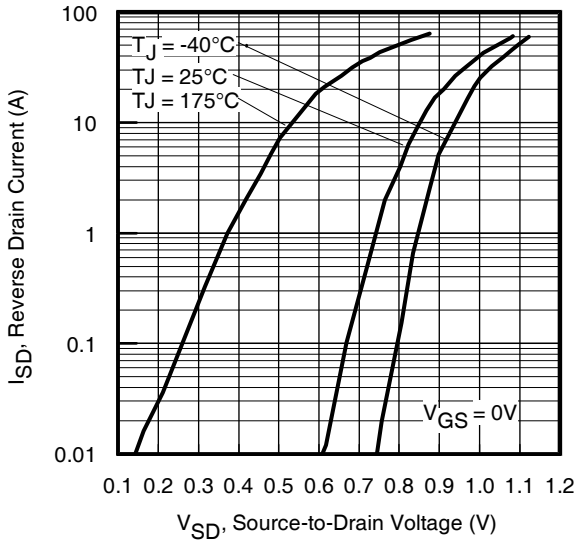
**Fig 4.** Normalized On-Resistance vs. Temperature



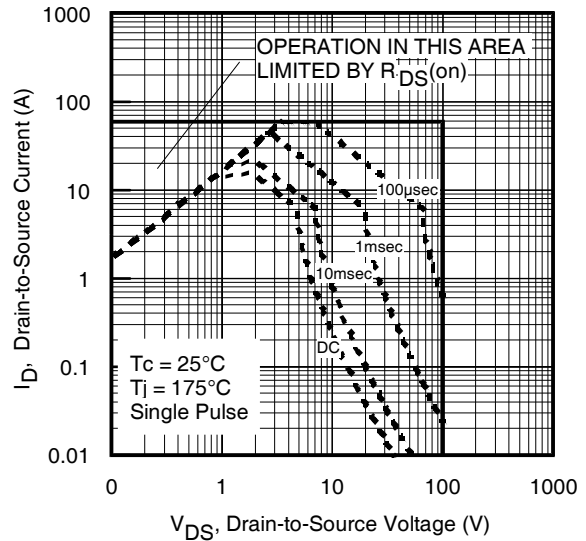
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



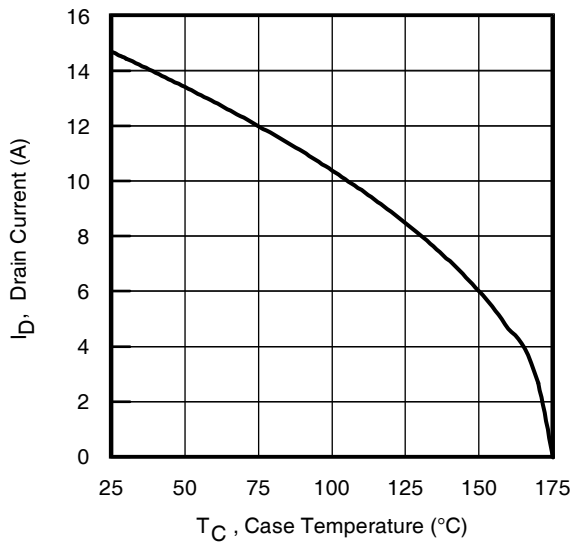
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



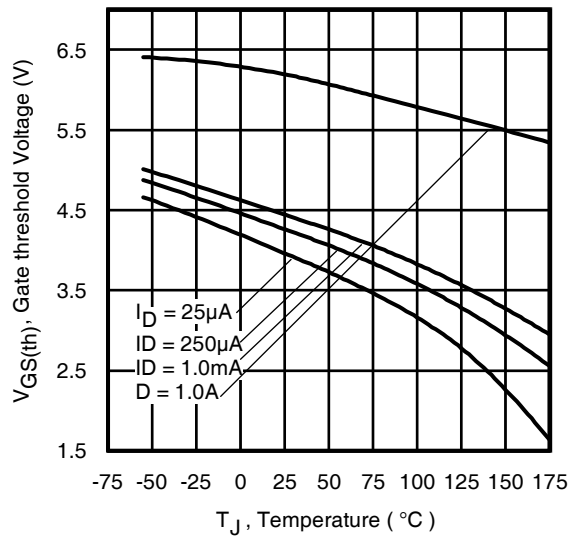
**Fig 7.** Typical Source-Drain Diode Forward Voltage



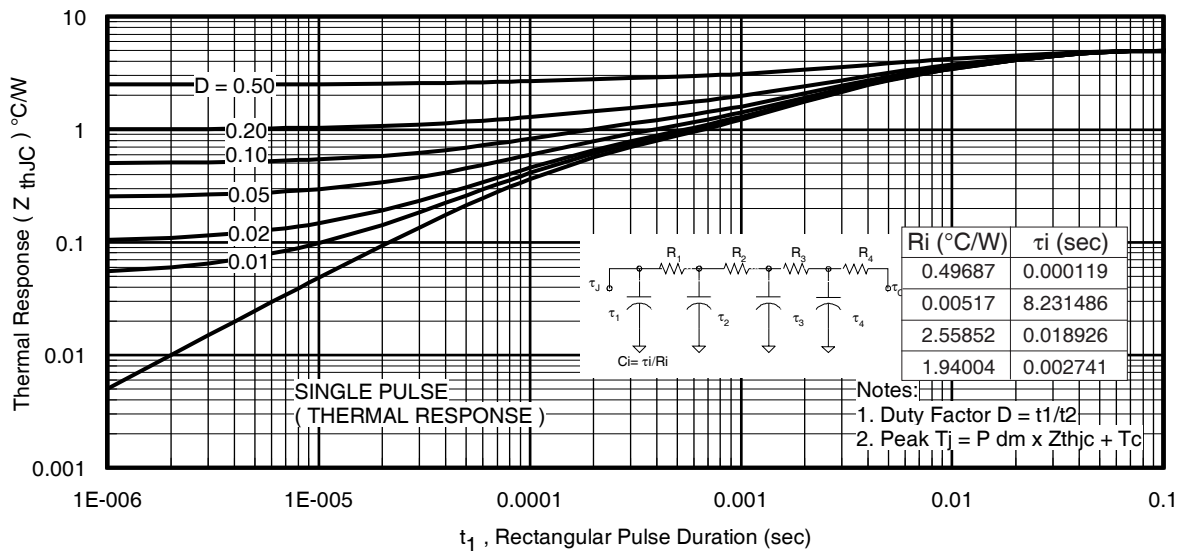
**Fig 8.** Maximum Safe Operating Area



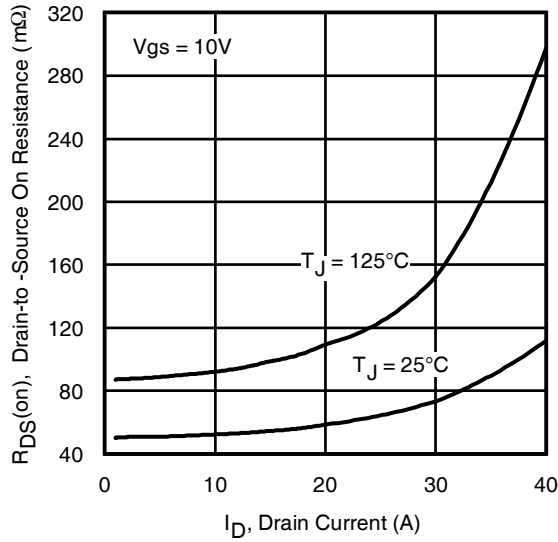
**Fig 9.** Maximum Drain Current vs. Case Temperature



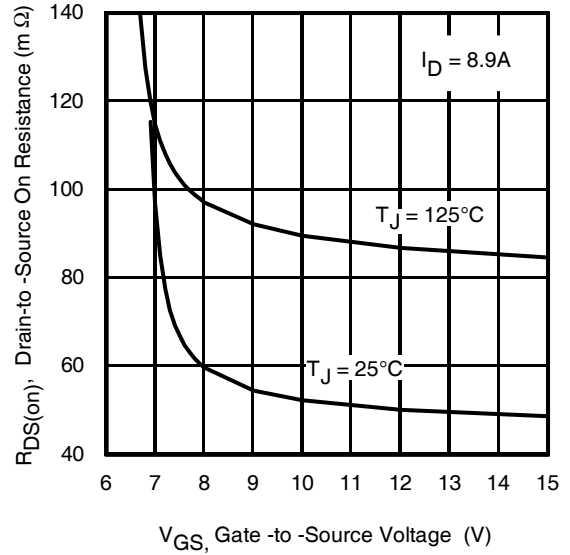
**Fig 10.** Threshold Voltage vs. Temperature



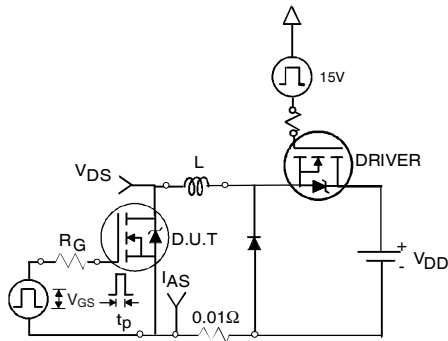
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ©



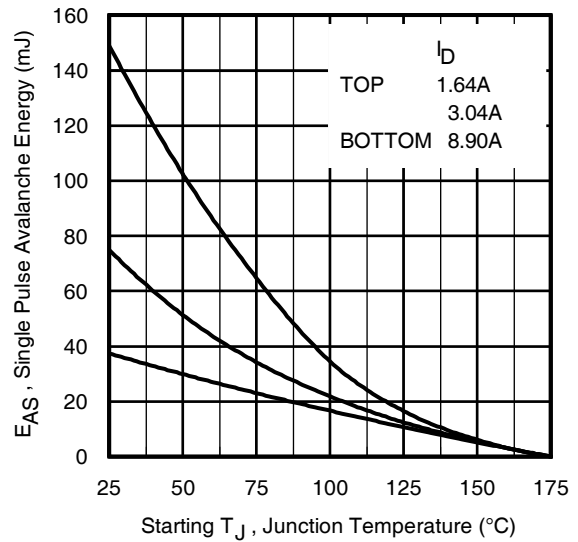
**Fig 12.** On-Resistance vs. Gate Voltage



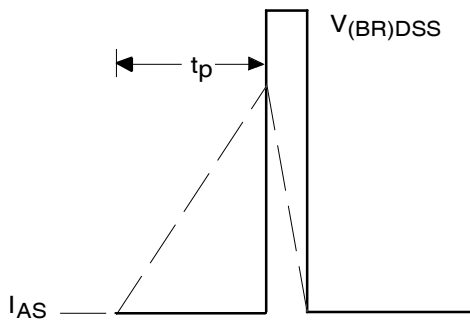
**Fig 13.** On-Resistance vs. Drain Current



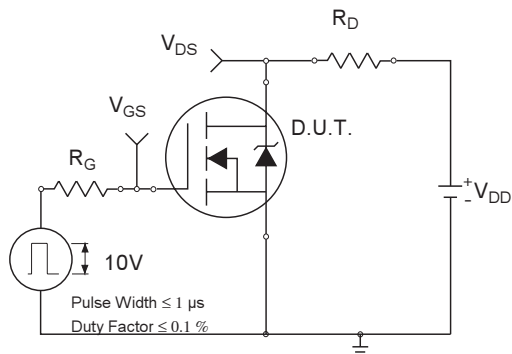
**Fig 15a.** Unclamped Inductive Test Circuit



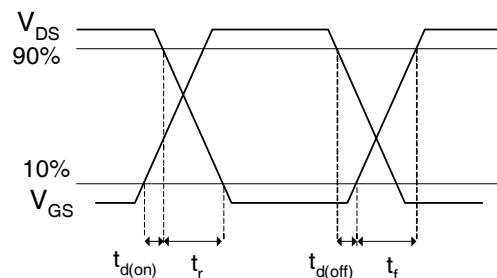
**Fig 14.** Maximum Avalanche Energy vs. Drain Current



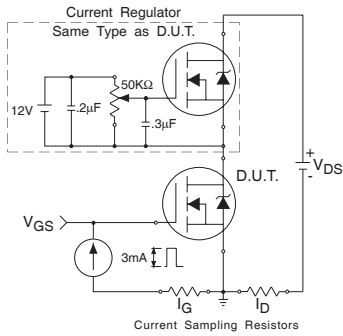
**Fig 15b.** Unclamped Inductive Waveforms



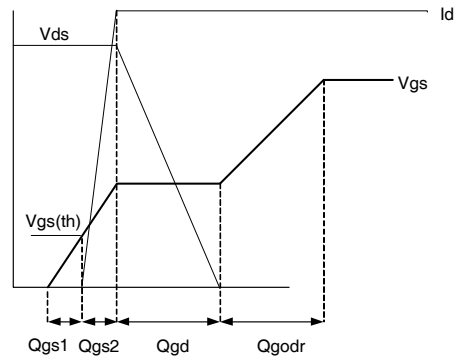
**Fig 16a.** Switching Time Test Circuit  
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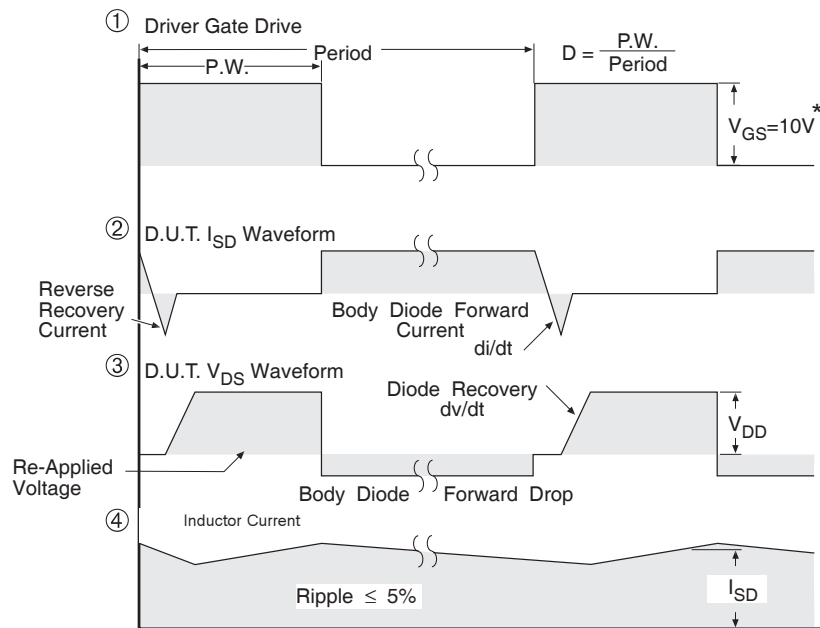
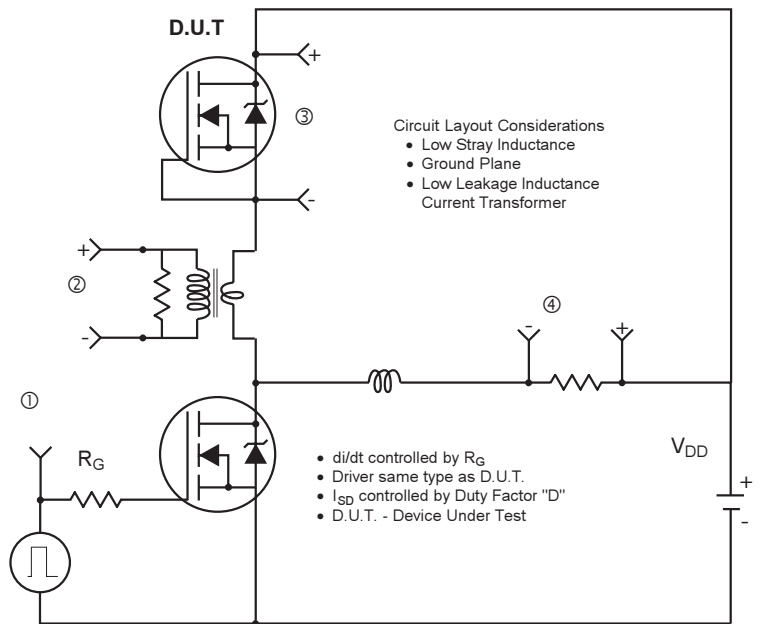
**Fig 16b.** Switching Time Waveforms



**Fig 17a.** Gate Charge Test Circuit



**Fig 17b.** Gate Charge Waveform

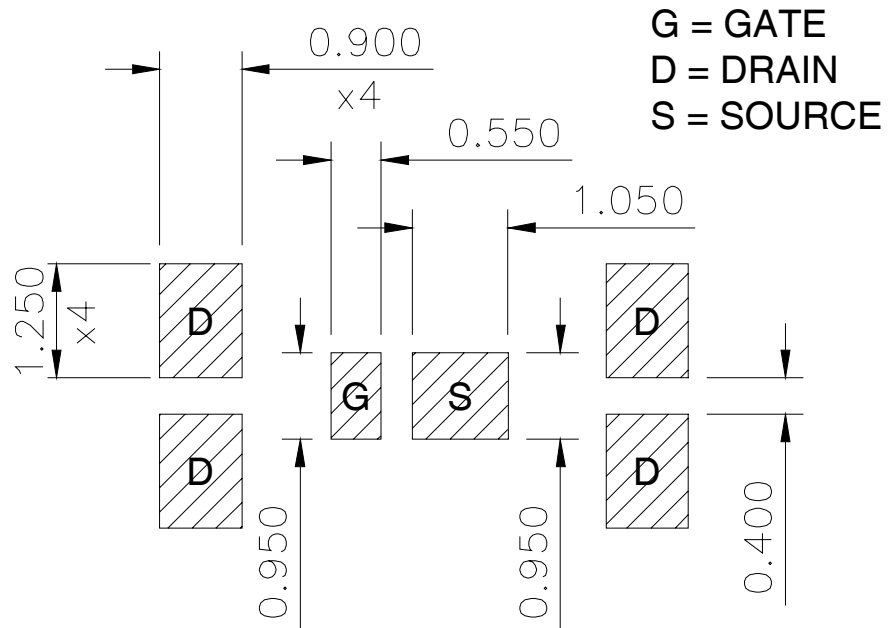
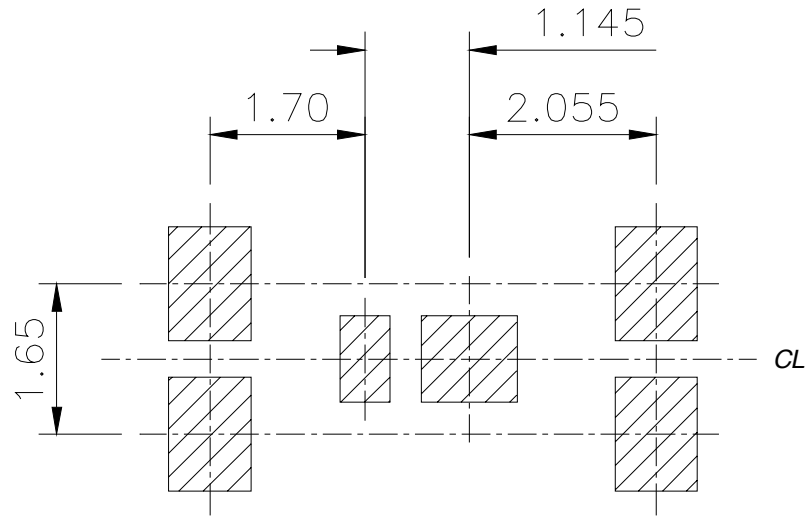


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 18.** Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

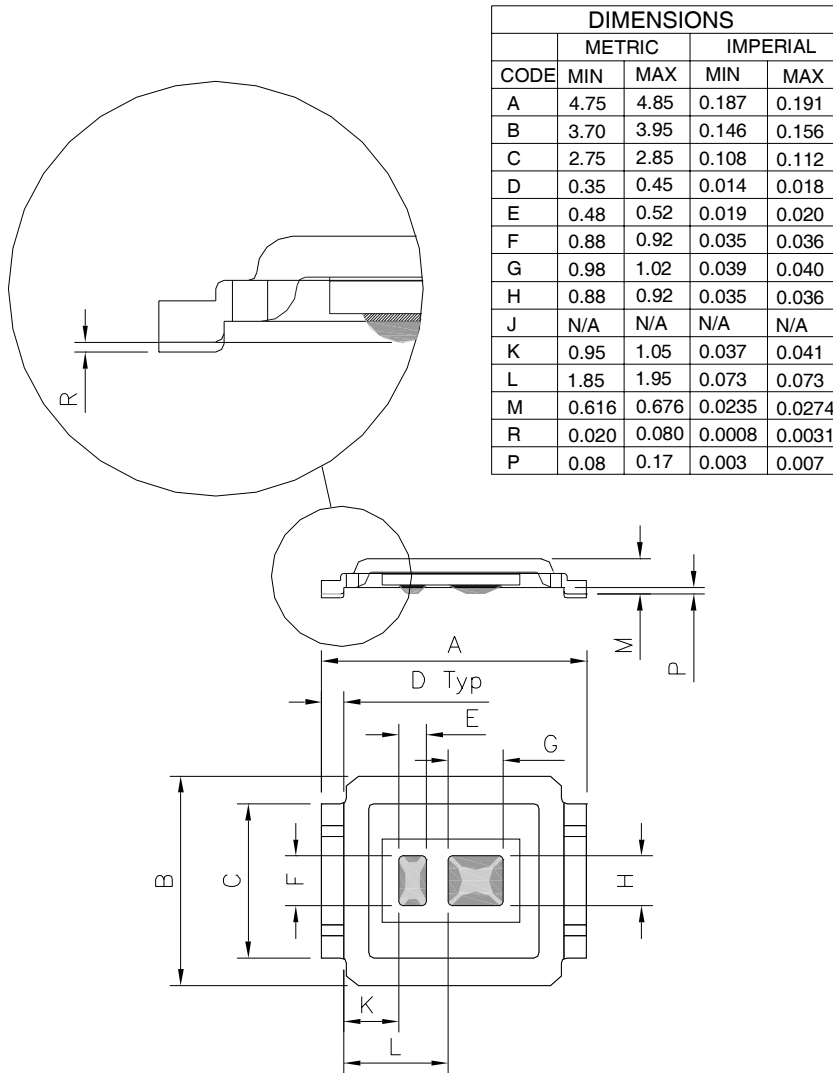
**DirectFET Auto™ Board Footprint, SB (Small Size Can).**

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations

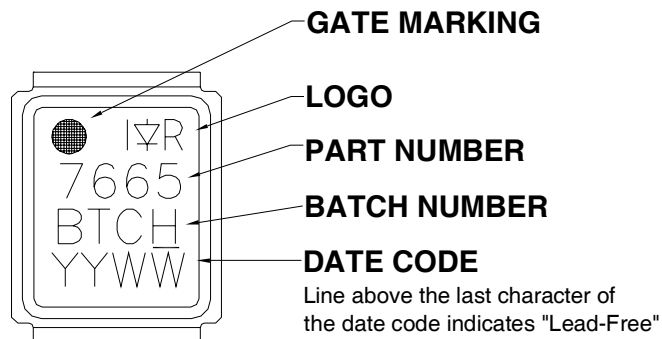


## DirectFET Auto™ Outline Dimension, SB Outline (Small Size Can).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations

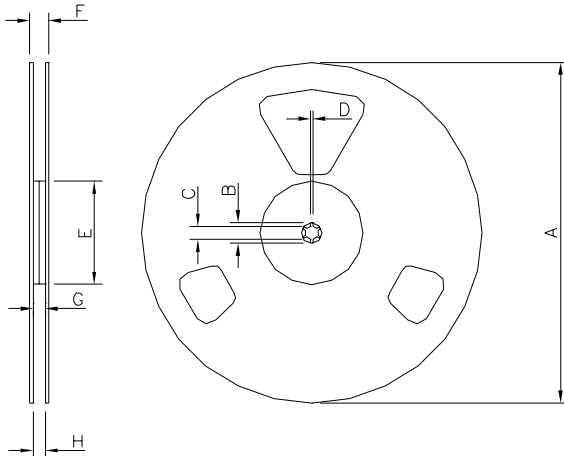


## DirectFET™ Part Marking



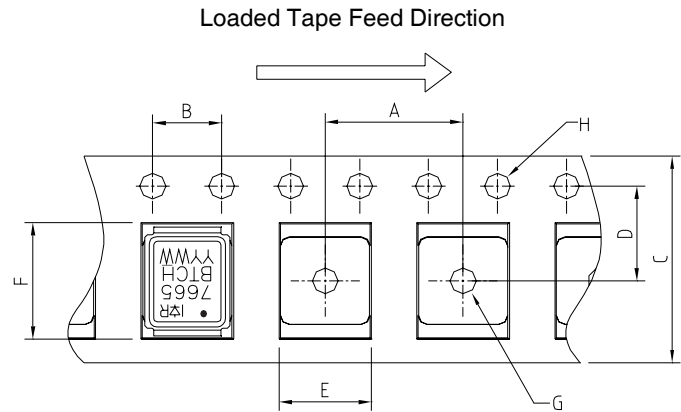


## DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm  
 Std reel quantity is 4800 parts. IRF7665S2PbF

REEL DIMENSIONS				
STANDARD OPTION (QTY 4800)				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	4.00	4.20	0.158	0.165
F	5.00	5.20	0.197	0.205
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.

This product has been designed and qualified to MSL1 rating for the Industrial market.

Additional storage requirement details for DirectFET products can be found in application note AN1035 on IR's Web site.

Qualification Standards can be found on IR's Web site.