International
IOR Rectifier

PD- 95731

IRF7452PbF

SMPS MOSFET

HEXFET® Power MOSFET

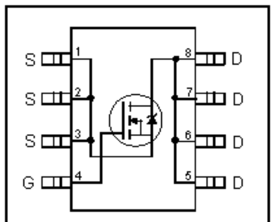
Applications

- High frequency DC-DC converters
- Lead-Free

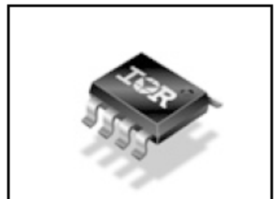
V_{DSS}	$R_{DS(on)}$ max	I_D
100V	**0.060Ω**	**4.5A**

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Top View


SO-8

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	4.5	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	3.6	
I_{DM}	Pulsed Drain Current ①	36	
P_D @T_A = 25°C	Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies

- Telecom 48V input DC-DC with Half Bridge Primary or Datacom 28V input with Passive Reset Forward Converter Primary

Notes ① through ⑤ are on page 8

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.11	–––	V/°C	Reference to 25°C, I_D = 1mA ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.060	Ω	V_{GS} = 10V, I_D = 2.7A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	–––	5.5	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	25	μA	V_{DS} = 100V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 24V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -24V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	3.4	–––	–––	S	V_{DS} = 50V, I_D = 2.7A
Q_g	Total Gate Charge	–––	33	50	nC	I_D = 2.7A
Q_{gs}	Gate-to-Source Charge	–––	7.3	11		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	16	24		V_{GS} = 10V, ④
$t_{d(on)}$	Turn-On Delay Time	–––	9.5	–––	ns	V_{DD} = 50V
t_r	Rise Time	–––	11	–––		I_D = 2.7A
$t_{d(off)}$	Turn-Off Delay Time	–––	16	–––		R_G = 6.0Ω
t_f	Fall Time	–––	13	–––		V_{GS} = 10V ④
C_{iss}	Input Capacitance	–––	930	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	300	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	84	–––		f = 1.0MHz
C_{oss}	Output Capacitance	–––	1370	–––		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	–––	170	–––		V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	–––	280	–––		V_{GS} = 0V, V_{DS} = 0V to 80V ⑤

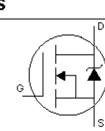
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	–––	200	mJ
I_{AR}	Avalanche Current①	–––	4.5	A
E_{AR}	Repetitive Avalanche Energy①	–––	0.25	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient⑥	–––	50	°C/W

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	2.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	36		
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	T_J = 25°C, I_S = 2.7A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	77	120	ns	T_J = 25°C, I_F = 2.7A
Q_{rr}	Reverse RecoveryCharge	–––	270	410	nC	di/dt = 100A/μs ④

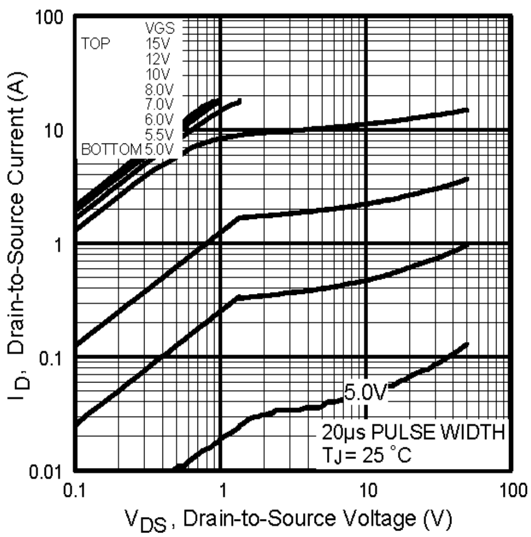


Fig 1. Typical Output Characteristics

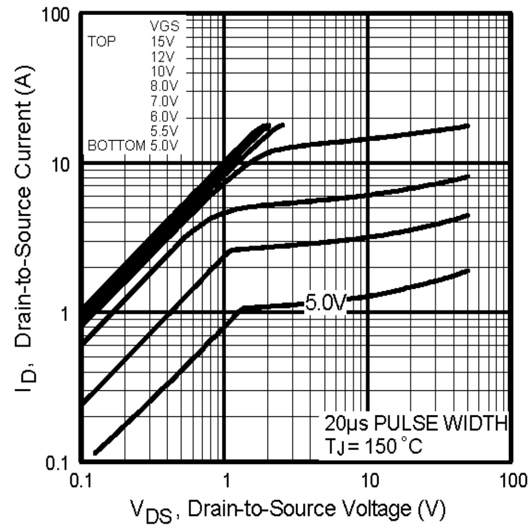


Fig 2. Typical Output Characteristics

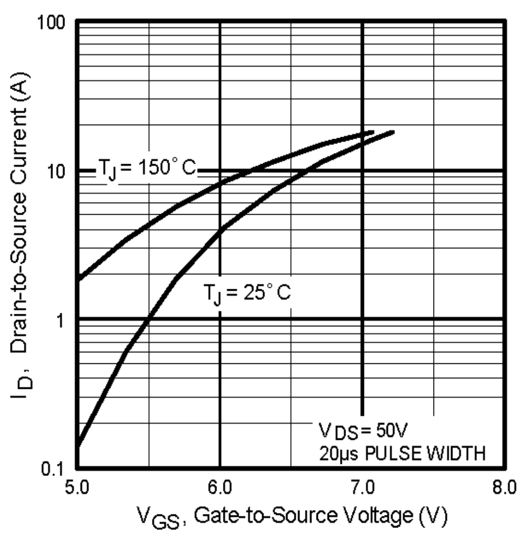


Fig 3. Typical Transfer Characteristics

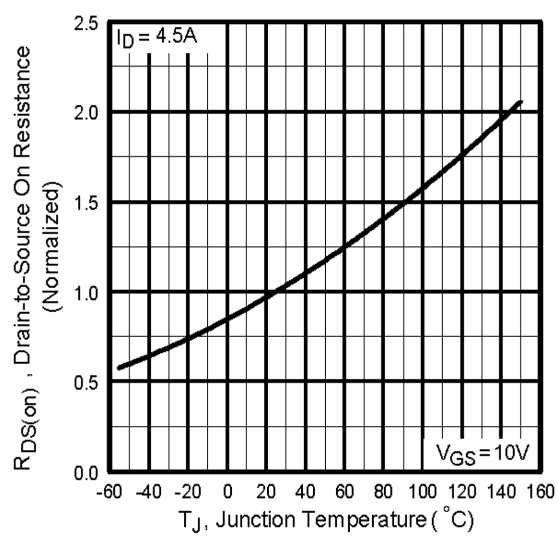


Fig 4. Normalized On-Resistance
Vs. Temperature

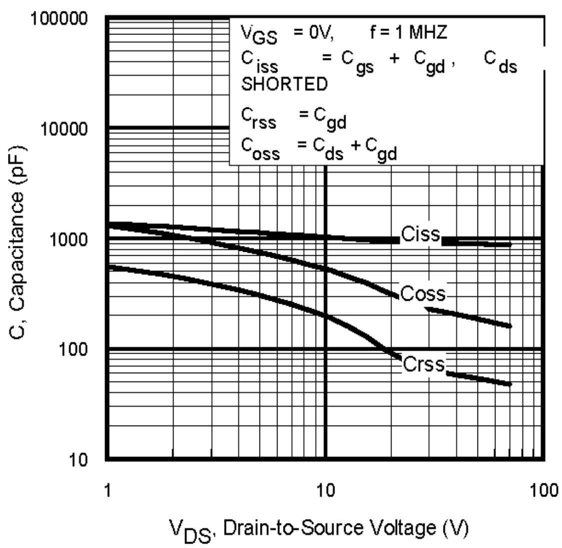


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

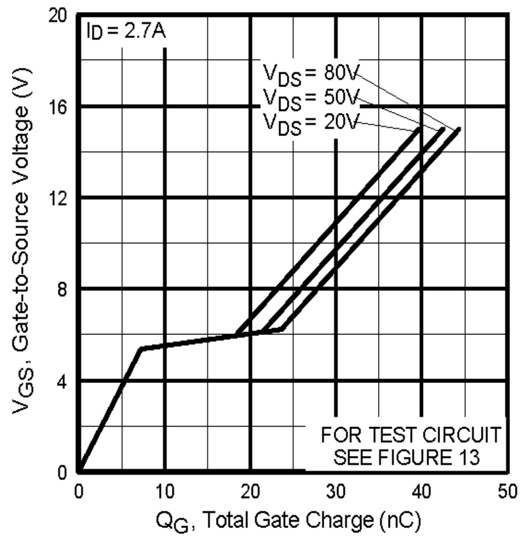


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

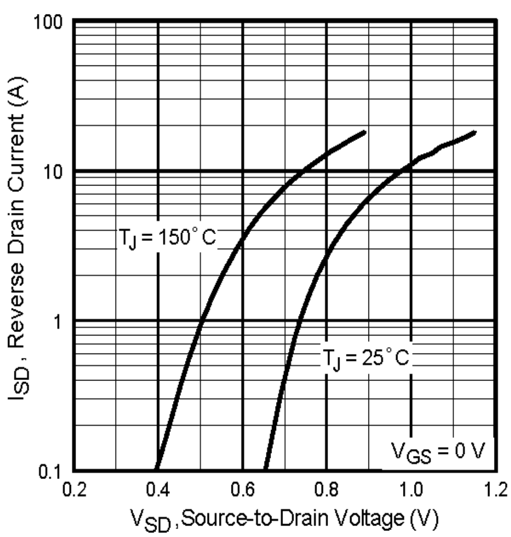


Fig 7. Typical Source-Drain Diode Forward Voltage

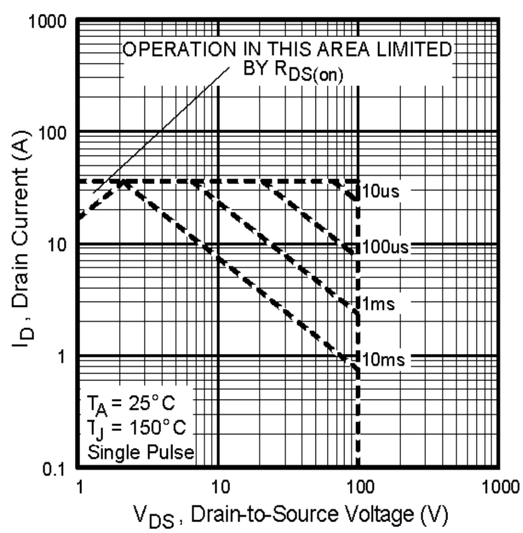
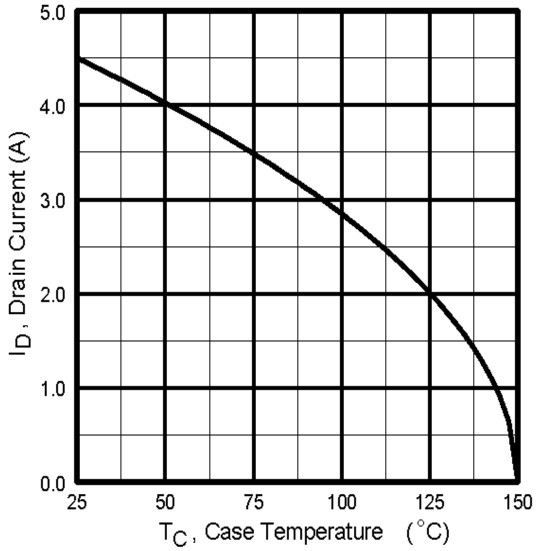


Fig 8. Maximum Safe Operating Area



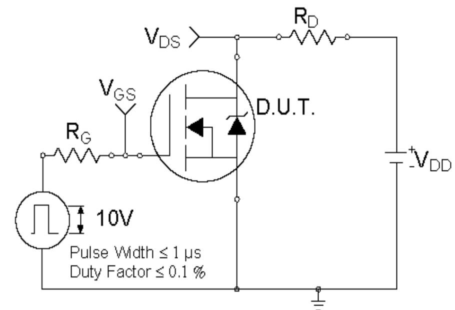


Fig 10a. Switching Time Test Circuit

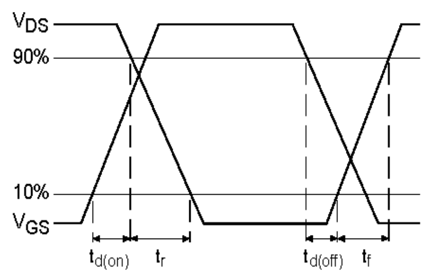


Fig 10b. Switching Time Waveforms

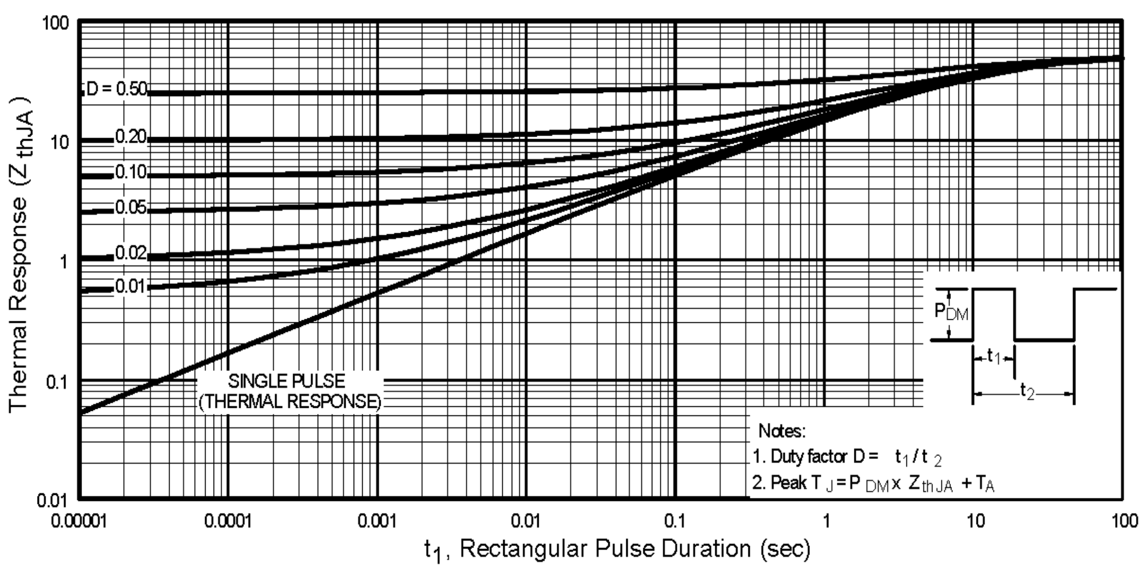


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

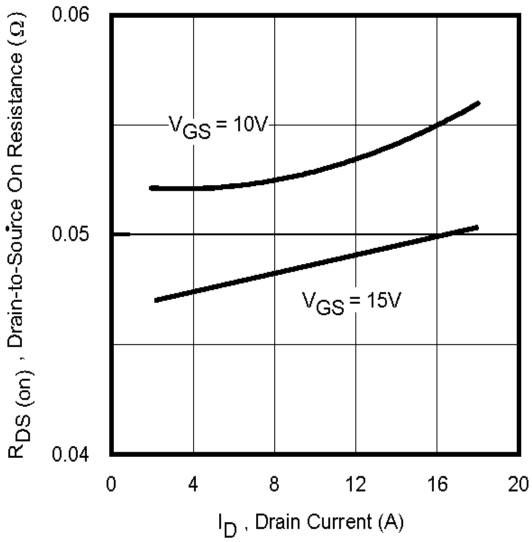


Fig 12. On-Resistance Vs. Drain Current

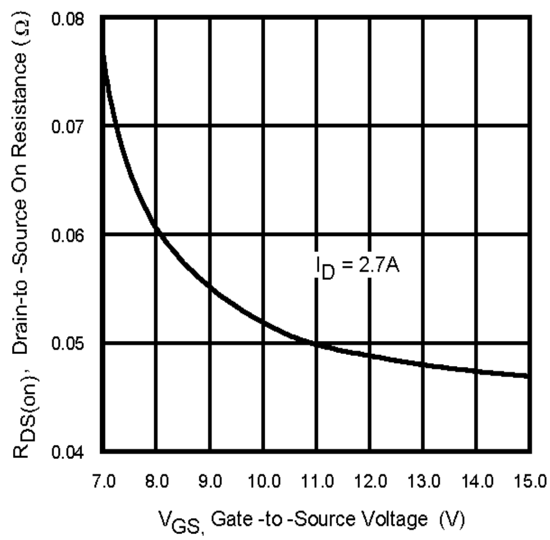


Fig 13. On-Resistance Vs. Gate Voltage

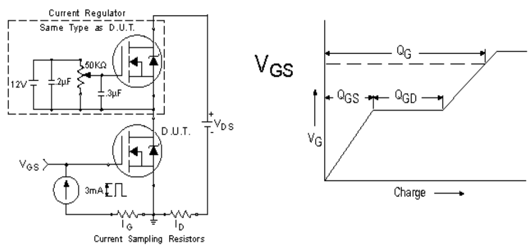
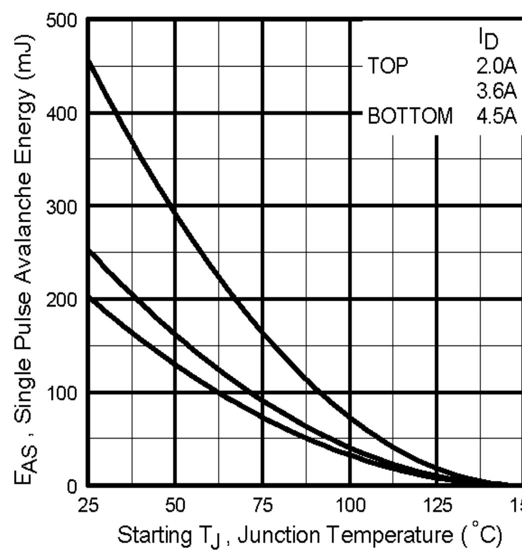


Fig 13a&b. Basic Gate Charge Test Circuit and Waveform



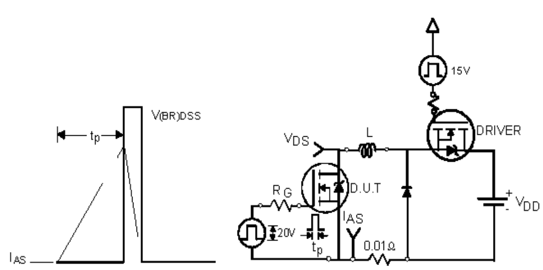
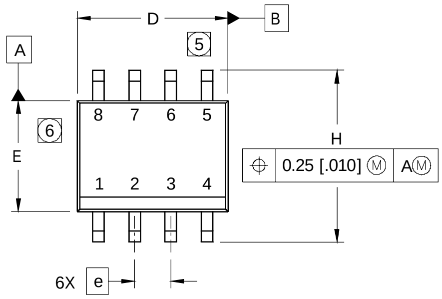


Fig 14a&b. Unclamped Inductive Test circuit and Waveforms

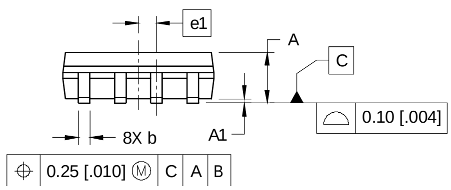
Fig 14c. Maximum Avalanche Energy Vs. Drain Current

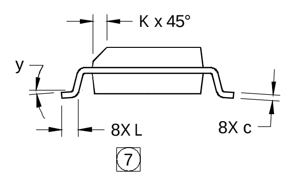
SO-8 Package Outline

Dimensions are shown in millimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

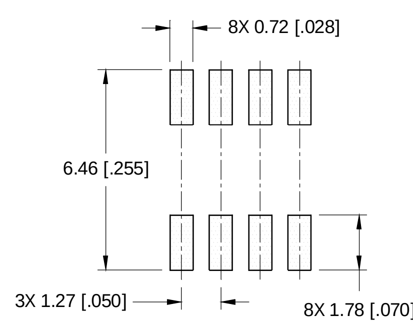




NOTES:

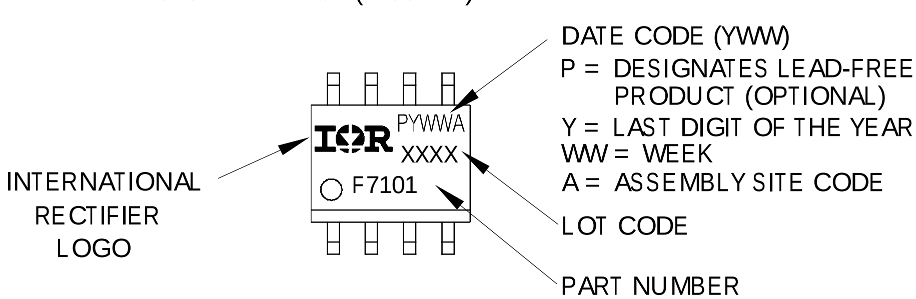
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



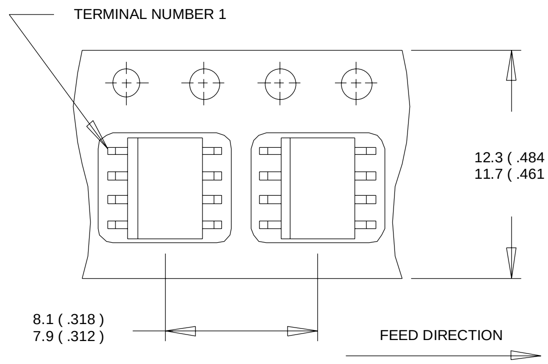
SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

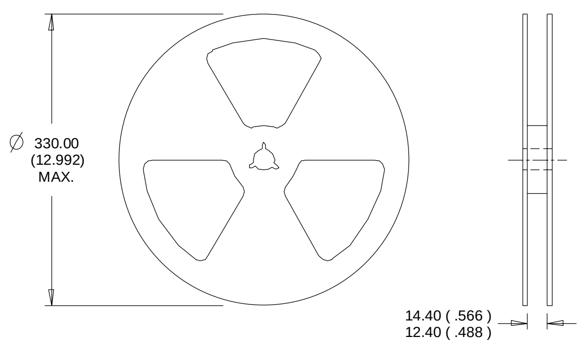


SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

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