

IRF2903ZPbF

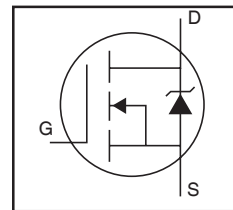
HEXFET® Power MOSFET

Features

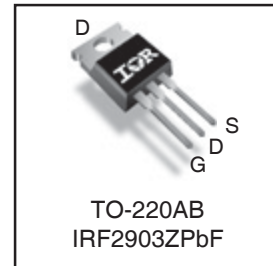
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free

Description

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



$V_{DS} = 30V$
$R_{DS(on)} = 2.4m\Omega$
$I_D = 75A$



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	260	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	180	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	75	
I_{DM}	Pulsed Drain Current ①	1020	
$P_D @ T_C = 25^\circ C$	Power Dissipation	290	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	290	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ③	820	
I_{AR}	Avalanche Current ④	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.51	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑨	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑩	—	62	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.021	—	V/°C	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.9	2.4	m Ω	$V_{GS} = 10V, I_D = 75A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
g_{fs}	Forward Transconductance	120	—	—	S	$V_{DS} = 10V, I_D = 75A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 30V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	160	240	nC	$I_D = 75A$
Q_{gs}	Gate-to-Source Charge	—	51	—		$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	58	—		$V_{GS} = 10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	$V_{DD} = 15V$
t_r	Rise Time	—	100	—		$I_D = 75A$
$t_{d(off)}$	Turn-Off Delay Time	—	48	—		$R_G = 3.2\Omega$
t_f	Fall Time	—	37	—		$V_{GS} = 10V$ ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	6320	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1980	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	1100	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	5930	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	2010	—		$V_{GS} = 0V, V_{DS} = 24V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	3050	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 24V$ ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	1020		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 75A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	34	51	ns	$T_J = 25^\circ\text{C}, I_F = 75A, V_{DD} = 15V$
Q_{rr}	Reverse Recovery Charge	—	29	44	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} ; starting $T_J = 25^\circ\text{C}$, $L = 0.10mH$, $R_G = 25\Omega$, $I_{AS} = 75A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0ms$; duty cycle $\leq 2\%$.
- ④ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ This is only applied to TO-220AB package.
- ⑧ R_θ is measured at T_J approximately 90°C

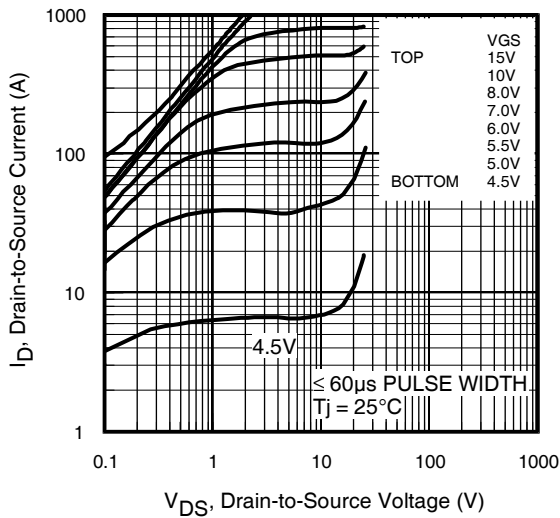


Fig 1. Typical Output Characteristics

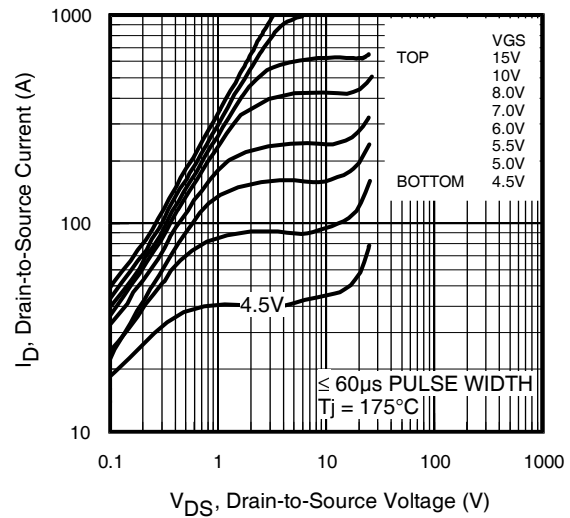


Fig 2. Typical Output Characteristics

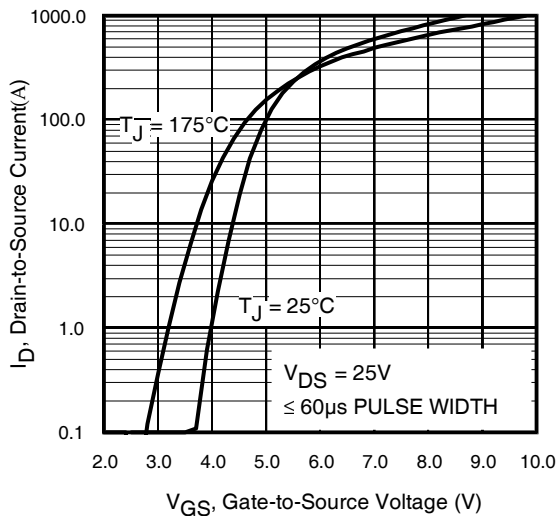


Fig 3. Typical Transfer Characteristics

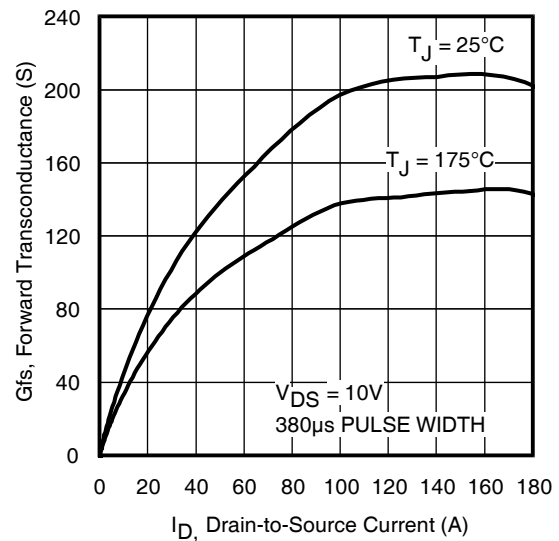


Fig 4. Typical Forward Transconductance Vs. Drain Current

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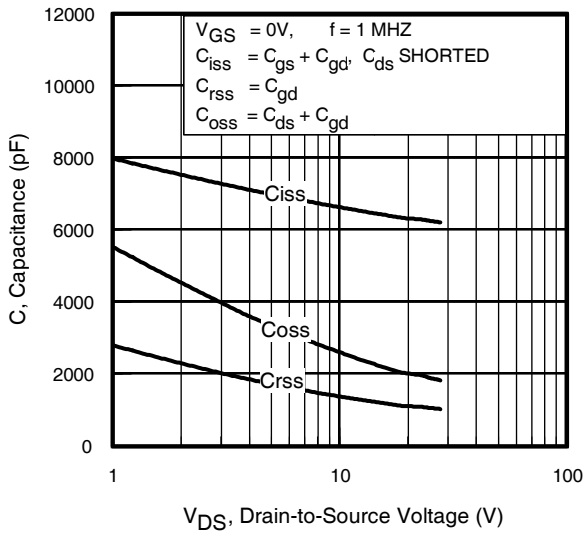


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

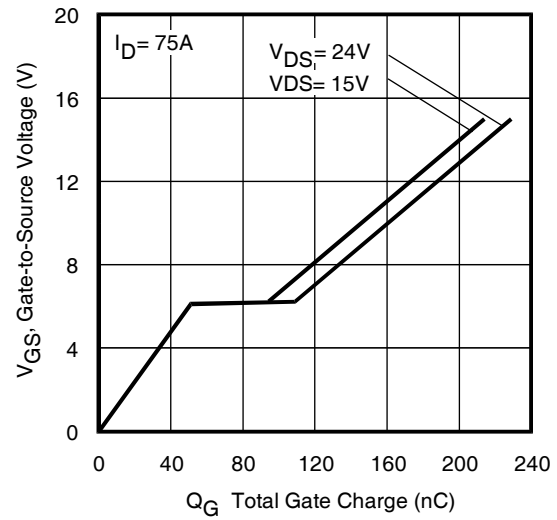


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

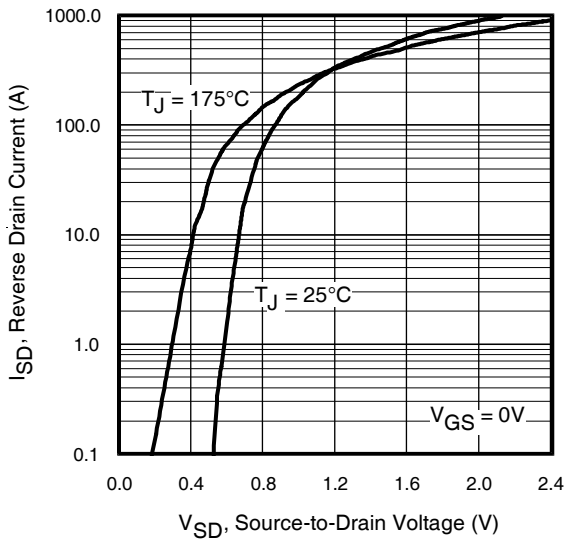


Fig 7. Typical Source-Drain Diode Forward Voltage

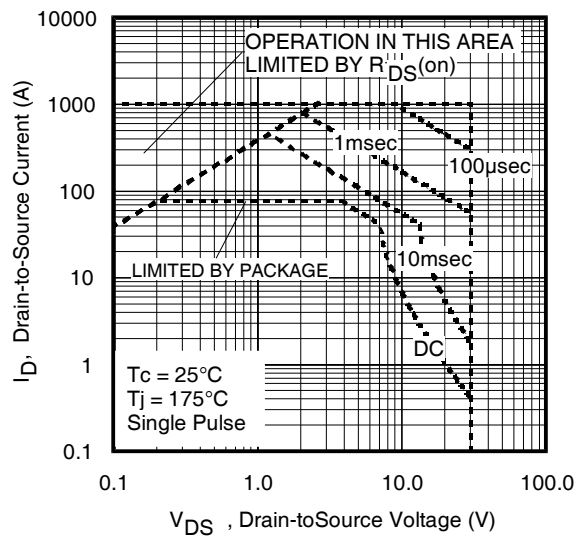


Fig 8. Maximum Safe Operating Area

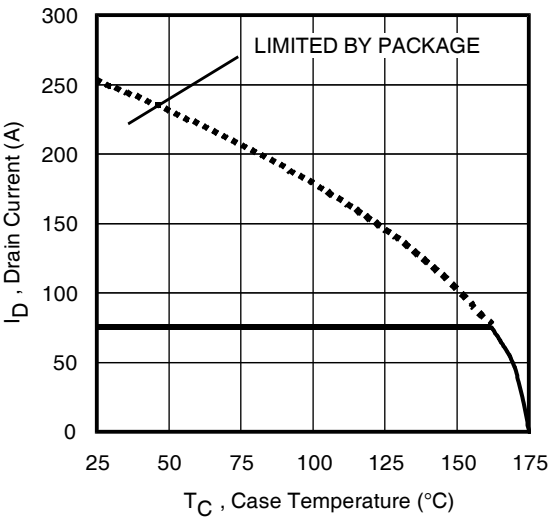


Fig 9. Maximum Drain Current Vs. Case Temperature

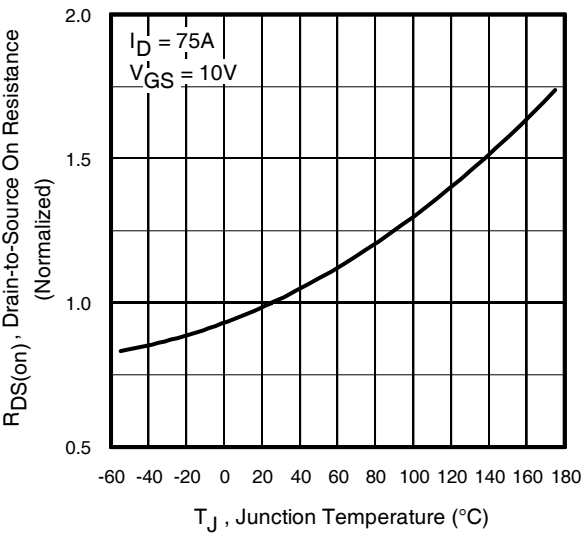


Fig 10. Normalized On-Resistance Vs. Temperature

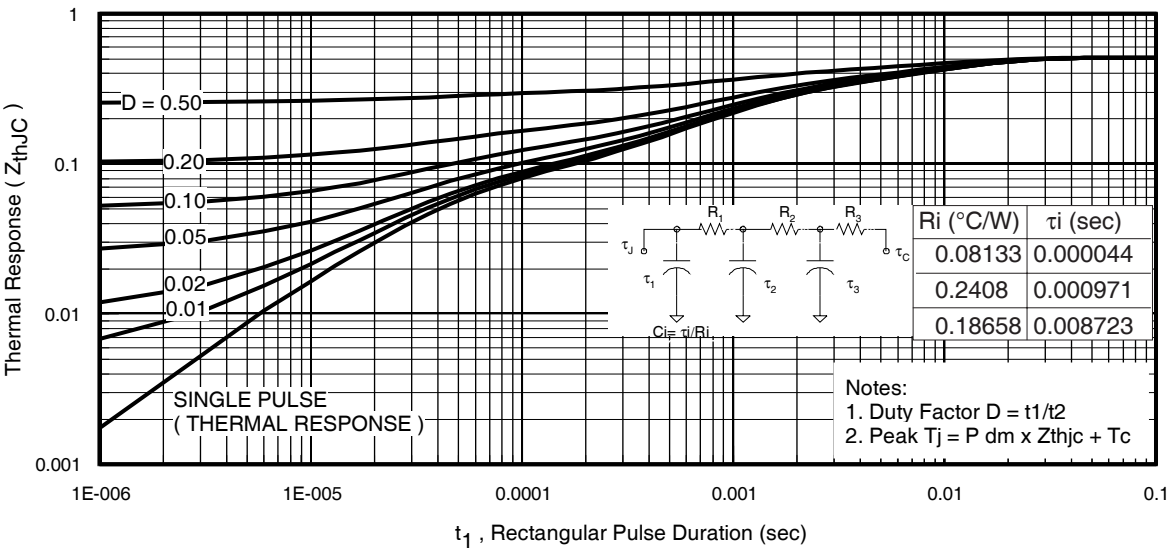


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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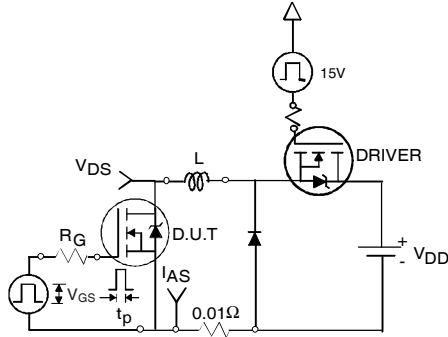


Fig 12a. Unclamped Inductive Test Circuit

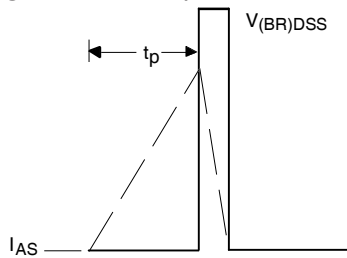


Fig 12b. Unclamped Inductive Waveforms

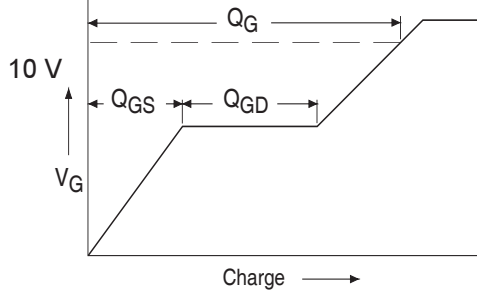


Fig 13a. Basic Gate Charge Waveform

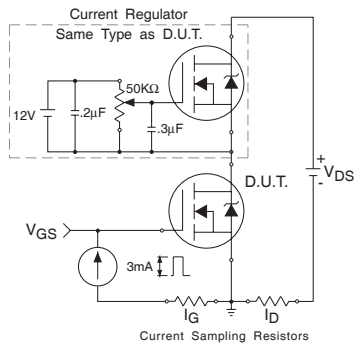


Fig 13b. Gate Charge Test Circuit

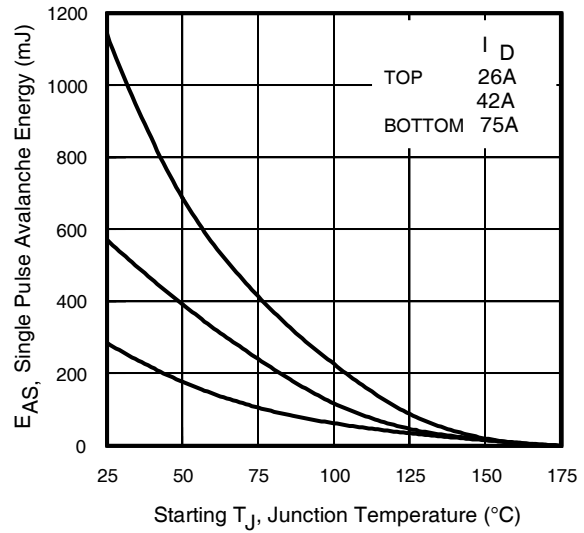


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

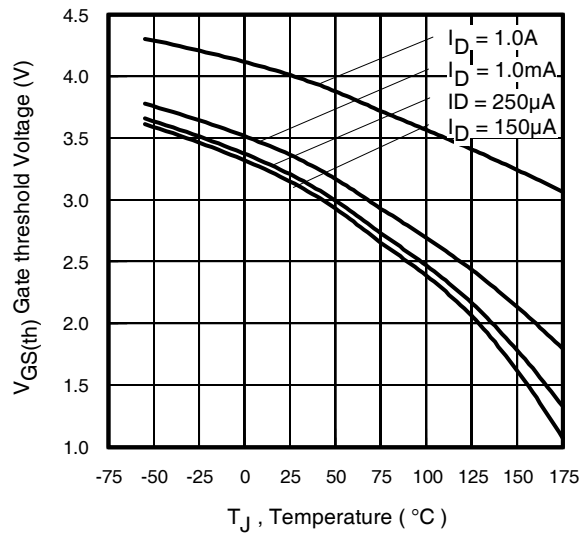


Fig 14. Threshold Voltage Vs. Temperature

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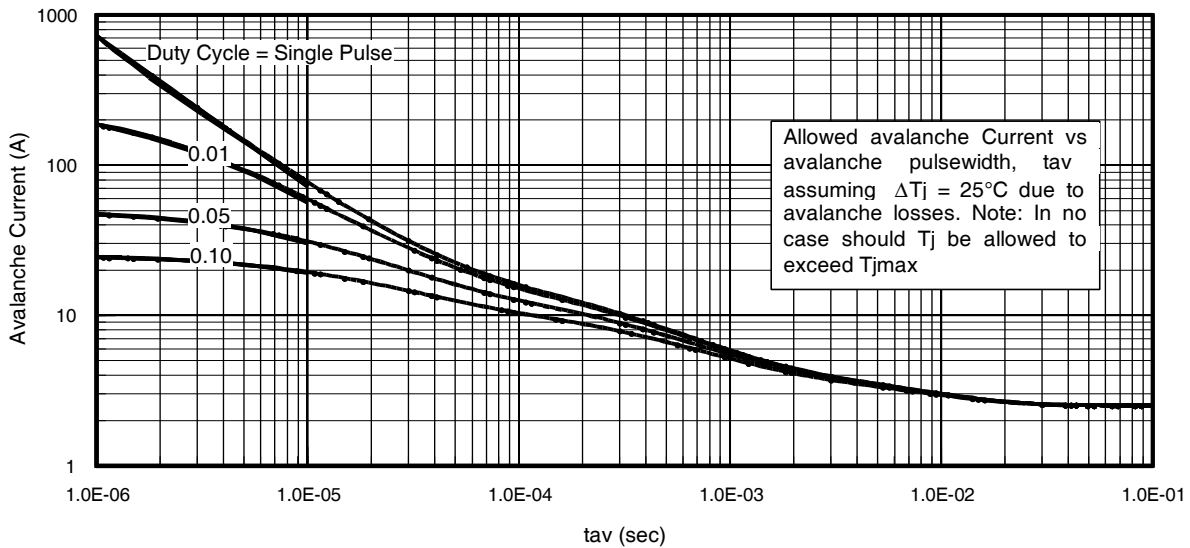


Fig 15. Typical Avalanche Current Vs. Pulsewidth

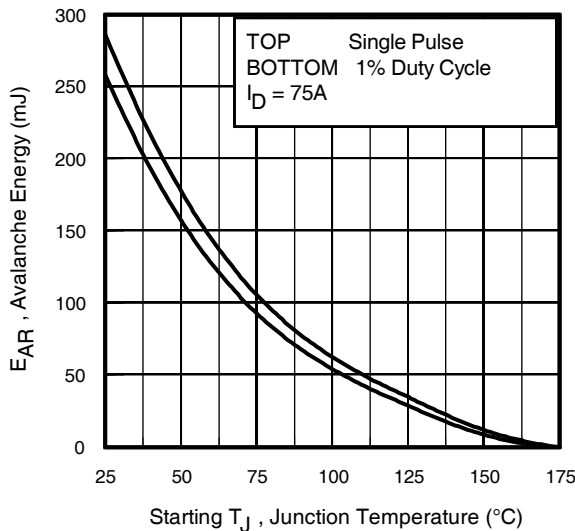


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

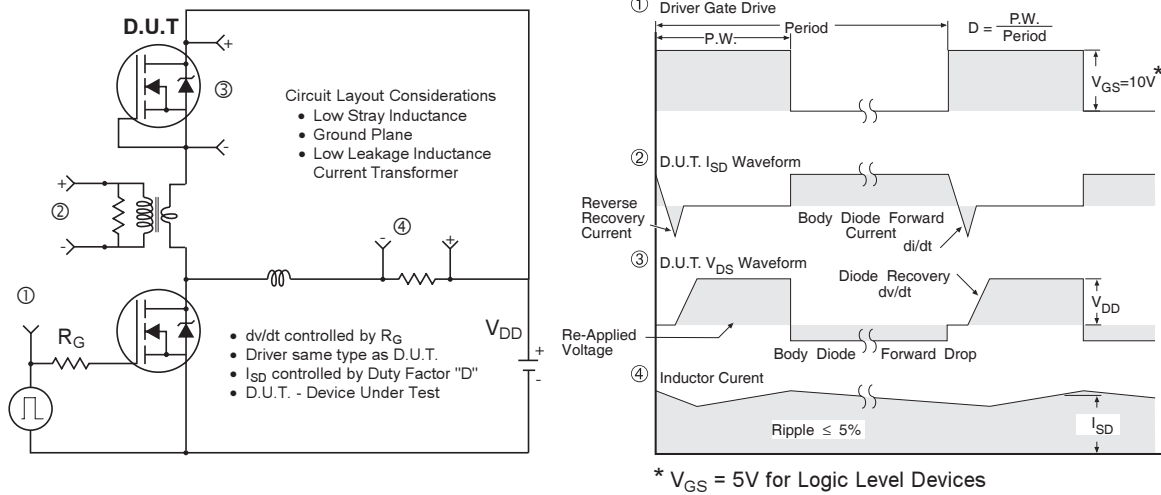


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

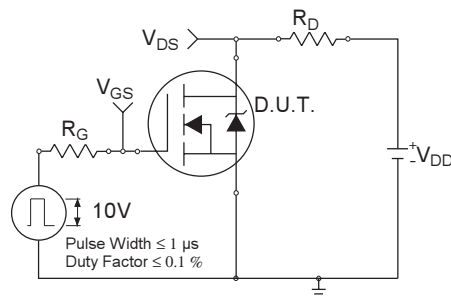


Fig 18a. Switching Time Test Circuit

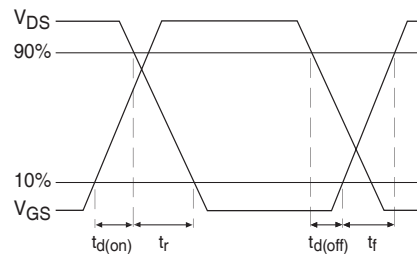
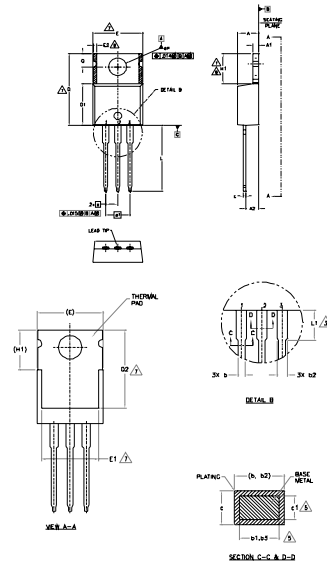


Fig 18b. Switching Time Waveforms

TO-220AB Package Outline(Dimensions are shown in millimeters (inches))



- NOTES
- 1- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M-1994.
 - 2- DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 - 3- LEAD DIMENSIONS AND TOLERANCES UNCONTROLLED IN U.S.
 - 4- DIMENSION D1 BY 8.0 ± 0.15 (0.315) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 5- DIMENSION D2 BY 8.0 ± 0.15 (0.315) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 6- CONTROLLING DIMENSION - INCHES.
 - 7- DIMENSION D2 X 8.0 ± 0.15 (0.315) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 8- DIMENSION D2 X 8.0 ± 0.15 (0.315) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 9- DIMENSION D2 X 8.0 ± 0.15 (0.315) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 10- DIMENSION D2 X 8.0 ± 0.15 (0.315) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.056	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	5
b1	0.38	0.97	.015	.038	
c	1.14	1.78	.045	.070	5
d	1.14	1.73	.045	.068	
e	0.36	0.61	.014	.024	
f	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	0.76	-	.030	.030	8
e	2.54	2.54	.100	.100	
e1	2.54	2.54	.100	.100	
h	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	2.56	4.06	.100	.160	3
MP	2.54	4.06	.100	.160	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

1- GATE
2- SOURCE
3- DRAIN

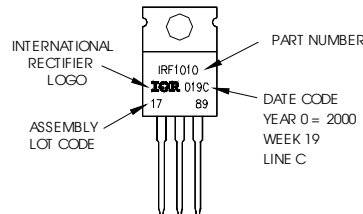
1- GATE
2- SOURCE
3- DRAIN

1- GATE
2- SOURCE
3- DRAIN

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-220AB package is not recommended for Surface Mount Application.

Notes:

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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