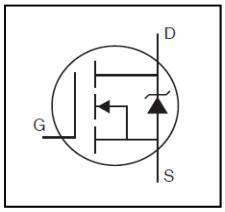
IRF1324S-7PPbF

HEXFET® Power MOSFET



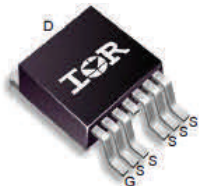
V_{DSS}	**24V**
$R_{DS(on)}$ typ.	**0.8mΩ**
max.	**1.0mΩ**
$I_{D\ (Silicon\ Limited)}$	**429A①**
$I_{D\ (Package\ Limited)}$	**240A**

Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



D^2Pak 7 Pin

G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF1324S-7PPbF	D^2Pak 7 Pin	Tube	50	IRF1324S-7PPbF
		Tape and Reel Left	800	IRF1324STRL-7PP

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	429①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	303①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	240	
I_{DM}	Pulsed Drain Current ②	1640	
P_D @T_C = 25°C	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	1.6	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ③	230	mJ
I_{AR}	Avalanche Current ②	See Fig.14,15, 18a, 18b	A
E_{AR}	Repetitive Avalanche Energy		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	—	0.50	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑧	—	40	

HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	24	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.023	—	V/°C	Reference to 25°C, I_D = 5mA ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.80	1.0	mΩ	V_{GS} = 10V, I_D = 160A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} =24V, V_{GS} = 0V
		—	—	250		V_{DS} =19V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
R_G	Gate Resistance	—	3.0	—	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

gfs	Forward Trans conductance	190	—	—	S	V_{DS} = 15V, I_D = 160A
Q_g	Total Gate Charge	—	180	252	nC	I_D = 75A
Q_{gs}	Gate-to-Source Charge	—	47	—		V_{DS} = 12V
Q_{gd}	Gate-to-Drain Charge	—	58	—		V_{GS} = 10V⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	—	122	—		
$t_{d(on)}$	Turn-On Delay Time	—	19	—	ns	V_{DD} = 16V
t_r	Rise Time	—	240	—		I_D = 160A
$t_{d(off)}$	Turn-Off Delay Time	—	86	—		R_G= 2.7Ω
t_f	Fall Time	—	93	—		V_{GS} = 10V⑤
C_{iss}	Input Capacitance	—	7700	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	3380	—		V_{DS} = 19V
C_{rss}	Reverse Transfer Capacitance	—	1930	—		f = 1.0MHz, See Fig. 5
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	4780	—		V_{GS} = 0V, V_{DS} = 0V to 19V⑦
$C_{oss\ eff.(TR)}$	Effective Output Capacitance (Time Related)	—	4970	—		V_{GS} = 0V, V_{DS} = 0V to 19V⑥

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	429①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	1640		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 160A,V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	—	71	107	ns	T_J = 25°C V_{DD} = 20V
		—	74	110		T_J = 125°C I_F = 160A,
Q_{rr}	Reverse Recovery Charge	—	83	120	nC	T_J = 25°C di/dt = 100A/µs ⑤
		—	92	140		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	2.0	—	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.018mH, R_G = 25Ω, I_{AS} = 160A, V_{GS} =10V. Part not recommended for use above this value.

④ I_{SD} ≤ 160A, di/dt ≤ 600A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

⑨ R_θ is measured at T_J approximately 90°C.

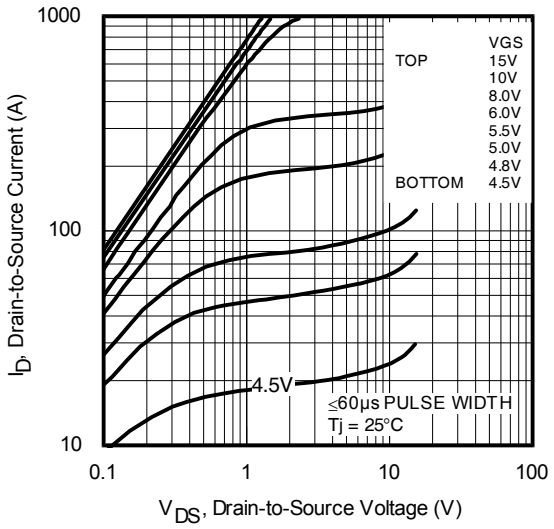


Fig. 1 Typical Output Characteristics

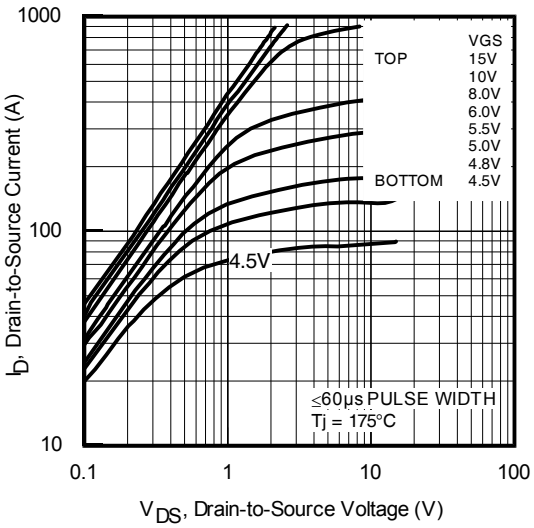


Fig. 2 Typical Output Characteristics

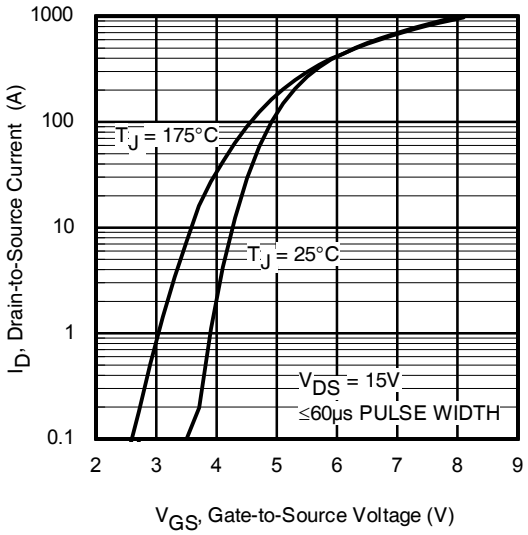


Fig. 3 Typical Transfer Characteristics

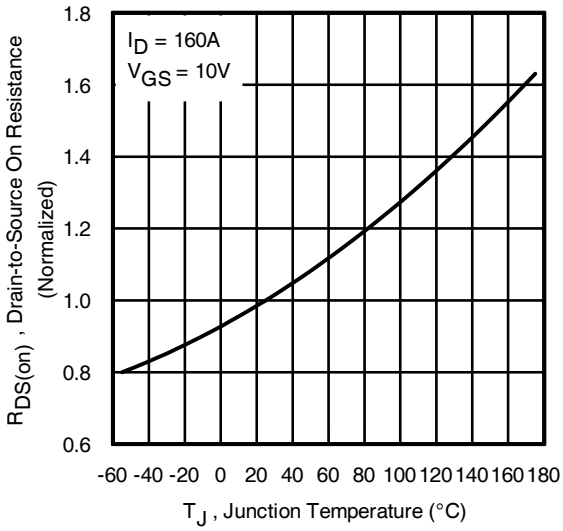


Fig. 4 Normalized On-Resistance vs. Temperature

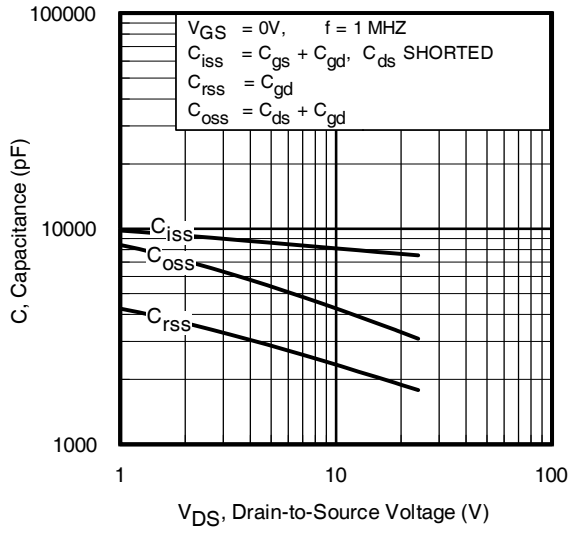


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

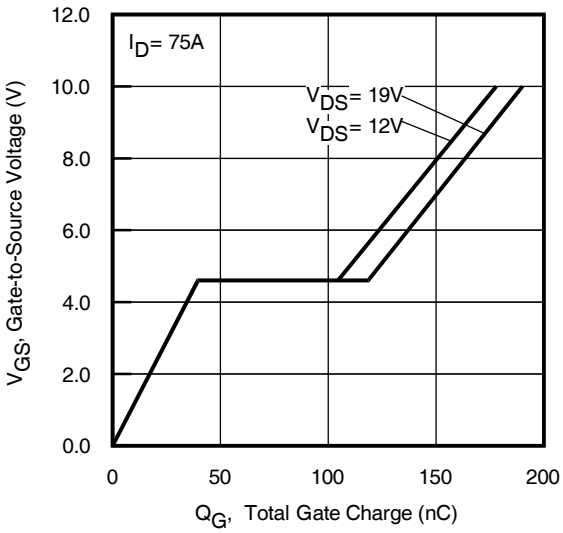


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

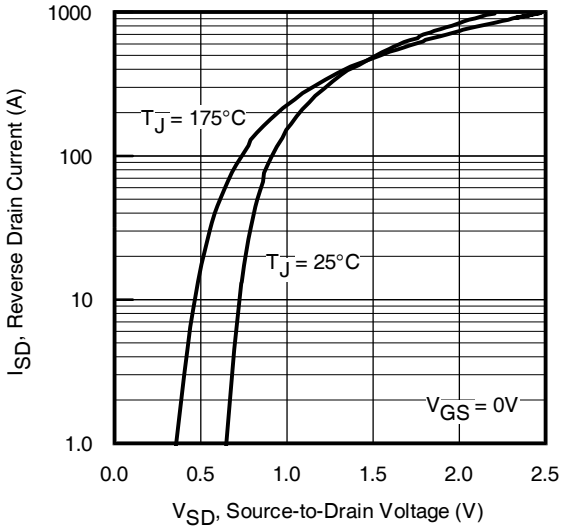


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

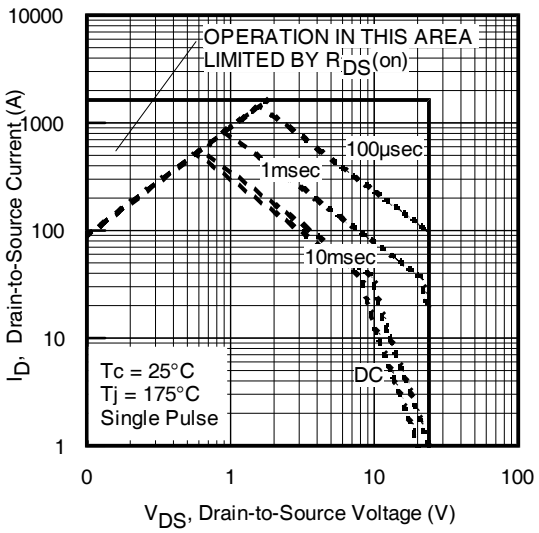


Fig 8. Maximum Safe Operating Area

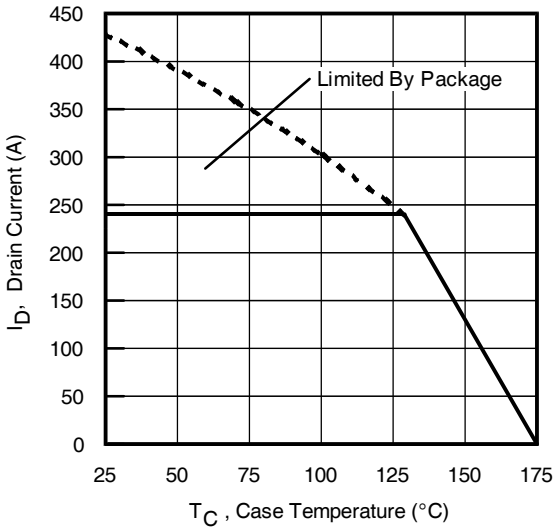


Fig 9. Maximum Drain Current vs. Case Temperature

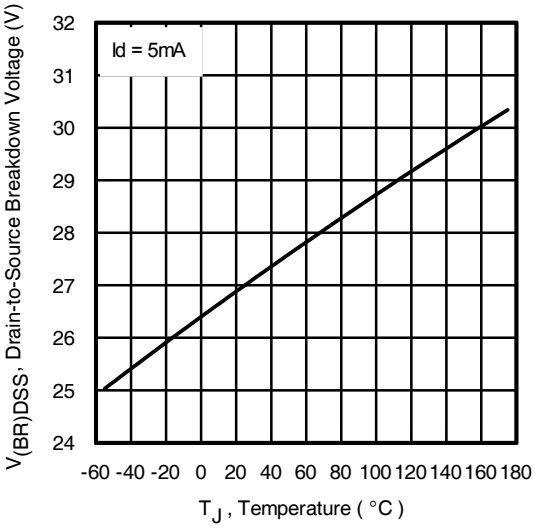


Fig 10. Drain-to-Source Breakdown Voltage

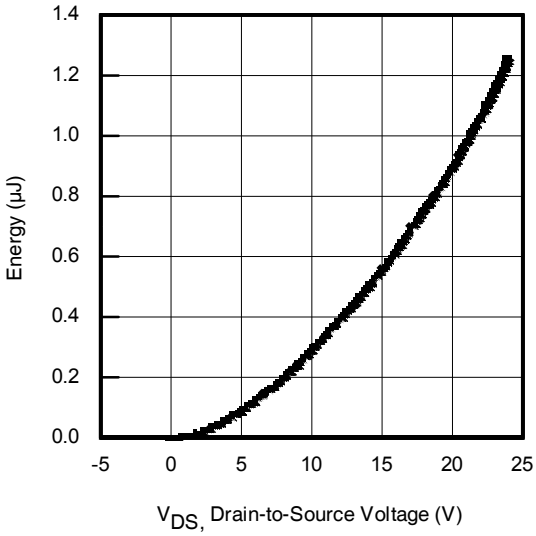


Fig 11. Typical Coss Stored Energy

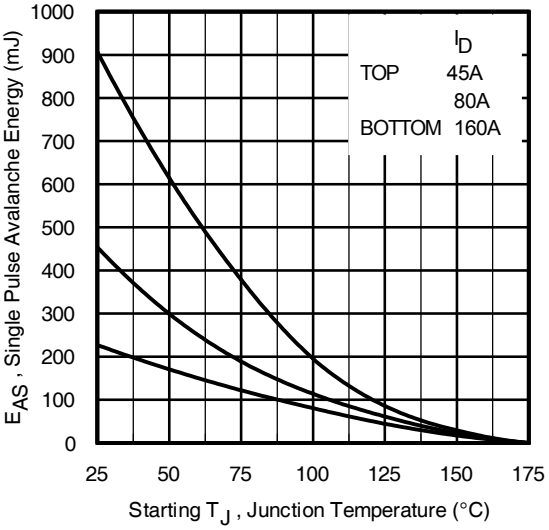


Fig 12. Maximum Avalanche Energy vs. Drain Current

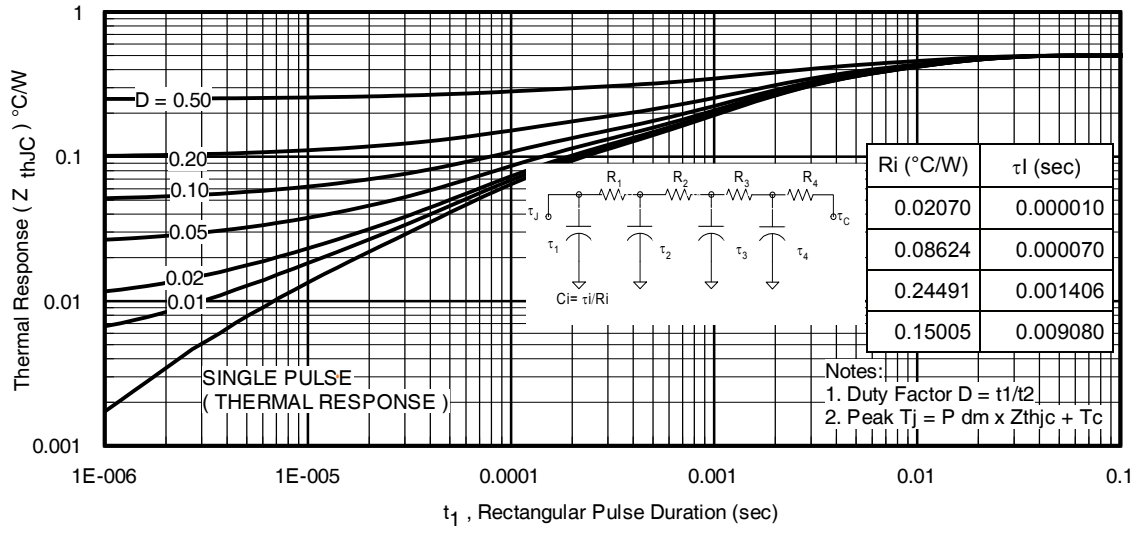


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

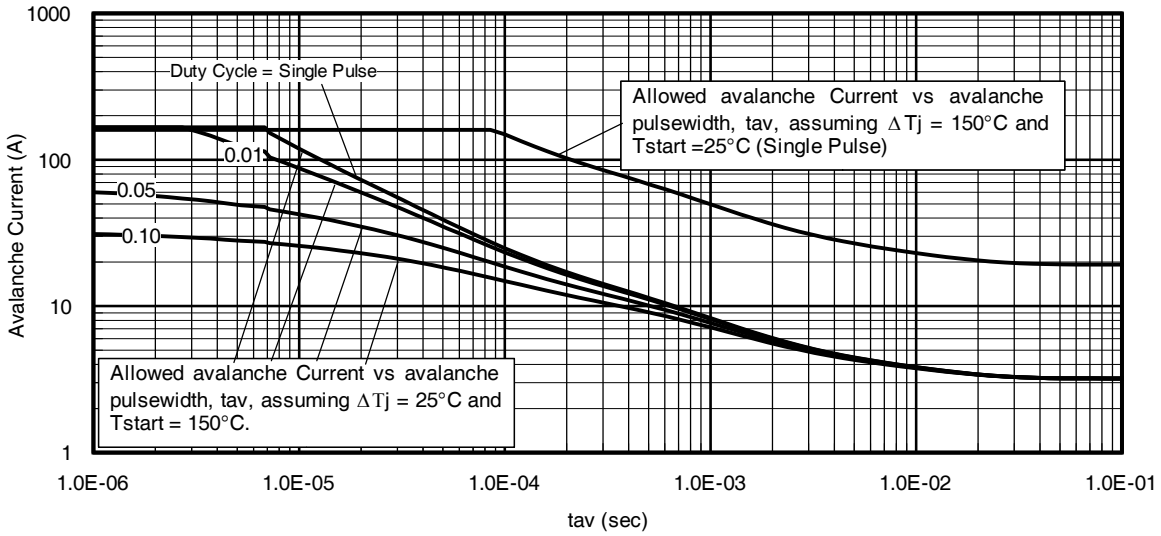


Fig 14. Avalanche Current vs. Pulse width

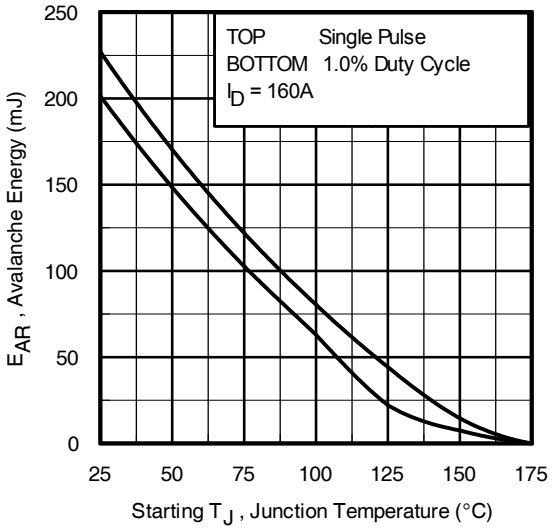


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

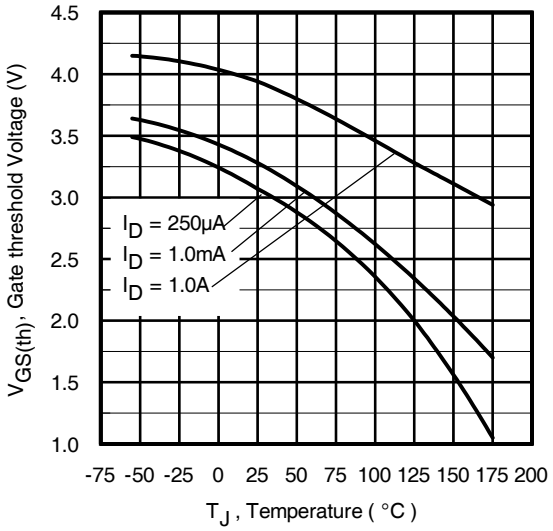


Fig 16. Threshold Voltage vs. Temperature

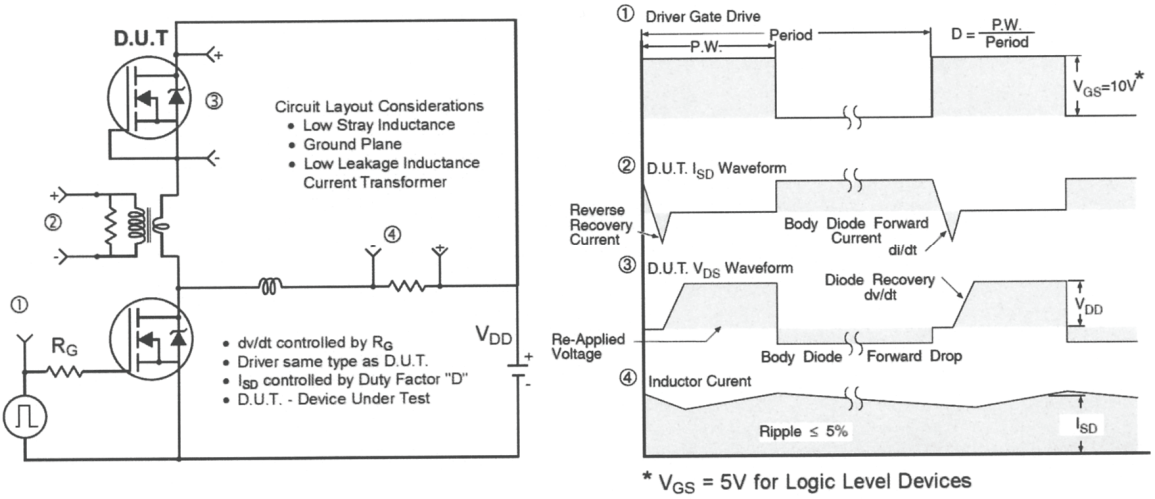


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

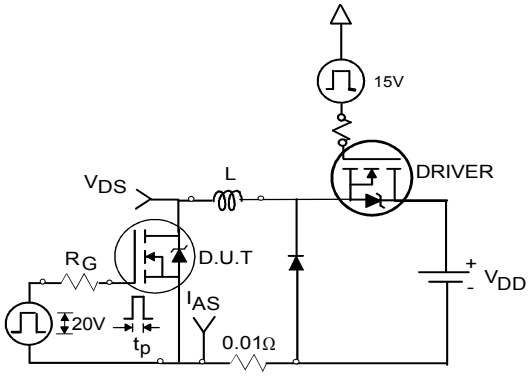


Fig 18a. Unclamped Inductive Test Circuit

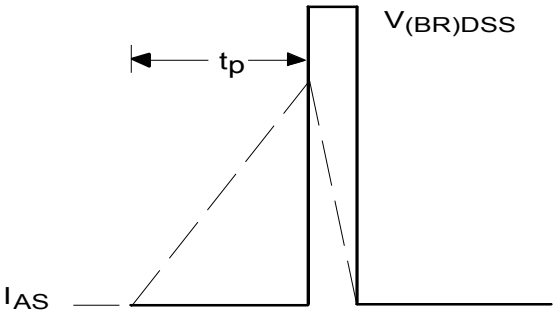


Fig 18b. Unclamped Inductive Waveforms

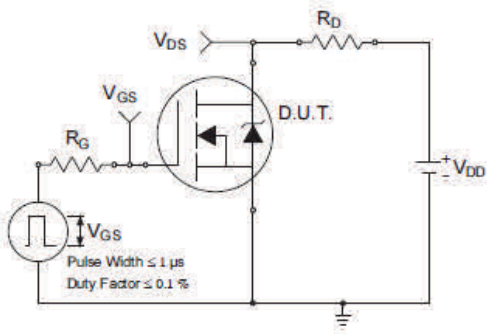


Fig 19a. Switching Time Test Circuit

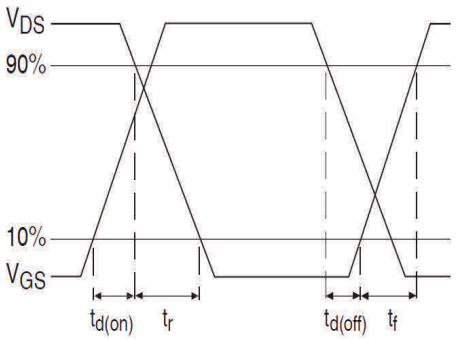


Fig 19b. Switching Time Waveforms

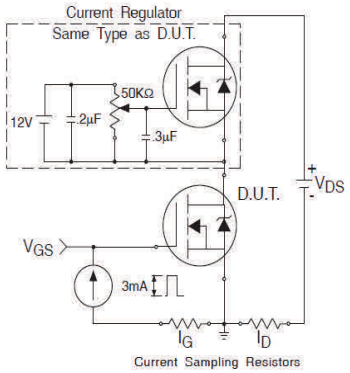


Fig 20a. Gate Charge Test Circuit

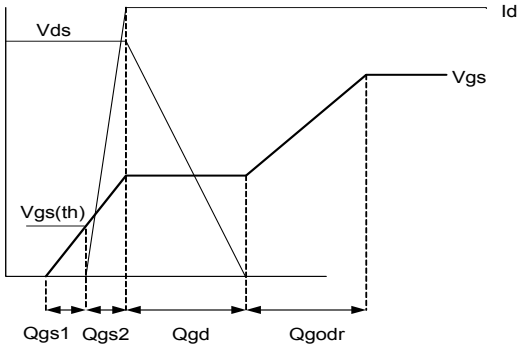
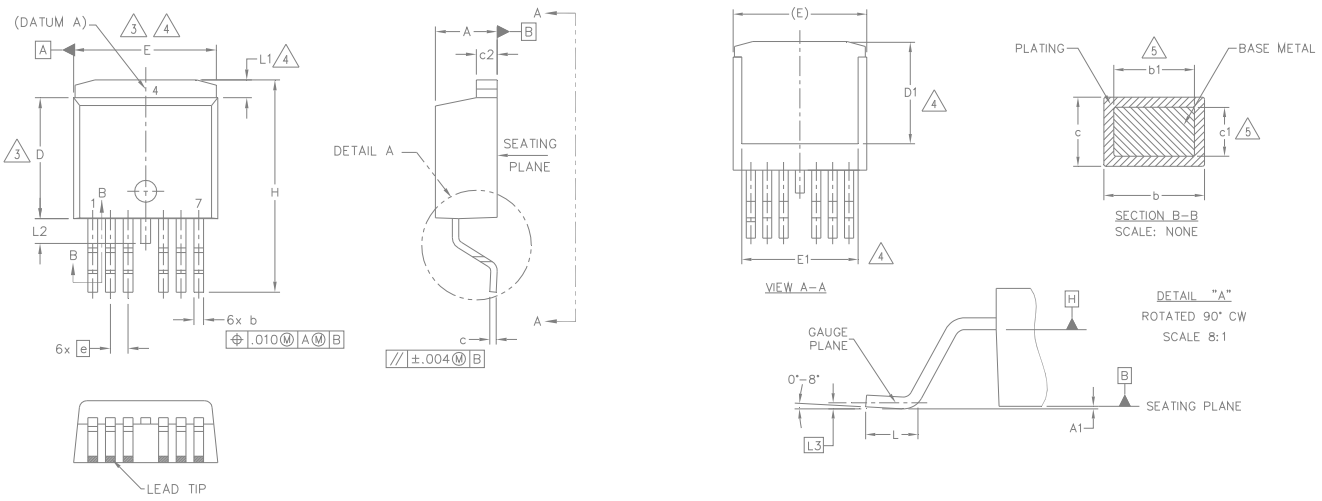


Fig 20b. Gate Charge Waveform

D²Pak - 7 Pin Package Outline (Dimensions are shown in millimeters (inches))



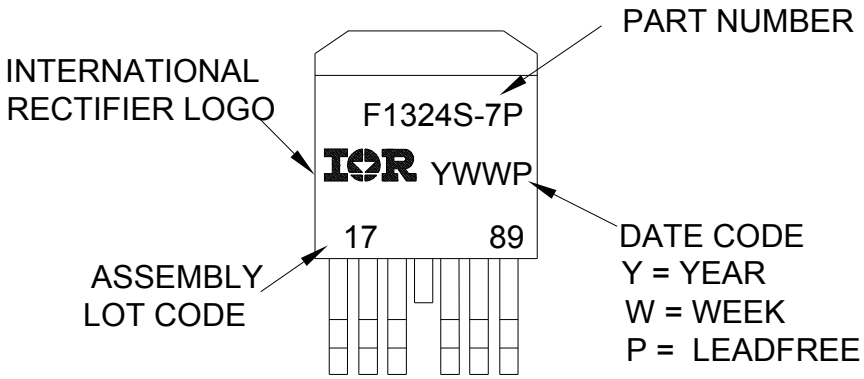
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	–	0.254	–	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	7.42	.270	.292	4
E	9.65	10.54	.380	.415	3,4
E1	6.22	8.48	.245	.334	4
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB. EXCEPT FOR DIMS. E, E1 & D1.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D²Pak - 7 Pin Part Marking Information

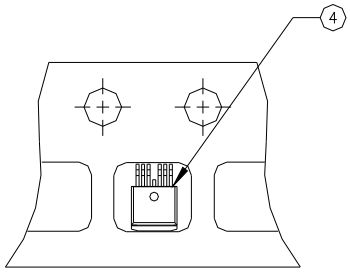


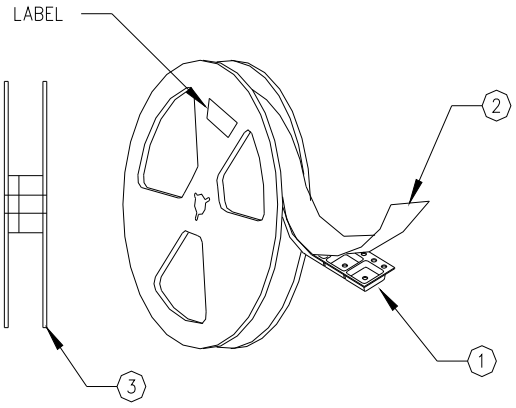
D²Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
   - 1.1 REEL SIZE 13 INCH DIAMETER.
   - 1.2 EACH REEL CONTAINING 800 DEVICES.
   - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
   - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
   - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
   - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).
   - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
   - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
   - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
   - 2.4 QUANTITY:
   - 2.5 VENDOR CODE: IR
   - 2.6 LOT CODE:
   - 2.7 DATE CODE:





Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information

Qualification Level	Industrial†† (per JEDEC JESD47F†† guidelines)	
Moisture Sensitivity Level	D^2-Pak 7 Pin	MSL1 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http//www.irf.com/

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
4/8/2014	• Added Ordering information table on page 1 • Updated package outline on page 8 • Updated part marking on page 9 • Added Qualification table on page 10. • Updated data sheet with new IR corporate template.
10/15/2015	• Updated datasheet with corporate template • Updated typo on GFS from "V_{DD} =50V, I_D =160A, Min= 270S to "V_{DD} = 15V,I_D =160A Min =190S on page 2. • Corrected typo on Fig9 package limited from "160A" to "240A" on page 4.

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