

IR2175(S) & (PbF)

LINEAR CURRENT SENSING IC

Features

- Floating channel up to +600V
- Monolithic integration
- Linear current feedback through shunt resistor
- Direct digital PWM output for easy interface
- Low IQBS allows the boot strap power supply
- Independent fast overcurrent trip signal
- High common mode noise immunity
- Input overvoltage protection for IGBT short circuit condition
- Open Drain outputs
- Also available LEAD-FREE

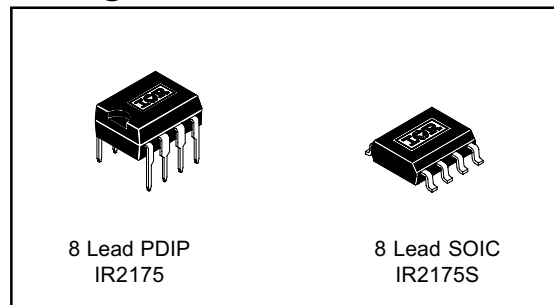
Description

The IR2175 is a monolithic current sensing IC designed for motor drive applications. It senses the motor phase current through an external shunt resistor, converts from analog to digital signal, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The output format is discrete PWM to eliminate need for the A/D input interface for the IR2175. The dedicated overcurrent trip (OC) signal facilitates IGBT short circuit protection. The open-drain outputs make easy for any interface from 3.3V to 15V. S

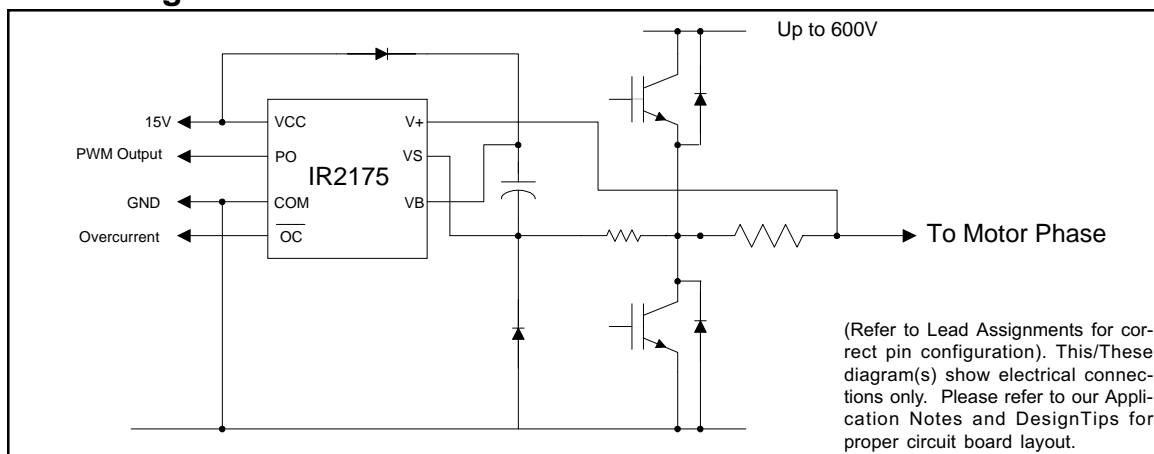
Product Summary

V _{OFFSET}	600V _{max}
I _{QBS}	2mA
V _{in}	+/-260mV _{max}
Gain temp.drift	20ppm/°C (typ.)
f _o	130kHz (typ.)
Overcurrent trip signal delay	2μsec (typ)
Overcurrent trip level	+/-260mV (typ.)

Packages



Block Diagram



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _S	High side offset voltage	-0.3	600	V	
V _{BS}	High side floating supply voltage	-0.3	25		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{IN}	Maximum input voltage between V _{IN+} and V _S	-5	5		
V _{PO}	Digital PWM output voltage	COM -0.3	VCC +0.3		
V _{OC}	Overcurrent output voltage	COM -0.3	VCC +0.3		
dV/dt	Allowable offset voltage slew rate	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	8 lead SOIC	—	.625	W
		8 lead PDIP	—	1.0	
R _{thJA}	Thermal resistance, junction to ambient	8 lead SOIC	—	200	°C/W
		8 lead PDIP	—	125	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Note 1: Capacitors are required between V_B and V_S when bootstrap power is used. The external power supply, when used, is required between V_B and V_S pins.

Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply voltage	V _S +13.0	V _S +20	V
V _S	High side floating supply offset voltage	0.3	600	
V _{PO}	Digital PWM output voltage	COM	VCC	
V _{OC}	Overcurrent output voltage	COM	VCC	
V _{CC}	Low side and logic fixed supply voltage	9.5	20	
V _{IN}	Input voltage between V _{IN+} and V _S	-260	+260	mV
T _A	Ambient temperature	-40	125	°C

DC Electrical Characteristics

V_{CC} = V_{BS} = 15V, and T_A = 25° unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V _{IN}	Nominal input voltage range before saturation V _{IN+} - V _S	-260	—	260	mV	
V _{OC+}	Overcurrent trip positive input voltage	—	260	—		
V _{OC-}	Overcurrent trip negative input voltage	—	-260	—		
V _{OS}	Input offset voltage	-10	0	10		V _{IN} = 0V (Note 1)
ΔV _{OS} /ΔT _A	Input offset voltage temperature drift	—	25	—	μV/°C	
G	Gain (duty cycle % per V _{IN})	155	160	165	%/V	max gain error=5% (Note 2)
ΔG/ΔT _A	Gain temperature drift	—	20	—	ppm/°C	
I _{LK}	Offset supply leakage current	—	—	50	μA	V _B = V _S = 600V
I _{QBS}	Quiescent V _{BS} supply current	—	2	—	mA	V _S = 0V
I _{QCC}	Quiescent V _{CC} supply current	—	—	0.5		
L _{IN}	Linearity (duty cycle deviation from ideal linearity curve)	—	0.5	1	%	
ΔV _{LIN} /ΔT _A	Linearity temperature drift	—	.005	—	%/°C	
I _{OPO}	Digital PWM output sink current	20	—	—	mA	V _O = 1V
		2	—	—		V _O = 0.1V
I _{OCC}	OC output sink current	10	—	—		V _O = 1V
		1	—	—		V _O = 0.1V

Note 1: ±10mV offset represents ±1.5% duty cycle fluctuation

Note 2: Gain = (full range of duty cycle in %) / (full input voltage range).

AC Electrical Characteristics

V_{CC} = V_{BS} = 15V, and T_A = 25° unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
f _o	Carrier frequency output	100	130	180	kHz	figure 1
Δf/ΔT _A	Temperature drift of carrier frequency	—	500	—	ppm/°C	V _{IN} = 0 & 5V
D _{min}	Minimum duty	—	9	—	%	V _{IN+} = -260mV,
D _{max}	Maximum duty	—	91	—	%	V _{IN+} = +260mV
BW	f _o bandwidth	—	15	—	kHz	V _{IN+} = 100mVpk -pk sine wave, gain=-3dB
PHS	Phase shift at 1kHz	—	-10	—	°	V _{IN+} = 100mVpk-pk sine wave
tdoc	Propagation delay time of OC	1	2	—	μsec	
twoc	Low true pulse width of OC	—	1.5	—		

Timing Waveforms

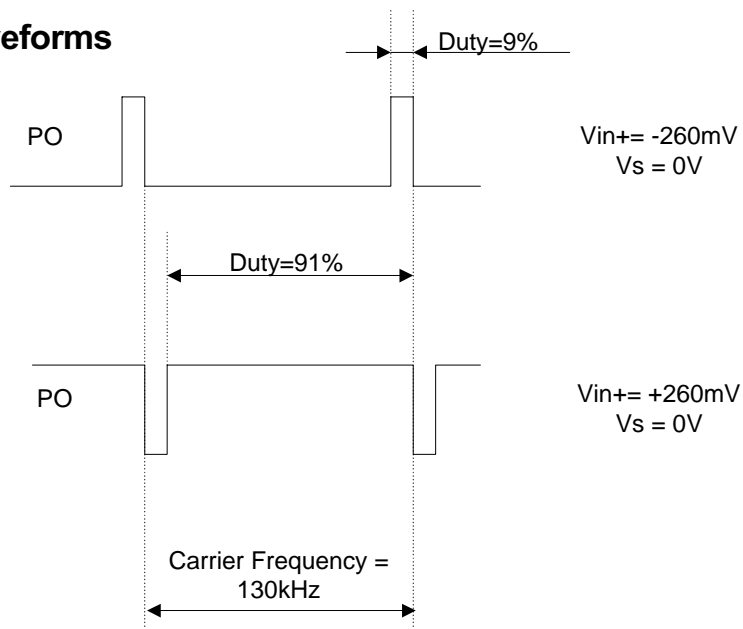


Figure 1 Output waveform

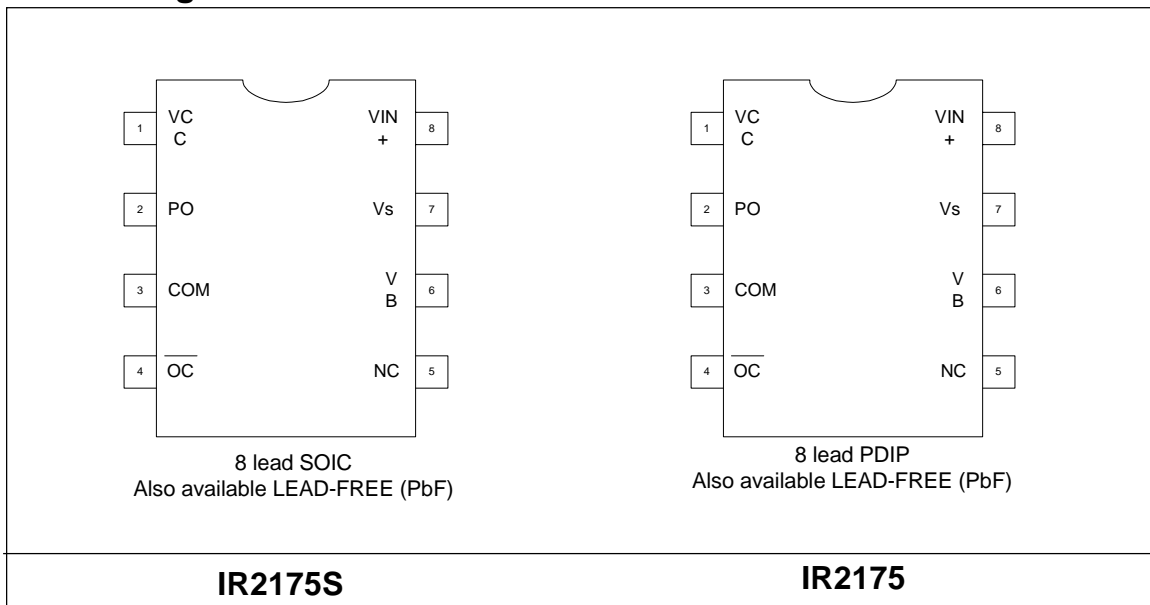
Application Hint:

Temperature drift of the output carrier frequency can be cancelled by measuring both a PWM period and the on-time of PWM (Duty) at the same time. Since both periods vary in the same direction, computing the ratio between these values at each PWM period gives consistent measurement of the current feedback over the temperature drift.

Lead Definitions

Symbol	Description
V _{CC}	Low side and logic supply voltage
COM	Low side logic ground
V _{IN+}	Positive sense input
V _B	High side supply
V _S	High side return
PO	Digital PWM output
\overline{OC}	Overcurrent output (negative logic)
N.C.	No connection

Lead Assignment



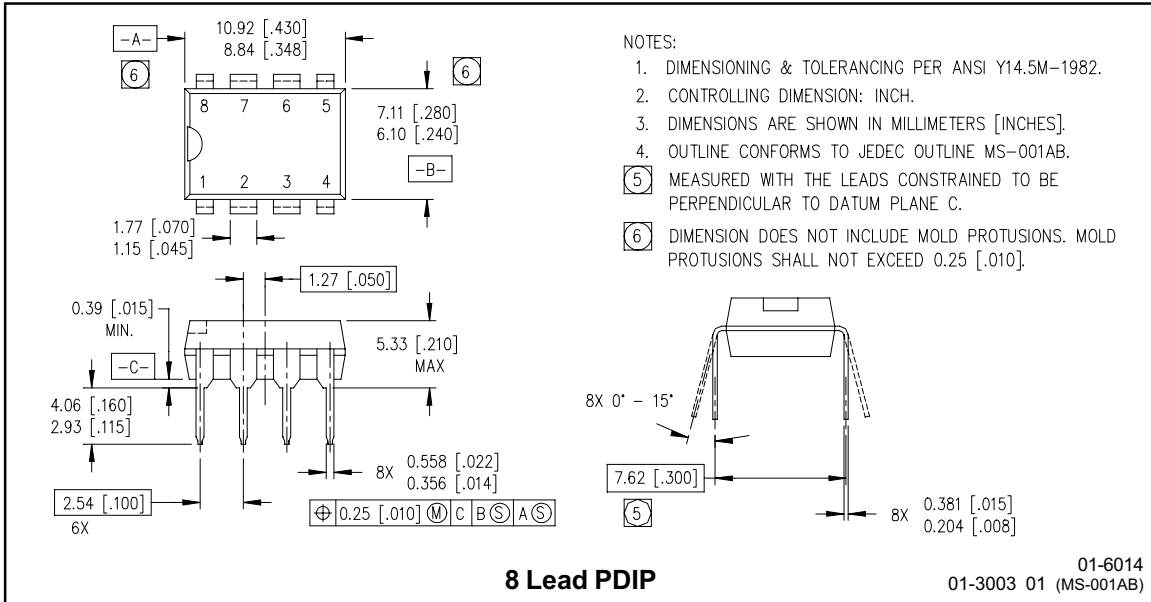
IR2175S

IR2175

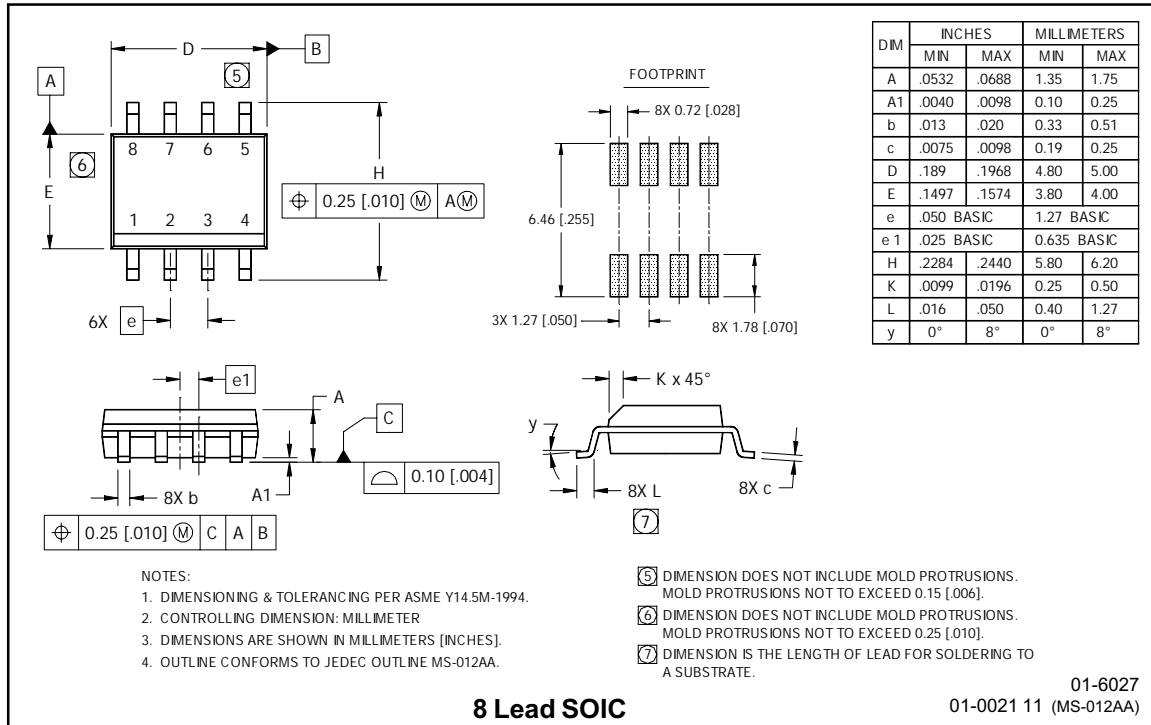
IR2175(S) & (PbF)

International
IR Rectifier

Case Outlines

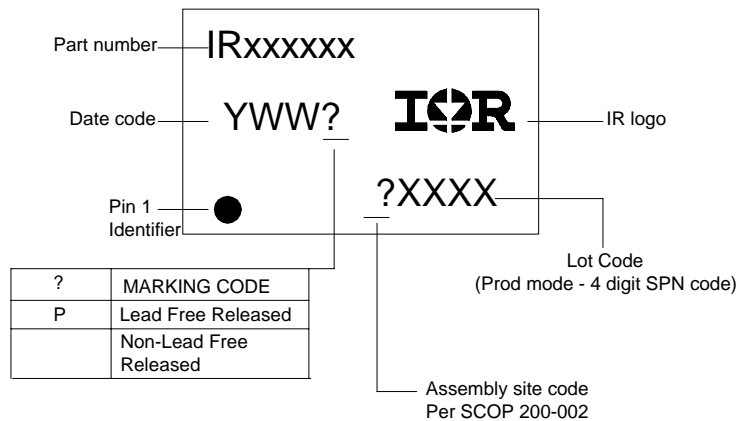


8 Lead PDIP



8 Lead SOIC

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2175 order IR2175
 8-Lead SOIC IR2175S order IR2175S

Leadfree Part

8-Lead PDIP IR2175 order IR2175PbF
 8-Lead SOIC IR2175S order IR2175SPbF