IR2130/IR2132(J)(S) & (PbF)

3-PHASE BRIDGE DRIVER

Features
- Floating channel designed for bootstrap operation
  - Fully operational to +600V
  - Tolerant to negative transient voltage
  - dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Independent half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- Cross-conduction prevention logic
- Also available LEAD-FREE

Description
The IR2130/IR2132(J)(S) is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain FAULT signal indicates if an over-current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

Product Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOFFSET</td>
<td>600V max.</td>
</tr>
<tr>
<td>IO+/−</td>
<td>200 mA / 420 mA</td>
</tr>
<tr>
<td>VOUT</td>
<td>10 - 20V</td>
</tr>
<tr>
<td>ton/off (typ.)</td>
<td>675 &amp; 425 ns</td>
</tr>
<tr>
<td>Deadtime (typ.)</td>
<td>2.5 µs (IR2130)</td>
</tr>
<tr>
<td></td>
<td>0.8 µs (IR2132)</td>
</tr>
</tbody>
</table>

Packages

- 28-Lead SOIC
- 28-Lead PDIP
- 44-Lead PLCC w/o 12 Leads

Typical Connection

(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

www.irf.com
## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to $V_S0$. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 50 through 53.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{B1,2,3}$</td>
<td>High Side Floating Supply Voltage</td>
<td>-0.3</td>
<td>625</td>
<td></td>
</tr>
<tr>
<td>$V_{S1,2,3}$</td>
<td>High Side Floating Offset Voltage</td>
<td>$V_{B1,2,3} - 0.3$</td>
<td>$V_{B1,2,3} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{HO1,2,3}$</td>
<td>High Side Floating Output Voltage</td>
<td>$V_{S1,2,3} - 0.3$</td>
<td>$V_{B1,2,3} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Low Side and Logic Fixed Supply Voltage</td>
<td>-0.3</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>Logic Ground</td>
<td>$V_{CC} - 25$</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{LO1,2,3}$</td>
<td>Low Side Output Voltage</td>
<td>-0.3</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Logic Input Voltage ($HINT1,2,3$, $LINT1,2,3$ &amp; ITRIP)</td>
<td>$V_{SS} - 0.3$</td>
<td>($V_{SS} + 15$) or ($V_{CC} + 0.3$) whichever is lower</td>
<td></td>
</tr>
<tr>
<td>$V_{FLT}$</td>
<td>FAULT Output Voltage</td>
<td>$V_{SS} - 0.3$</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{CAO}$</td>
<td>Operational Amplifier Output Voltage</td>
<td>$V_{SS} - 0.3$</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{CA-}$</td>
<td>Operational Amplifier Inverting Input Voltage</td>
<td>$V_{SS} - 0.3$</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$dV_{S}/dt$</td>
<td>Allowable Offset Supply Voltage Transient</td>
<td>—</td>
<td>50</td>
<td>V/ns</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Package Power Dissipation @ $T_A \leq +25°C$</td>
<td>—</td>
<td>1.5</td>
<td>W</td>
</tr>
<tr>
<td>$R_{thJA}$</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td>—</td>
<td>83</td>
<td>°C/W</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction Temperature</td>
<td>—</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_S$</td>
<td>Storage Temperature</td>
<td>-55</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>$T_L$</td>
<td>Lead Temperature (Soldering, 10 seconds)</td>
<td>—</td>
<td>300</td>
<td></td>
</tr>
</tbody>
</table>

### Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to $V_S0$. The $V_S$ offset rating is tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figure 54.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{B1,2,3}$</td>
<td>High Side Floating Supply Voltage</td>
<td>$V_{S1,2,3} + 10$</td>
<td>$V_{B1,2,3} + 20$</td>
<td></td>
</tr>
<tr>
<td>$V_{S1,2,3}$</td>
<td>High Side Floating Offset Voltage</td>
<td>Note 1</td>
<td>600</td>
<td></td>
</tr>
<tr>
<td>$V_{HO1,2,3}$</td>
<td>High Side Floating Output Voltage</td>
<td>$V_{S1,2,3}$</td>
<td>$V_{B1,2,3}$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Low Side and Logic Fixed Supply Voltage</td>
<td>10</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>Logic Ground</td>
<td>-5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>$V_{LO1,2,3}$</td>
<td>Low Side Output Voltage</td>
<td>0</td>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Logic Input Voltage ($HINT1,2,3$, $LINT1,2,3$ &amp; ITRIP)</td>
<td>$V_{SS}$</td>
<td>$V_{SS} + 5$</td>
<td></td>
</tr>
<tr>
<td>$V_{FLT}$</td>
<td>FAULT Output Voltage</td>
<td>$V_{SS}$</td>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$V_{CAO}$</td>
<td>Operational Amplifier Output Voltage</td>
<td>$V_{SS}$</td>
<td>$V_{SS} + 5$</td>
<td></td>
</tr>
<tr>
<td>$V_{CA-}$</td>
<td>Operational Amplifier Inverting Input Voltage</td>
<td>$V_{SS}$</td>
<td>$V_{SS} + 5$</td>
<td></td>
</tr>
<tr>
<td>$T_A$</td>
<td>Ambient Temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note 1: Logically operational for $V_S$ of ($V_{S0} - 5V$) to ($V_{S0} + 600V$). Logic state held for $V_S$ of ($V_{S0} - 5V$) to ($V_{S0} - V_{BS}$).

Note 2: All input pins, CA- and CAO pins are internally clamped with a 5.2V zener diode.
## Dynamic Electrical Characteristics

\( V_{\text{BIAS}} (V_{\text{CC}}, V_{\text{BS}1,2,3}) = 15V, V_{S0,1,2,3} = V_{SS}, C_L = 1000 \text{ pF} \) and \( T_A = 25^\circ C \) unless otherwise specified. The dynamic electrical characteristics are defined in Figures 3 through 5.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Figure</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{on}} )</td>
<td>Turn-On Propagation Delay</td>
<td>11</td>
<td>500</td>
<td>675</td>
<td>850</td>
<td>ns</td>
<td>( V_{\text{IN}} = 0 ) &amp; 5V</td>
</tr>
<tr>
<td>( I_{\text{off}} )</td>
<td>Turn-Off Propagation Delay</td>
<td>12</td>
<td>300</td>
<td>425</td>
<td>550</td>
<td>ns</td>
<td>( V_{S1,2,3} = 0 ) to 600V</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Turn-On Rise Time</td>
<td>13</td>
<td>—</td>
<td>80</td>
<td>125</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( t_f )</td>
<td>Turn-Off Fall Time</td>
<td>14</td>
<td>—</td>
<td>35</td>
<td>55</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{ITRIP}} )</td>
<td>ITRIP to Output Shutdown Prop. Delay</td>
<td>15</td>
<td>400</td>
<td>660</td>
<td>920</td>
<td>ns</td>
<td>( V_{\text{IN}}, V_{\text{ITRIP}} = 0 ) &amp; 5V</td>
</tr>
<tr>
<td>( I_{\text{IH}} )</td>
<td>ITRIP Blanking Time</td>
<td>—</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{ILH}} )</td>
<td>ITRIP to FAULT Indication Delay</td>
<td>16</td>
<td>335</td>
<td>590</td>
<td>845</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{ILH,in}} )</td>
<td>Input Filter Time (All Six Inputs)</td>
<td>—</td>
<td>—</td>
<td>310</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{ILH,clear}} )</td>
<td>LINT1,2,3 to FAULT Clear Time</td>
<td>17</td>
<td>6.0</td>
<td>9.0</td>
<td>12.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( \tau_{\text{ON}} )</td>
<td>Deadtime (IR2130)</td>
<td>18</td>
<td>1.3</td>
<td>2.5</td>
<td>3.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( \tau_{\text{OFF}} )</td>
<td>Deadtime (IR2132)</td>
<td>19</td>
<td>0.4</td>
<td>0.8</td>
<td>1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( \tau_{t_{\text{trip}}} )</td>
<td>ITRIP to Output Shutdown Propagation Delay</td>
<td>20</td>
<td>4.4</td>
<td>6.2</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( \tau_{\text{SR+}} )</td>
<td>Operational Amplifier Slew Rate (+)</td>
<td>21</td>
<td>4.4</td>
<td>6.2</td>
<td>—</td>
<td>V/\mu s</td>
<td></td>
</tr>
<tr>
<td>( \tau_{\text{SR-}} )</td>
<td>Operational Amplifier Slew Rate (-)</td>
<td>22</td>
<td>2.4</td>
<td>3.2</td>
<td>—</td>
<td>V/\mu s</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** For high side PWM, HIN pulse width must be \( \geq 1.5 \mu \text{sec} \)

## Static Electrical Characteristics

\( V_{\text{BIAS}} (V_{\text{CC}}, V_{\text{BS}1,2,3}) = 15V, V_{S0,1,2,3} = V_{SS} \) and \( T_A = 25^\circ C \) unless otherwise specified. The \( V_{\text{IN}}, V_{\text{TH}} \) and \( I_{\text{IN}} \) parameters are referenced to \( V_{SS} \) and are applicable to all six logic input leads: \( \text{HIN1,2,3} \) \& \( \text{LIN1,2,3} \). The \( V_O \) and \( I_O \) parameters are referenced to \( V_{S0,1,2,3} \) and are applicable to the respective output leads: \( \text{HO1,2,3} \) or \( \text{LO1,2,3} \).

<table>
<thead>
<tr>
<th>Symbol</th>
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<th>Figure</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{IH}} )</td>
<td>Logic 0' Input Voltage (OUT = LO)</td>
<td>23</td>
<td>400</td>
<td>490</td>
<td>580</td>
<td>mV</td>
<td>( V_{\text{IN}} = 0V, I_O = 0A )</td>
</tr>
<tr>
<td>( V_{\text{IL}} )</td>
<td>Logic 1' Input Voltage (OUT = HI)</td>
<td>24</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mV</td>
<td>( V_{\text{IN}} = 5V, I_O = 0A )</td>
</tr>
<tr>
<td>( V_{\text{OLH}} )</td>
<td>High Level Output Voltage, ( V_{\text{BIAS}} ) - VO</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mV</td>
<td>( V_{\text{IN}} = 0V ) or 5V</td>
</tr>
<tr>
<td>( V_{\text{OLL}} )</td>
<td>Low Level Output Voltage, VO</td>
<td>26</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>( V_B = V_S = 600V )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{ILK}} )</td>
<td>Offset Supply Leakage Current</td>
<td>27</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>( V_B = V_S = 600V )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{QBS}} )</td>
<td>Quiescent VBS Supply Current</td>
<td>28</td>
<td>—</td>
<td>4.0</td>
<td>0.8</td>
<td>mA</td>
<td>( V_{\text{IN}} = 0V ) or 5V</td>
</tr>
<tr>
<td>( I_{\text{QCC}} )</td>
<td>Quiescent VCC Supply Current</td>
<td>29</td>
<td>—</td>
<td>—</td>
<td>3.0</td>
<td>mA</td>
<td>( V_{\text{IN}} = 0V ) or 5V</td>
</tr>
<tr>
<td>( I_{\text{IN}} )</td>
<td>Logic 1' Input Bias Current (OUT = HI)</td>
<td>30</td>
<td>450</td>
<td>650</td>
<td>950</td>
<td>( V_B = V_S = 600V )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{IN}} )</td>
<td>Logic 0' Input Bias Current (OUT = LO)</td>
<td>31</td>
<td>225</td>
<td>400</td>
<td>600</td>
<td>( V_B = V_S = 600V )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{ITRIP+}} )</td>
<td>&quot;High&quot; ITRIP Bias Current</td>
<td>32</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>nA</td>
<td>ITRIP = 5V</td>
</tr>
<tr>
<td>( I_{\text{ITRIP-}} )</td>
<td>&quot;Low&quot; ITRIP Bias Current</td>
<td>33</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>nA</td>
<td>ITRIP = 0V</td>
</tr>
<tr>
<td>( V_{\text{BSUV+}} )</td>
<td>VBS Supply Undervoltage Positive Going Threshold</td>
<td>34</td>
<td>7.5</td>
<td>8.35</td>
<td>9.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{BSUV-}} )</td>
<td>VBS Supply Undervoltage Negative Going Threshold</td>
<td>35</td>
<td>7.1</td>
<td>7.95</td>
<td>8.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{CCUV+}} )</td>
<td>VCC Supply Undervoltage Positive Going Threshold</td>
<td>36</td>
<td>8.3</td>
<td>9.0</td>
<td>9.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{CCUV-}} )</td>
<td>VCC Supply Undervoltage Negative Going Threshold</td>
<td>37</td>
<td>8.0</td>
<td>8.7</td>
<td>9.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{ON,FLT}} )</td>
<td>FAULT Low On-Resistance</td>
<td>38</td>
<td>—</td>
<td>55</td>
<td>75</td>
<td>( \Omega )</td>
<td></td>
</tr>
</tbody>
</table>
## Static Electrical Characteristics -- Continued

\( V_{BIAS} (V_{CC}, V_{BS1,2,3}) = 15V, V_{SS0,1,2,3} = V_{SS} \) and \( T_A = 25^\circ C \) unless otherwise specified. The \( V_{IN} \), \( V_{TH} \) and \( I_{IN} \) parameters are referenced to \( V_{SS} \) and are applicable to all six logic input leads: \( HIN1,2,3 \) & \( LIN1,2,3 \). The \( VO \) and \( IO \) parameters are referenced to \( V_{SS0,1,2,3} \) and are applicable to the respective output leads: \( HO1,2,3 \) or \( LO1,2,3 \).

### Table: Static Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Figure</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( IO^+ )</td>
<td>Output High Short Circuit Pulsed Current</td>
<td>38</td>
<td>200</td>
<td>250</td>
<td>—</td>
<td>mA</td>
<td>( V_O = 0V, V_{IN} = 0V ) ( PW \leq 10 \mu s )</td>
</tr>
<tr>
<td>( IO^- )</td>
<td>Output Low Short Circuit Pulsed Current</td>
<td>39</td>
<td>420</td>
<td>500</td>
<td>—</td>
<td>mA</td>
<td>( V_{CA} = 15V, V_{IN} = 5V ) ( PW \leq 10 \mu s )</td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>Operational Amplifier Input Offset Voltage</td>
<td>40</td>
<td>—</td>
<td>20</td>
<td>30</td>
<td>mV</td>
<td>( V_{CA} = 0.2V ) ( V_{SS} = V_{CA} )</td>
</tr>
<tr>
<td>( I_{CA} )</td>
<td>CA- Input Bias Current</td>
<td>41</td>
<td>—</td>
<td>—</td>
<td>4.0</td>
<td>nA</td>
<td>( V_{CA} = 2.5V )</td>
</tr>
<tr>
<td>( CMRR )</td>
<td>Op. Amp. Common Mode Rejection Ratio</td>
<td>42</td>
<td>60</td>
<td>80</td>
<td>—</td>
<td>dB</td>
<td>( V_{SS} = V_{CA} = 0.1V, 5V ) ( V_{CA} = 0.2V ) ( V_{SS} = V_{CA} )</td>
</tr>
<tr>
<td>( PSRR )</td>
<td>Op. Amp. Power Supply Rejection Ratio</td>
<td>43</td>
<td>55</td>
<td>75</td>
<td>—</td>
<td>—</td>
<td>( V_{SS} = V_{CA} = 0.2V ) ( V_{SS} = V_{CA} ) ( V_{SS} = V_{CA} )</td>
</tr>
<tr>
<td>( V_{OH,AMP} )</td>
<td>Op. Amp. High Level Output Voltage</td>
<td>44</td>
<td>5.0</td>
<td>5.2</td>
<td>5.4</td>
<td>V</td>
<td>( V_{CA} = 0V, V_{SS} = 1V )</td>
</tr>
<tr>
<td>( V_{OL,AMP} )</td>
<td>Op. Amp. Low Level Output Voltage</td>
<td>45</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>mV</td>
<td>( V_{CA} = 1V, V_{SS} = 0V )</td>
</tr>
<tr>
<td>( I_{SRC,AMP} )</td>
<td>Op. Amp. Output Source Current</td>
<td>46</td>
<td>2.3</td>
<td>4.0</td>
<td>—</td>
<td>mA</td>
<td>( V_{CA} = 0.1V, 5V ) ( V_{CA} = 0.2V ) ( V_{SS} = V_{CA} )</td>
</tr>
<tr>
<td>( I_{SRC,AMP} )</td>
<td>Op. Amp. Output Sink Current</td>
<td>47</td>
<td>1.0</td>
<td>2.1</td>
<td>—</td>
<td>mA</td>
<td>( V_{CA} = 0V, 5V ) ( V_{CA} = 1V ) ( V_{SS} = V_{CA} )</td>
</tr>
<tr>
<td>( IO^+,AMP )</td>
<td>Operational Amplifier Output High Short Circuit Current</td>
<td>48</td>
<td>4.5</td>
<td>6.5</td>
<td>—</td>
<td>mA</td>
<td>( V_{CA} = 0.1V, 5V ) ( V_{CA} = 0.2V ) ( V_{SS} = V_{CA} )</td>
</tr>
<tr>
<td>( IO^-,AMP )</td>
<td>Operational Amplifier Output Low Short Circuit Current</td>
<td>49</td>
<td>3.2</td>
<td>5.2</td>
<td>—</td>
<td>mA</td>
<td>( V_{CA} = 0V, 5V ) ( V_{CA} = 1V ) ( V_{SS} = V_{CA} )</td>
</tr>
</tbody>
</table>

### Lead Assignments

- **28 Lead PDIP**
- **44 Lead PLCC w/o 12 Leads**
- **28 Lead SOIC (Wide Body)**

**Part Number**

**IR2130 / IR2132**

**IR2130J / IR2132J**

**IR2130S / IR2132S**
**IR2130/IR2132(J)(S) & (PbF)**

**Functional Block Diagram**

- **HIN1,2,3**: Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
- **LIN1,2,3**: Logic inputs for low side gate driver output (LO1,2,3), out of phase
- **FAULT**: Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
- **VCC**: Low side and logic fixed supply
- **ITRIP**: Input for over-current shutdown
- **CAO**: Output of current amplifier
- **CA-**: Negative input of current amplifier
- **VSS**: Logic ground
- **VB1,2,3**: High side floating supplies
- **HO1,2,3**: High side gate drive outputs
- **VS1,2,3**: High side floating supply returns
- **LO1,2,3**: Low side gate drive outputs
- **VS0**: Low side return and positive input of current amplifier

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Figure 1. Input/Output Timing Diagram

Figure 2. Floating Supply Voltage Transient Test Circuit

Figure 3. Deadtime Waveform Definitions

Figure 4. Input/Output Switching Time Waveform Definitions
Figure 5. Overcurrent Shutdown Switching Time Waveform Definitions

Figure 5.5 Input Filter Function

Figure 6. Diagnostic Feedback Operational Amplifier Circuit
IR2130/IR2132(J)(S) & (PbF)

Figure 7. Operational Amplifier Slew Rate Measurement

$$SR_+ = \frac{\Delta V}{\Delta T_1}$$
$$SR_- = \frac{\Delta V}{\Delta T_2}$$

Figure 8. Operational Amplifier Input Offset Voltage Measurement

$$V_{OS} = \frac{V_{CAO}}{21} - 0.2V$$

Figure 9. Operational Amplifier Common Mode Rejection Ratio Measurements

Measure $V_{CAO1}$ at $V_{S0} = 0.1V$
Measure $V_{CAO2}$ at $V_{S0} = 5V$

$$CMRR = -20 \cdot \log \left( \frac{|V_{CAO1} - 0.1V| - (V_{CAO2} - 5V)|}{4.9V} \right) \text{ (dB)}$$

Figure 10. Operational Amplifier Power Supply Rejection Ratio Measurements

Measure $V_{CAO1}$ at $V_{CC} = 10V$
Measure $V_{CAO2}$ at $V_{CC} = 20V$

$$PSRR = -20 \cdot \log \left( \frac{|V_{CAO1} - V_{CAO2}|}{(10V) (21)} \right)$$

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**Figure 11A. Turn-On Time vs. Temperature**

- **Temperature (°C):** -50 to 125
- **Turn-On Delay Time (µs):** 0.00 to 1.50

**Figure 11B. Turn-On Time vs. Supply Voltage**

- **VBIAS Supply Voltage (V):** 10 to 20
- **Turn-On Delay Time (µs):** 0.00 to 1.50

**Figure 11C. Turn-On Time vs. Voltage**

- **Input Voltage (V):** 0 to 6
- **Turn-On Delay Time (µs):** 0.00 to 1.50

**Figure 12A. Turn-Off Time vs. Temperature**

- **Temperature (°C):** -50 to 125
- **Turn-Off Delay Time (µs):** 0.00 to 1.00

**Figure 12B. Turn-Off Time vs. Supply Voltage**

- **VBIAS Supply Voltage (V):** 10 to 20
- **Turn-Off Delay Time (µs):** 0.00 to 1.00

**Figure 12C. Turn-Off Time vs. Input Voltage**

- **Input Voltage (V):** 0 to 6
- **Turn-Off Delay Time (µs):** 0.00 to 1.50
IR2130/IR2132(J)(S) & (PbF)

Figure 13A. Turn-On Rise Time vs. Temperature

Figure 13B. Turn-On Rise Time vs. Voltage

Figure 14A. Turn-Off Fall Time vs. Temperature

Figure 14B. Turn-Off Fall Time vs. Voltage

Figure 15A. ITRIP to Output Shutdown Time vs. Temperature

Figure 15B. ITRIP to Output Shutdown Time vs. Voltage
Figure 16A. ITRIP to FAULT Indication Time vs. Temperature

Figure 16B. ITRIP to FAULT Indication Time vs. Voltage

Figure 17A. LIN1,2,3 to FAULT Clear Time vs. Temperature

Figure 17B. LIN1,2,3 to FAULT Clear Time vs. Voltage

Figure 18A. Deadtime vs. Temperature (IR2130)

Figure 18B. Deadtime vs. Voltage (IR2130)
Figure 18C. Deadtime vs. Temperature (IR2132)

Figure 18D. Deadtime vs. Voltage (IR2132)

Figure 19A. Amplifier Slew Rate (+) vs. Temperature

Figure 19B. Amplifier Slew Rate (+) vs. Voltage

Figure 20A. Amplifier Slew Rate (-) vs. Temperature

Figure 20B. Amplifier Slew Rate (-) vs. Voltage
Figure 21A. Logic “0” Input Threshold vs. Temperature

Figure 20B. Logic “0” Input Threshold vs. Voltage

Figure 22A. Logic “1” Input Threshold vs. Temperature

Figure 22B. Logic “1” Input Threshold vs. Voltage

Figure 23A. ITRIP Input Positive Going Threshold vs. Temperature

Figure 23B. ITRIP Input Positive Going Threshold vs. Voltage
IR2130/IR2132(J)(S) & (PbF)

Figure 24A. High Level Output vs. Temperature

Figure 24B. High Level Output vs. Voltage

Figure 25A. Low Level Output vs. Temperature

Figure 25B. Low Level Output vs. Voltage

Figure 26A. Offset Supply Leakage Current vs. Temperature

Figure 26B. Offset Supply Leakage Current vs. Voltage
Figure 27A. VBS Supply Current vs. Temperature

Figure 27B. VBS Supply Current vs. Voltage

Figure 28A. VCC Supply Current vs. Temperature

Figure 28B. VCC Supply Current vs. Voltage

Figure 29A. Logic “1” Input Current vs. Temperature

Figure 29B. Logic “1” Input Current vs. Voltage
IR2130/IR2132(J)(S) & (PbF)

Figure 30A. Logic “0” Input Current vs. Temperature

Figure 30B. Logic “0” Input Current vs. Voltage

Figure 31A. “High” ITRIP Current vs. Temperature

Figure 31B. “High” ITRIP Current vs. Voltage

Figure 32A. “Low” ITRIP Current vs. Temperature

Figure 32B. “Low” ITRIP Current vs. Voltage
Figure 33. VBS Undervoltage (+) vs. Temperature

Figure 34. VBS Undervoltage (-) vs. Temperature

Figure 35. VCC Undervoltage (+) vs. Temperature

Figure 36. VCC Undervoltage (-) vs. Temperature

Figure 37A. FAULT Low On Resistance vs. Temperature

Figure 37B. FAULT Low On Resistance vs. Voltage
Figure 41A. CA- Input Current vs. Temperature

Figure 41B. CA- Input Current vs. Voltage

Figure 42A. Amplifier CMRR vs. Temperature

Figure 42B. Amplifier CMRR vs. Voltage

Figure 43A. Amplifier PSRR vs. Temperature

Figure 43B. Amplifier PSRR vs. Voltage
Figure 47A. Amplifier Output Sink Current vs. Temperature

Figure 47B. Amplifier Output Sink Current vs. Voltage

Figure 48A. Amplifier Output High Short Circuit Current vs. Temperature

Figure 48B. Amplifier Output High Short Circuit Current vs. Voltage

Figure 49A. Amplifier Output Low Short Circuit Current vs. Temperature

Figure 49B. Amplifier Output Low Short Circuit Current vs. Voltage
Figure 55. IR2130J/IR2132J
$T_J$ vs. Frequency (IRGPC20KD2)
$R_{GATE} = 33\, \Omega$, $V_{CC} = 15\, V$

Figure 56. IR2130J/IR2132J
$T_J$ vs. Frequency (IRGPC30KD2)
$R_{GATE} = 20\, \Omega$, $V_{CC} = 15\, V$

Figure 57. IR2130J/IR2132J
$T_J$ vs. Frequency (IRGPC40KD2)
$R_{GATE} = 15\, \Omega$, $V_{CC} = 15\, V$

Figure 58. IR2130J/IR2132J
$T_J$ vs. Frequency (IRGPC50KD2)
$R_{GATE} = 10\, \Omega$, $V_{CC} = 15\, V$
**IR2130/IR2132(J)(S) & (PbF)**

**Case outline**

**NOTES**

2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, A, 0- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE. 
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.25MM [.010].

**44-Lead PLCC w/o 12 leads**

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[Diagram of 44-Lead PLCC w/o 12 leads]
LEADFREE PART MARKING INFORMATION

ORDER INFORMATION

Basic Part (Non-Lead Free)
28-Lead PDIP IR2130 order IR2130
28-Lead SOIC IR2130S order IR2130S
28-Lead PDIP IR2132 order IR2132
28-Lead SOIC IR2132S order IR2132S
44-Lead PLCC IR2130J order IR2130J
44-Lead PLCC IR2132J order IR2132J

Leadfree Part
28-Lead PDIP IR2130 order IR2130PbF
28-Lead SOIC IR2130S order IR2130SPbF
28-Lead PDIP IR2132 order IR2132PbF
28-Lead SOIC IR2132S order IR2132SPbF
44-Lead PLCC IR2130J order IR2130JPbF
44-Lead PLCC IR2132J order IR2132JPbF

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245  Tel: (310) 252-7105
This product has been qualified per industrial level
Data and specifications subject to change without notice.  4/2/2004

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