**Features**

- Floating channel designed for bootstrap operation
  - Fully operational to +600V
  - Tolerant to negative transient voltage
  - dV/dt immune
- Gate drive supply range from 10 to 20V (IR2106(4))
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs (IR2106)
- Also available LEAD-FREE

**Description**

The IR2106(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.
## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_B )</td>
<td>High side floating absolute voltage</td>
<td>-0.3</td>
<td>625</td>
<td>( V )</td>
</tr>
<tr>
<td>( V_S )</td>
<td>High side floating supply offset voltage</td>
<td>( V_B - 25 )</td>
<td>( V_B + 0.3 )</td>
<td></td>
</tr>
<tr>
<td>( V_{HO} )</td>
<td>High side floating output voltage</td>
<td>( V_S - 0.3 )</td>
<td>( V_B + 0.3 )</td>
<td></td>
</tr>
<tr>
<td>( V_{CC} )</td>
<td>Low side and logic fixed supply voltage</td>
<td>-0.3</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>( V_{LO} )</td>
<td>Low side output voltage</td>
<td>-0.3</td>
<td>( V_{CC} + 0.3 )</td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Logic input voltage</td>
<td>( V_{SS} - 0.3 )</td>
<td>( V_{CC} + 0.3 )</td>
<td></td>
</tr>
<tr>
<td>( V_{SS} )</td>
<td>Logic ground (IR21064 only)</td>
<td>( V_{CC} - 25 )</td>
<td>( V_{CC} + 0.3 )</td>
<td></td>
</tr>
<tr>
<td>( dV_S/dt )</td>
<td>Allowable offset supply voltage transient</td>
<td>—</td>
<td>50</td>
<td>( V/\text{ns} )</td>
</tr>
<tr>
<td>( P_D )</td>
<td>Package power dissipation @ ( T_A \leq +25^\circ C )</td>
<td>—</td>
<td>1.0</td>
<td>( W )</td>
</tr>
<tr>
<td></td>
<td>(8 lead PDIP)</td>
<td>—</td>
<td>0.625</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(8 lead SOIC)</td>
<td>—</td>
<td>1.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(14 lead PDIP)</td>
<td>—</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(14 lead SOIC)</td>
<td>—</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>( R_{thJA} )</td>
<td>Thermal resistance, junction to ambient</td>
<td>—</td>
<td>125</td>
<td>( ^\circ \text{C/W} )</td>
</tr>
<tr>
<td></td>
<td>(8 lead PDIP)</td>
<td>—</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(8 lead SOIC)</td>
<td>—</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(14 lead PDIP)</td>
<td>—</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(14 lead SOIC)</td>
<td>—</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td>( T_J )</td>
<td>Junction temperature</td>
<td>—</td>
<td>150</td>
<td>( ^\circ \text{C} )</td>
</tr>
<tr>
<td>( T_S )</td>
<td>Storage temperature</td>
<td>-50</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>( T_L )</td>
<td>Lead temperature (soldering, 10 seconds)</td>
<td>—</td>
<td>300</td>
<td></td>
</tr>
</tbody>
</table>
Recommended Operating Conditions
The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The $V_S$ and $V_{SS}$ offset rating are tested with all supplies biased at 15V differential.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VB</td>
<td>High side floating supply absolute voltage IR2106(4)</td>
<td>$V_S + 10$</td>
<td>$V_S + 20$</td>
<td>V</td>
</tr>
<tr>
<td>$V_S$</td>
<td>High side floating supply offset voltage</td>
<td>Note 1</td>
<td>600</td>
<td></td>
</tr>
<tr>
<td>$V_{HO}$</td>
<td>High side floating output voltage</td>
<td>$V_S$</td>
<td>$V_B$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Low side and logic fixed supply voltage IR2106(4)</td>
<td>10</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>$V_{LO}$</td>
<td>Low side output voltage</td>
<td>0</td>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Logic input voltage</td>
<td>$V_{SS}$</td>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>Logic ground (IR21064 only)</td>
<td>-5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>$T_A$</td>
<td>Ambient temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note 1: Logic operational for $V_S$ of -5 to +600V. Logic state held for $V_S$ of -5V to $V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics
$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V, $V_{SS}$ = COM, $C_L$ = 1000 pF, $T_A$ = 25°C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{on}$</td>
<td>Turn-on propagation delay</td>
<td>—</td>
<td>220</td>
<td>300</td>
<td>nsec</td>
<td>$V_S = 0V$</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Turn-off propagation delay</td>
<td>—</td>
<td>200</td>
<td>280</td>
<td></td>
<td>$V_S = 0V$ or 600V</td>
</tr>
<tr>
<td>$MT$</td>
<td>Delay matching, HS &amp; LS turn-on/off</td>
<td>—</td>
<td>0</td>
<td>30</td>
<td>nsec</td>
<td></td>
</tr>
<tr>
<td>$t_{r}$</td>
<td>Turn-on rise time</td>
<td>—</td>
<td>150</td>
<td>220</td>
<td></td>
<td>$V_S = 0V$</td>
</tr>
<tr>
<td>$t_{f}$</td>
<td>Turn-off fall time</td>
<td>—</td>
<td>50</td>
<td>80</td>
<td></td>
<td>$V_S = 0V$</td>
</tr>
</tbody>
</table>
### Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}, V_{BS}$) = 15V, $V_{SS}$ = COM and $T_A = 25^\circ$C unless otherwise specified. The $V_{IL}$, $V_{IH}$ and $I_{IN}$ parameters are referenced to $V_{SS}/$COM and are applicable to the respective input leads. The $V_O$, $I_O$ and $R_{on}$ parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Logic “1” input voltage (IR2106(4))</td>
<td>2.9</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>$V_{CC} = 10V$ to $20V$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic “0” input voltage (IR2106(4))</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>$I_O = 20$ mA</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High level output voltage, $V_{BIAS} - V_O$</td>
<td>—</td>
<td>0.8</td>
<td>1.4</td>
<td>mA</td>
<td>$V_O = 20$ mA</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low level output voltage, $V_O$</td>
<td>—</td>
<td>0.3</td>
<td>0.6</td>
<td>mA</td>
<td>$V_O = 20$ mA</td>
</tr>
<tr>
<td>$I_{ILK}$</td>
<td>Offset supply leakage current</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>mA</td>
<td>$V_B = V_S = 600$V</td>
</tr>
<tr>
<td>$I_{QBS}$</td>
<td>Quiescent $V_{BS}$ supply current</td>
<td>20</td>
<td>75</td>
<td>130</td>
<td>mA</td>
<td>$V_{IN} = 0V$ or $5V$</td>
</tr>
<tr>
<td>$I_{QCC}$</td>
<td>Quiescent $V_{CC}$ supply current</td>
<td>60</td>
<td>120</td>
<td>180</td>
<td>mA</td>
<td>$V_{IN} = 0V$ or $5V$</td>
</tr>
<tr>
<td>$I_{IN}^+$</td>
<td>Logic “1” input bias current $V_{IN} = 5V$ (IR2106(4))</td>
<td>—</td>
<td>5</td>
<td>20</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}^-$</td>
<td>Logic “0” input bias current $V_{IN} = 0V$ (IR2106(4))</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV+}$</td>
<td>$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold</td>
<td>8.0</td>
<td>8.9</td>
<td>9.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV-}$</td>
<td>$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold</td>
<td>7.4</td>
<td>8.2</td>
<td>9.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUVH}$</td>
<td>Hysteresis</td>
<td>0.3</td>
<td>0.7</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{O+}$</td>
<td>Output high short circuit pulsed current</td>
<td>120</td>
<td>200</td>
<td>—</td>
<td>mA</td>
<td>$V_O = 0V$, $PW \leq 10 \mu$s</td>
</tr>
<tr>
<td>$I_{O-}$</td>
<td>Output low short circuit pulsed current</td>
<td>250</td>
<td>350</td>
<td>—</td>
<td>mA</td>
<td>$V_O = 15V$, $PW \leq 10 \mu$s</td>
</tr>
</tbody>
</table>
**IR2106(S) & (PBF)**

**Lead Definitions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIN</td>
<td>Logic input for high side gate driver output (HO), in phase</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low side gate driver output (LO), in phase</td>
</tr>
<tr>
<td>VSS</td>
<td>Logic Ground (IR21064 only)</td>
</tr>
<tr>
<td>VB</td>
<td>High side floating supply</td>
</tr>
<tr>
<td>HO</td>
<td>High side gate drive output</td>
</tr>
<tr>
<td>VS</td>
<td>High side floating supply return</td>
</tr>
<tr>
<td>VCC</td>
<td>Low side and logic fixed supply</td>
</tr>
<tr>
<td>LO</td>
<td>Low side gate drive output</td>
</tr>
<tr>
<td>COM</td>
<td>Low side return</td>
</tr>
</tbody>
</table>

**Lead Assignments**

**8 Lead PDIP**

- **IR2106**
  - 1: VCC
  - 2: HIN
  - 3: LIN
  - 4: COM
  - 8: VB
  - 7: HO
  - 6: VS
  - 5: LO

- **IR2106S**
  - 1: VCC
  - 2: HIN
  - 3: LIN
  - 4: COM
  - 8: VB
  - 7: HO
  - 6: VS
  - 5: LO

**14 Lead PDIP**

- **IR21064**
  - 1: VCC
  - 2: HIN
  - 3: LIN
  - 4: VSS
  - 5: COM
  - 6: LO
  - 7: VB
  - 8: HO
  - 9: VS
  - 10: VSS
  - 11: COM
  - 12: LO
  - 13: VB
  - 14: HO

- **IR21064S**
  - 1: VCC
  - 2: HIN
  - 3: LIN
  - 4: VSS
  - 5: COM
  - 6: LO
  - 7: VB
  - 8: HO
  - 9: VS
  - 10: VSS
  - 11: COM
  - 12: LO
  - 13: VB
  - 14: HO
Figure 1. Input/Output Timing Diagram

Figure 2. Switching Time Waveform Definitions

Figure 3. Delay Matching Waveform Definitions
Figure 4A. Turn-on Propagation Delay vs. Temperature

Figure 4B. Turn-on Propagation Delay vs. Supply Voltage

Figure 5A. Turn-off Propagation Delay vs. Temperature

Figure 5B. Turn-off Propagation Delay vs. Supply Voltage
Figure 6A. Turn-on Rise Time vs. Temperature

Figure 6B. Turn-on Rise Time vs. Supply Voltage

Figure 7A. Turn-off Fall Time vs. Temperature

Figure 7B. Turn-off Fall Time vs. Supply Voltage
Figure 8A. Logic “1” Input Voltage vs. Temperature

Figure 8B. Logic “1” Input Voltage vs. Supply Voltage

Figure 9A. Logic “0” Input Voltage vs. Temperature

Figure 9B. Logic “0” Input Voltage vs. Supply Voltage
Figure 10A. High Level Output Voltage vs. Temperature

Figure 10B. High Level Output Voltage vs. Supply Voltage

Figure 11A. Low Level Output Voltage vs. Temperature

Figure 11B. Low Level Output Voltage vs. Supply Voltage
IR2106(4)(S) & (PBF)

Figure 12A. Offset Supply Leakage Current vs. Temperature

Figure 12B. Offset Supply Leakage Current vs. Supply Voltage

Figure 13A. VGS Supply Current vs. Temperature

Figure 13B. VGS Supply Current vs. Supply Voltage
Figure 14A. Quiescent VCC Supply Current vs. Temperature

Figure 14B. Quiescent VCC Supply Current vs. VCC Supply Voltage

Figure 15A. Logic “1” Input Current vs. Temperature

Figure 15B. Logic “1” Bias Current vs. Supply Voltage
Figure 16A. Logic “0” Input Current vs. Temperature

Figure 16B. Logic “0” Input Current vs. Supply Voltage

Figure 17. VCC Undervoltage Threshold (+) vs. Temperature

Figure 18. VCC Undervoltage Threshold (-) vs. Temperature
Figure 19. VBS Undervoltage Threshold (+) vs. Temperature

Figure 20. VBS Undervoltage Threshold (-) vs. Temperature

Figure 21A. Output Source Current vs. Temperature

Figure 21B. Output Source Current vs. Supply Voltage
IR2106(4)(S) & (PBF)

Figure 22A. Output Sink Current vs. Temperature

Figure 22B. Output Sink Current vs. Supply Voltage

Figure 23. Maximum V<sub>S</sub> Negative Offset vs. Supply Voltage

Figure 24. IR2106 vs. Frequency (IRFBC20), R<sub>gate</sub>=33Ω, VCC=15V
Figure 25. IR2106 vs. Frequency (IRFBC30),
$R_{gate}=22\,\Omega$, $V_{cc}=15\,V$

Figure 26. IR2106 vs. Frequency (IRFBC40),
$R_{gate}=15\,\Omega$, $V_{cc}=15\,V$

Figure 27. IR2106 vs. Frequency (IRFPE50),
$R_{gate}=10\,\Omega$, $V_{cc}=15\,V$

Figure 28. IR21064 vs. Frequency (IRFBC20),
$R_{gate}=33\,\Omega$, $V_{cc}=15\,V$
Figure 29. IR21064 vs. Frequency (IRFBC30), $R_{\text{gate}}=22\,\Omega$, $V_{\text{CC}}=15\,\text{V}$

Figure 30. IR21064 vs. Frequency (IRFBC40), $R_{\text{gate}}=15\,\Omega$, $V_{\text{CC}}=15\,\text{V}$

Figure 31. IR21064 vs. Frequency (IRFPE50), $R_{\text{gate}}=10\,\Omega$, $V_{\text{CC}}=15\,\text{V}$

Figure 32. IR21064S vs. Frequency (IRFBC20), $R_{\text{gate}}=33\,\Omega$, $V_{\text{CC}}=15\,\text{V}$
Figure 33. IR2106S vs. Frequency (IRFBC30),
\( R_{\text{gate}} = 22\Omega, V_{CC} = 15\text{V} \)

Figure 34. IR2106S vs. Frequency (IRFBC40),
\( R_{\text{gate}} = 15\Omega, V_{CC} = 15\text{V} \)

Figure 35. IR2106S vs. Frequency (IRFPE50),
\( R_{\text{gate}} = 10\Omega, V_{CC} = 15\text{V} \)

Figure 36. IR2106S vs. Frequency (IRFBC20),
\( R_{\text{gate}} = 33\Omega, V_{CC} = 15\text{V} \)
Figure 37. IR21064S vs. Frequency (IRFBC30), $R_{\text{gate}}=22\,\Omega$, $V_{\text{cc}}=15V$

Figure 38. IR21064S vs. Frequency (IRFBC40), $R_{\text{gate}}=15\,\Omega$, $V_{\text{cc}}=15V$

Figure 39. IR21064S vs. Frequency (IRFPE50), $R_{\text{gate}}=10\,\Omega$, $V_{\text{cc}}=15V$
IR2106(4)(S & (PbF))

Case Outlines

NOTES:
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE ShOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS SHALL NOT EXCEED 0.25 [0.10].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
8. EXCEPT WHERE SHOWN IN MILLIMETERS, DIMENSIONS ARE SHOWN IN INCHES.

8 Lead PDIP

8 Lead SOIC

FOOTPRINT

Table:

<table>
<thead>
<tr>
<th>Dim</th>
<th>Inches</th>
<th>Millimeters</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.032</td>
<td>0.81</td>
</tr>
<tr>
<td>aA</td>
<td>0.040</td>
<td>1.02</td>
</tr>
<tr>
<td>b</td>
<td>0.020</td>
<td>0.51</td>
</tr>
<tr>
<td>c</td>
<td>0.075</td>
<td>1.91</td>
</tr>
<tr>
<td>D</td>
<td>0.189</td>
<td>4.80</td>
</tr>
<tr>
<td>E</td>
<td>0.1497</td>
<td>3.80</td>
</tr>
<tr>
<td>e</td>
<td>0.050</td>
<td>1.27</td>
</tr>
<tr>
<td>e1</td>
<td>0.025</td>
<td>0.64</td>
</tr>
<tr>
<td>e2</td>
<td>0.284</td>
<td>7.20</td>
</tr>
<tr>
<td>K</td>
<td>0.099</td>
<td>0.25</td>
</tr>
<tr>
<td>L</td>
<td>0.016</td>
<td>0.40</td>
</tr>
<tr>
<td>Y</td>
<td>0°</td>
<td>0°</td>
</tr>
</tbody>
</table>

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS.
6. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.06].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
IR2106(4)(S) & (PBF)

14 Lead PDIP

NOTES:
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONstrained TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTrUSIONS. MOLD PROTrUSIONS SHALL NOT EXCED 0.25 [.010].

14 Lead SOIC (narrow body)

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTrUSIONS. MOLD PROTrUSIONS SHALL NOT EXCEED 0.15 [.006].
LEADFREE PART MARKING INFORMATION

ORDER INFORMATION

Basic Part (Non-Lead Free)
- 8-Lead PDIP IR2106 order IR2106
- 8-Lead SOIC IR2106S order IR2106S
- 14-Lead PDIP IR21064 order IR21064
- 14-Lead SOIC IR21064S order IR21064S

Leadfree Part
- 8-Lead PDIP IR2106 order IR2106PbF
- 8-Lead SOIC IR2106S order IR2106SPbF
- 14-Lead PDIP IR21064 order IR21064PbF
- 14-Lead SOIC IR21064S order IR21064SPbF