Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic input compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs (IR2101) or out of
  phase with inputs (IR2102)
- Also available LEAD-FREE

Description

The IR2101(S)/IR2102(S) are high voltage, high speed
power MOSFET and IGBT drivers with independent
high and low side referenced output channels. Proprietary
HVIC and latch immune CMOS technologies enable
ruggedized monolithic construction. The logic
input is compatible with standard CMOS or LSTTL
output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum
driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in
the high side configuration which operates up to 600 volts.

Typical Connection

(Refer to Lead Assignments for correct pin
configuration). These diagram(s) show
electrical connections only. Please refer to
our Application Notes and DesignTips for
proper circuit board layout.
Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_B</td>
<td>High side floating supply voltage</td>
<td>-0.3</td>
<td>625</td>
<td>V</td>
</tr>
<tr>
<td>V_S</td>
<td>High side floating supply offset voltage</td>
<td>V_B - 25</td>
<td>V_B + 0.3</td>
<td></td>
</tr>
<tr>
<td>V_HO</td>
<td>High side floating output voltage</td>
<td>V_S - 0.3</td>
<td>V_B + 0.3</td>
<td></td>
</tr>
<tr>
<td>V_CC</td>
<td>Low side and logic fixed supply voltage</td>
<td>-0.3</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>V_LO</td>
<td>Low side output voltage</td>
<td>-0.3</td>
<td>V_CC + 0.3</td>
<td></td>
</tr>
<tr>
<td>V_IN</td>
<td>Logic input voltage (HIN &amp; LIN) (IR2101) &amp; (HIN &amp; LIN) (IR2102)</td>
<td>-0.3</td>
<td>V_CC + 0.3</td>
<td></td>
</tr>
<tr>
<td>dV_S/dt</td>
<td>Allowable offset supply voltage transient</td>
<td>—</td>
<td>50</td>
<td>V/ns</td>
</tr>
<tr>
<td>P_D</td>
<td>Package power dissipation @ T_A ≤ +25°C</td>
<td>—</td>
<td>1.0</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>(8 lead PDIP)</td>
<td>—</td>
<td>0.625</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(8 lead SOIC)</td>
<td>—</td>
<td>125</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>Thermal resistance, junction to ambient</td>
<td>—</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(8 lead PDIP)</td>
<td>—</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>(8 lead SOIC)</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_J</td>
<td>Junction temperature</td>
<td>—</td>
<td>300</td>
<td>°C</td>
</tr>
<tr>
<td>T_S</td>
<td>Storage temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>T_L</td>
<td>Lead temperature (soldering, 10 seconds)</td>
<td>—</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_B</td>
<td>High side floating supply absolute voltage</td>
<td>V_S + 10</td>
<td>V_S + 20</td>
<td>V</td>
</tr>
<tr>
<td>V_S</td>
<td>High side floating supply offset voltage</td>
<td>Note 1</td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>V_HO</td>
<td>High side floating output voltage</td>
<td>V_S</td>
<td>V_B</td>
<td>V</td>
</tr>
<tr>
<td>V_CC</td>
<td>Low side and logic fixed supply voltage</td>
<td>10</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>V_LO</td>
<td>Low side output voltage</td>
<td>0</td>
<td>V_CC</td>
<td>V</td>
</tr>
<tr>
<td>V_IN</td>
<td>Logic input voltage (HIN &amp; LIN) (IR2101) &amp; (HIN &amp; LIN) (IR2102)</td>
<td>0</td>
<td>V_CC</td>
<td>V</td>
</tr>
<tr>
<td>T_A</td>
<td>Ambient temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_B. (Please refer to the Design Tip DT97-3 for more details).
## Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 \text{ pF} \text{ and } T_A = 25^\circ C \text{ unless otherwise specified.}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{on}$</td>
<td>Turn-on propagation delay</td>
<td>—</td>
<td>160</td>
<td>220</td>
<td>ns</td>
<td>$V_S = 0V$</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Turn-off propagation delay</td>
<td>—</td>
<td>150</td>
<td>220</td>
<td>ns</td>
<td>$V_S = 600V$</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Turn-on rise time</td>
<td>—</td>
<td>100</td>
<td>170</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Turn-off fall time</td>
<td>—</td>
<td>50</td>
<td>90</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$MT$</td>
<td>Delay matching, HS &amp; LS turn-on/off</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

## Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V \text{ and } T_A = 25^\circ C \text{ unless otherwise specified.} \text{ The } V_{IN}, V_{TH} \text{ and } I_{IN} \text{ parameters are referenced to COM. The } V_O \text{ and } I_O \text{ parameters are referenced to COM and are applicable to the respective output leads: HO or LO.}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Logic “1” input voltage (IR2101)</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>—</td>
<td>$V_{CC} = 10V \text{ to } 20V$</td>
</tr>
<tr>
<td></td>
<td>Logic “0” input voltage (IR2102)</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>mV</td>
<td>$V_{CC} = 10V \text{ to } 20V$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic “0” input voltage (IR2101)</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>mV</td>
<td>$I_O = 0A$</td>
</tr>
<tr>
<td></td>
<td>Logic “1” input voltage (IR2102)</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>mV</td>
<td>$I_O = 0A$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High level output voltage, $V_{BIAS} - V_O$</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mV</td>
<td>$V_B = V_S = 600V$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low level output voltage, $V_O$</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mV</td>
<td>$V_{IN} = 0V \text{ or } 5V$</td>
</tr>
<tr>
<td>$I_{ILK}$</td>
<td>Offset supply leakage current</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{QBS}$</td>
<td>Quiescent $V_{BS}$ supply current</td>
<td>—</td>
<td>30</td>
<td>55</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{QCC}$</td>
<td>Quiescent $V_{CC}$ supply current</td>
<td>—</td>
<td>150</td>
<td>270</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{IN+}$</td>
<td>Logic “1” input bias current</td>
<td>—</td>
<td>3</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Logic “0” input bias current</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV+}$</td>
<td>$V_{CC}$ supply undervoltage positive going threshold</td>
<td>8</td>
<td>8.9</td>
<td>9.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV-}$</td>
<td>$V_{CC}$ supply undervoltage negative going threshold</td>
<td>7.4</td>
<td>8.2</td>
<td>9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{O+}$</td>
<td>Output high short circuit pulsed current</td>
<td>130</td>
<td>210</td>
<td>—</td>
<td>mA</td>
<td>$V_O = 0V$ $V_{IN} = \text{Logic } \text{“1”}$ $PW \leq 10 \mu s$</td>
</tr>
<tr>
<td>$I_{O-}$</td>
<td>Output low short circuit pulsed current</td>
<td>270</td>
<td>360</td>
<td>—</td>
<td>mA</td>
<td>$V_O = 15V$ $V_{IN} = \text{Logic } \text{“0”}$ $PW \leq 10 \mu s$</td>
</tr>
</tbody>
</table>
IR2101(S)/IR2102(S) & (PbF)

Functional Block Diagram

IR2101

IR2102

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## Lead Definitions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIN</td>
<td>Logic input for high side gate driver output (HO), in phase (IR2101)</td>
</tr>
<tr>
<td>HIN</td>
<td>Logic input for high side gate driver output (HO), out of phase (IR2102)</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low side gate driver output (LO), in phase (IR2101)</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low side gate driver output (LO), out of phase (IR2102)</td>
</tr>
<tr>
<td>VB</td>
<td>High side floating supply</td>
</tr>
<tr>
<td>HO</td>
<td>High side gate drive output</td>
</tr>
<tr>
<td>VS</td>
<td>High side floating supply return</td>
</tr>
<tr>
<td>VCC</td>
<td>Low side and logic fixed supply</td>
</tr>
<tr>
<td>LO</td>
<td>Low side gate drive output</td>
</tr>
<tr>
<td>COM</td>
<td>Low side return</td>
</tr>
</tbody>
</table>

## Lead Assignments

**8 Lead PDIP**

- **IR2101**
  - Pin 1: VCC
  - Pin 2: HIN
  - Pin 3: LIN
  - Pin 4: COM
  - Pin 5: LO
  - Pin 6: VS
  - Pin 7: HO
  - Pin 8: VB

- **IR2102**
  - Pin 1: VCC
  - Pin 2: HIN
  - Pin 3: LIN
  - Pin 4: COM
  - Pin 5: LO
  - Pin 6: VS
  - Pin 7: HO
  - Pin 8: VB

**8 Lead SOIC**

- **IR2101S**
  - Pin 1: VCC
  - Pin 2: HIN
  - Pin 3: LIN
  - Pin 4: COM
  - Pin 5: LO
  - Pin 6: VS
  - Pin 7: HO
  - Pin 8: VB

- **IR2102S**
  - Pin 1: VCC
  - Pin 2: HIN
  - Pin 3: LIN
  - Pin 4: COM
  - Pin 5: LO
  - Pin 6: VS
  - Pin 7: HO
  - Pin 8: VB

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IR2101(S)/IR2102(S) & (PbF)

Figure 1. Input/Output Timing Diagram

Figure 2. Switching Time Waveform Definitions

Figure 3. Delay Matching Waveform Definitions
IR2101(S)/IR2102(S) & (PbF)

Figure 6A. Turn-On Time vs Temperature

Figure 6B. Turn-On Time vs Supply Voltage

Figure 6C. Turn-On Time vs Input Voltage

Figure 7A. Turn-Off Time vs Temperature

Figure 7B. Turn-Off Time vs Supply Voltage

Figure 7C. Turn-Off Time vs Input Voltage
IR2101(S)/IR2102(S) & (PbF)

Figure 9A. Turn-On Rise Time vs Temperature

Figure 9B. Turn-On Rise Time vs Voltage

Figure 10A. Turn-Off Fall Time vs Temperature

Figure 10B. Turn-Off Fall Time vs Voltage

Figure 12A. Logic "1" Input Voltage (IR2101) Logic "0" Input Voltage (IR2102) vs Temperature

Figure 12B. Logic "1" Input Voltage (IR2101) Logic "0" Input Voltage (IR2102) vs Voltage
IR2101(S)/IR2102(S) & (PbF)

Figure 13A. Logic "0" Input Voltage (IR2101)
Logic "1" Input Voltage (IR2102) vs Temperature

Figure 13B. Logic "0" Input Voltage (IR2101)
Logic "1" Input Voltage (IR2102) vs Voltage

Figure 14A. High Level Output vs Temperature

Figure 14B. High Level Output vs Voltage

Figure 15A. Low Level Output vs Temperature

Figure 15B. Low Level Output vs Voltage
IR2101(S)/IR2102(S) & (PbF)

Figure 16A. Offset Supply Current vs Temperature

Figure 16B. Offset Supply Current vs Voltage

Figure 17A. VBS Supply Current vs Temperature

Figure 17B. VBS Supply Current vs Voltage

Figure 18A. Vcc Supply Current vs Temperature

Figure 18B. Vcc Supply Current vs Voltage
IR2101(S)/IR2102(S) & (PbF)

**Figure 19A.** Logic “1” Input Current vs Temperature

**Figure 19B.** Logic “1” Input Current vs Voltage

**Figure 20A.** Logic “0” Input Current vs Temperature

**Figure 20B.** Logic “0” Input Current vs Voltage

**Figure 21A.** Vcc Undervoltage Threshold(+) vs Temperature

**Figure 21B.** Vcc Undervoltage Threshold(-) vs Temperature
IR2101(S)/IR2102(S) & (PbF)

**Output Sink Current (mA)**

**Temperature (°C)**

**Figure 23A. Output Sink Current vs Temperature**

**Output Sink Current (mA)**

**Temperature (°C)**

**Figure 23B. Output Sink Current vs Voltage**

**Output Source Current (mA)**

**Temperature (°C)**

**Figure 22A. Output Source Current vs Temperature**

**Output Source Current (mA)**

**Temperature (°C)**

**Figure 22B. Output Source Current vs Voltage**

**VBIAS Supply Voltage (V)**

**Output Source Current (mA)**

**Temperature (°C)**

**Figure 22A. Output Source Current vs Temperature**

**Output Source Current (mA)**

**Temperature (°C)**

**Figure 22B. Output Source Current vs Voltage**

**VBIAS Supply Voltage (V)**
IR2101(S)/IR2102(S) & (PbF) 8 Lead PDIP

NOTES:
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

8 Lead SOIC

NOTES:
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3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
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8 Lead SOIC

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LEADFREE PART MARKING INFORMATION

ORDER INFORMATION

Basic Part (Non-Lead Free)
8-Lead PDIP IR2101 order IR2101
8-Lead SOIC IR2101S order IR2101S
8-Lead PDIP IR2102 order IR2102
8-Lead SOIC IR2102S order IR2102S

Leadfree Part
8-Lead PDIP IR2101 order IR2101PbF
8-Lead SOIC IR2101S order IR2101SPbF
8-Lead PDIP IR2102 order IR2102PbF
8-Lead SOIC IR2102S order IR2102SPbF