ESD5V3U2U Series
Uni-directional Ultra Low ESD / Transient Protection Diode

ESD5V3U2U-03F
ESD5V3U2U-03LRH
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Revision History: Rev. 1.2, 2013-08-16

Page or Item Subjects (major changes since previous revision)

Revision 1.3, 2013-08-16

4 + 16 All marking infos for TSLP-3-7 updated

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1 Uni-directional Ultra Low ESD / Transient Protection Diode

1.1 Features

- ESD / Transient protection of High-Speed data lines exceeding
  - IEC61000-4-2 (ESD): ± 20 kV (air / contact)
  - IEC61000-4-4 (EFT): ±50 A (5/50 ns)
  - IEC61000-4-5 (surge): ±3 A (8/20 μs)
- Maximum working voltage: $V_{RWM}$ 5.3 V
- Extremely low capacitance: down to 0.4 pF
- Very low reverse current: $I_R < 1$ nA typical
- Pb-free package (RoHS compliant) and halogen free package

1.2 Application Examples

- ESD / Transient protection of High Speed Interfaces:
  - HDMI, USB 2.0/USB 3.0, DisplayPort, DVI
  - Mobile HDMI Link, MDDI, MIPI.
  - 10/100/1000 Ethernet, Firewire, S-ATA, etc.

1.3 Product Description

Figure 1-1 Pin Configuration (a) and Schematic Diagram (b)

Table 1-1 Ordering information

<table>
<thead>
<tr>
<th>Type</th>
<th>Package</th>
<th>Configuration</th>
<th>Marking code</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD5V3U2U-03F</td>
<td>PG-TSFP-3-1</td>
<td>2 lines, uni-directional¹)</td>
<td>Z1</td>
</tr>
<tr>
<td>ESD5V3U2U-03LRH</td>
<td>PG-TSLP-3-7</td>
<td>2 lines, uni-directional¹)</td>
<td>Z1</td>
</tr>
</tbody>
</table>

¹) Or 1 line, bi-directional between pins 1 and 2, if pin 3 is not connected
2 Characteristics

Table 2-1 Maximum Rating at $T_A = 25 \, ^\circ C$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD (air / contact) discharge(^1)</td>
<td>$V_{\text{ESD}}$</td>
<td>-20 -</td>
<td>20</td>
</tr>
<tr>
<td>Peak pulse current ($t_p = 8/20 , \mu s$)(^2)</td>
<td>$I_{\text{PP}}$</td>
<td>-3 -</td>
<td>3</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>$T_{\text{OP}}$</td>
<td>-40 -</td>
<td>125</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{\text{stg}}$</td>
<td>-65 -</td>
<td>150</td>
</tr>
</tbody>
</table>

1) $V_{\text{ESD}}$ according to IEC61000-4-2
2) $I_{\text{PP}}$ according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at $T_A = 25 \, ^\circ C$, unless otherwise specified

![Figure 2-1 Definitions of electrical characteristics](image-url)
Table 2-2  DC characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Reverse working voltage</td>
<td>$V_{RWM}$</td>
<td>–</td>
<td>–</td>
<td>5.3</td>
</tr>
<tr>
<td>Breakdown voltage</td>
<td>$V_{BR}$</td>
<td>6</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Reverse current</td>
<td>$I_R$</td>
<td>–</td>
<td>&lt;1</td>
<td>50</td>
</tr>
</tbody>
</table>

Table 2-3  RF characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Line capacitance$^1$</td>
<td>$C_L$</td>
<td>–</td>
<td>0.4</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>0.2</td>
<td>0.4</td>
</tr>
</tbody>
</table>

1) Total capacitance line to ground

Table 2-4  ESD Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clamping voltage$^1$</td>
<td>$V_{CL}$</td>
<td>–</td>
<td>19</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>28</td>
<td>–</td>
</tr>
<tr>
<td>Forward clamping voltage$^1$</td>
<td>$V_{FC}$</td>
<td>–</td>
<td>10</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>17</td>
<td>–</td>
</tr>
<tr>
<td>Dynamic resistance$^1$</td>
<td>$R_{DYN}$</td>
<td>–</td>
<td>0.6</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>0.4</td>
<td>–</td>
</tr>
</tbody>
</table>

1)Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50 \, \Omega$, $t_p = 100\, \text{ns}$, $t_r = 300\, \text{ps}$, averaging window: $t_1 = 30\, \text{ns}$ to $t_2 = 60\, \text{ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 10\, \text{A}$ and $I_{PP2} = 40\, \text{A}$. 
Table 2-5  Surge characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Clamping voltage</td>
<td>$V_{CL}$</td>
<td>–</td>
<td>10</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>Forward clamping voltage</td>
<td>$V_{FC}$</td>
<td>–</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>4</td>
<td>6</td>
</tr>
</tbody>
</table>

\(^{1}\) $I_{PP}$ according to IEC61000-4-5
3 Typical characteristics

Typical characteristics at $= 25 \, ^{\circ}\mathrm{C}$, unless otherwise specified

Figure 3-1  Line capacitance $C_L = f(V_R)$, from pin 1/2 to 3, $f = 1 \, \text{MHz}$

Figure 3-2  Line capacitance $C_L = f(f)$, from pin 1/2 to 3
Figure 3-3  Line capacitance $C_L = f(T_A)$

Figure 3-4  Reverse current $I_R = f(T_A)$, $V_R = 5.3\, V$, from pin 1/2 to pin 3
Figure 3-5  IEC61000-4-2: $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2 ($R = 330 \, \Omega$, $C = 150 \, pF$)

Figure 3-6  IEC61000-4-2: $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2 ($R = 330 \, \Omega$, $C = 150 \, pF$)
ESD5V3U2U Series

Typical characteristics

Figure 3-7 IEC61000-4-2: \( V_{CL} = f(t) \), 15 kV positive pulse from pin 1 to pin 2 \((R = 330 \, \Omega, C = 150 \, \text{pF})\)

![Figure 3-7](image)

- \( V_{CL-\text{max-peak}} = 104.8 \, [V] \)
- \( V_{CL-30\text{ns-peak}} = 24.1 \, [V] \)

Scope: 20 GS/s

Figure 3-8 IEC61000-4-2: \( V_{CL} = f(t) \), 15 kV negative pulse from pin 1 to pin 2 \((R = 330 \, \Omega, C = 150 \, \text{pF})\)

![Figure 3-8](image)

- \( V_{CL-\text{max-peak}} = -105.1 \, [V] \)
- \( V_{CL-30\text{ns-peak}} = -13.7 \, [V] \)

Scope: 20 GS/s
Clamping voltage (TLP): $I_{\text{TLP}} = f(V_{\text{TLP}})$ according ANSI/ESD STM5.5.1- Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50 \ \Omega$, $t_p = 100 \ \text{ns}$, $t_r = 0.6 \ \text{ns}$, $I_{\text{TLP}}$ and $V_{\text{TLP}}$ averaging window: $t_1 = 30 \ \text{ns}$ to $t_2 = 60 \ \text{ns}$, extraction of dynamic resistance using squares fit to ELP characteristic between $I_{\text{TLP1}} = 10 \ \text{A}$ and $I_{\text{TLP2}} = 30 \ \text{A}$. Please refer to Application Note AN210 [1]
4 Application Information

Figure 4-1 2 lines, uni-directional TVS protection

Figure 4-2 1 line, bi-directional TVS protection

The protection diode should be placed very close to the location where the ESD or other transients can occur to keep loops and inductances as small as possible. Pin 3 should be connected directly to a ground plane on the board.

0.4 pF typ.

Application_ESD5V3U2U_2 lines uni-directional.vsd

Application_ESD5V3U2U_1 line bi-directional.vsd
5 Ordering information scheme (examples)

ESD 0P1 RF - XX YY

- **Package**
  - XX = Pin number (i.e.: 02 = 2 pins; 03 = 3 pins)
  - YY = Package family:
    - LS = TSSLP
    - LRH = TSLP

- **For Radio Frequency Applications**

- **Line Capacitance** $C_L$ in pF: (i.e.: 0P1 = 0.1pF)

ESD 5V3 U n U - XX YY

- **Package or Application**
  - XX = Pin number (i.e.: 02 = 2 pins; 03 = 3 pins)
  - YY = Package family:
    - LS = TSSLP
    - LRH = TSLP
    - S = SOT363
    - U = SC74

- **XX = Application family**
  - LC = Low Clamp
  - HDMI

- **U**n- / Bi-directional or **Rail to Rail protection**

- **Number of protected lines** (i.e.: 1 = 1 line; 4 = 4 lines)

- **Capacitance**:
  - Standard (>10pF), Low (<10pF), Ultra-low (<1pF)

- **Maximum working voltage** $V_{RWM}$ in V: (i.e.: 5V3 = 5.3V)

Figure 5-1 Ordering Information Scheme
6 Package Information

6.1 PG-TSFP-3-1

Figure 6-1 PG-TSFP-3-1: Package Overview

Figure 6-2 PG-TSFP-3-1: Footprint

Figure 6-3 PG-TSFP-3-1: Packing

Figure 6-4 PG-TSFP-3-1: Marking (example)
6.2 PG-TSLP-3-7

Figure 6-5 PG-TSLP-3-7: Package Overview

Figure 6-6 PG-TSLP-3-7: Footprint

Figure 6-7 PG-TSLP-3-7: Packing

Figure 6-8 PG-TSLP-3-7: Marking (example)
References
