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GATE DRIVERS

# Technical Overview of IR215x Products

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## Introduction

IR215x devices are widely used in high volume off-line, cost sensitive areas such as Electronic Ballasts, Primary and Standby AC/DC and DC/DC Power Supplies and Battery Chargers. All IR215x Control IC's integrate high voltage half-bridge drive with oscillator and all absorb the function of outmoded gate transformer and separate driver.

The most broadly applicable IR215x device is referred to as a Self-Oscillating Control IC. Table 1 lists availability and release order. Since introduction,the IR2155 has set an industry standard which has been advanced by subsequent devices, culminating in third generation products IR2153, IR2154, IR21531, IR53H series SIP hybrid modules and now the IR2157 and IR2159.

## 1. Technical Comparison of Second and Third Generation Self Oscillating Control IC's

This section shows improvements made to third generation Self-Oscillating Control IC's by direct comparison with the second generation IR2151. Key points are underlined and summarised at the end of the section. Part number IR2153 refers to all third generation ICs and IR2151 for second generation. Due to wide market acceptance, International Rectifier currently plans continued manufacture of all IR215x products. However, for new designs or upgrade to mature designs, third generation Self Oscillating Control ICs are advised on grounds of enhanced electrical performance and functionality.

**IR2153 has Increased Under Voltage Lockout Hysterisis.**

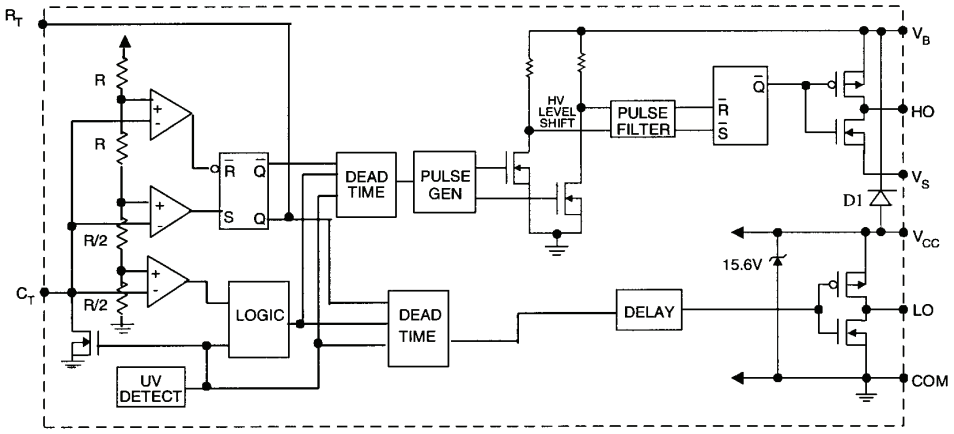
What is under-voltage lockout?

Under voltage lockout (UVLO) is the name for a protection feature built into IR2151, IR2153 and many other Control IC's from International Rectifier. This block is marked as UV detect on figure 1 and ensures that the gate drive outputs, HO and LO are both low should bias become too marginal for comfortable gate drive to the output transistors. The UVLO circuit also assures a repeatable start-up sequence and controls bias current needed for various elements of the IC. Second and third generation IR215x have one UVLO circuit, which is used to monitor the bias supply, Vcc.

**Table 1: IR215x Product Family.**

| Base # | Hybrid | Description | Oct /98; Status |
|---|---|---|---|
| IR2151 | IR51H(D)xxx | Gen.2 Self-Oscillating Control IC | Not new designs |
| IR2152 | Possible | Gen.2 Self-Oscillating Control IC | Not new designs |
| IR2153 | IR53H(D)xxx | Gen.3 Self-Oscillating Control IC | Available |
| IR2153D | Possible | Gen.3 Self-Oscillating Control IC | Available |
| IR21531 | Possible | Gen.3 Self-Oscillating Control IC | Available |
| IR21531D | Possible | Gen.3 Self-Oscillating Control IC | Available |
| IR2154 | Possible | Gen.3 Self-Oscillating Control IC | Available |
| IR2155 | No | Gen.1 Self-Oscillating Control IC | Not new designs |
| IR2157 | - - | CIC for HF.Ballast /Resonant loads | Sampling now |
| IR2159 | - - | CIC with Phase Mode Control | In Development |

**Figure 1: IR2153D Functional Block Diagram**




What is under-voltage lockout hysterisis?

Hysterisis is a technique commonly used to improve noise immunity. Instead of switching on/off at one voltage level, two threshold levels are defined; one sensitive to a rising edge and the other to a falling edge. In product data sheets describing Vcc undervoltage lockout, these two thresholds are listed as VccUV+ and VccUV-. Hysterisis is a measure of the difference between these two thresholds and is separately listed on data sheets as VccUVH. VccUV+ is the threshold at which the chip is first enabled, when Vcc is rising. Once enabled, Vcc is allowed to drop slightly without adverse effects.

How can Vcc noise be minimised?

Good local decoupling with low ESR capacitors and adequate reservoir capacitance from Vcc to COM should be used in designs based on IR2151, IR2153 and other Control IC's to minimise noise. Circuit layout is also important. Design Tip DT98-2 offers further guidance on this subject.

**IR2153 has True Micropower Start-Up.**

What is micropower start-up?

Micropower start-up means that the bias current needed when the IC is in a quiescent state (i.e. not oscillating and Vcc<VccUV) is reduced to a very low level. Figures 2 and 3 clearly show the differences in start-up bias between IR2151 and IR2153.

How will micropower start-up benefit my design?

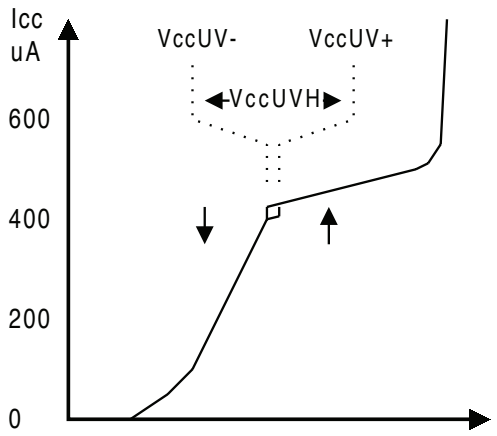
Off-line applications usually have a single resistor from a high voltage bus for start-up bias to keep component cost and complexity low. In some cases this resistor provides bias for all modes of operation (both start-up and running, where current demand is highest). However, an auxiliary low voltage source is more common for this purpose. 'Bootstrapping' is beneficial because an auxiliary supply can be derived with much higher efficiency than from a simple dropping resistor connected to the line.

In bootstrap start-up schemes, micropower feature allows the pull-up resistor value to be increased in value compared to schemes in which a single dropping resistor provides all the bias. This is because the resistor needs only to overcome quiescent bias current requirements for the IC and raise Vcc to UV+. When the IC starts oscillating, additional bias requirement is met by an auxiliary supply. The term 'bootstrap' is also used to describe the diode and Vbs capacitor arrangement shown in the typical circuit configuration for IR215x. This part of the circuit, explained by design tip DT98-2 serves a different function to the resistor in a bootstrap 'start-up' scheme.

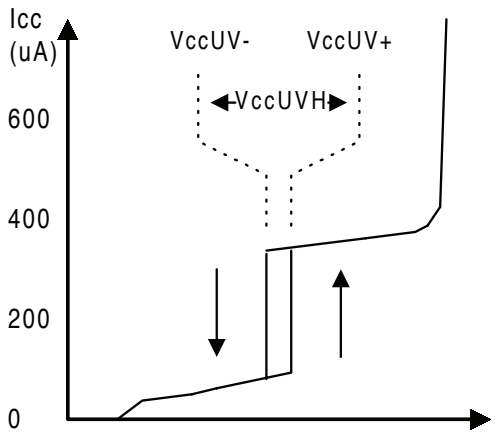
How is micropower start-up implemented on IR2153?

IR2153 and IR2151 behave slightly differently upon power-up. When using IR2151, the Rt output is held high and approximately tracks Vcc until the VccUV+ threshold is reached. The Ct pin is held low at this time and so an additional component of Vcc bias current must flow out through Rt and return to

IR2151 typical Vcc bias characteristics




IR2153 typical Vcc bias characteristics




COM through Ct. The component of current flowing through Rt and Ct during start-up is eliminated with IR2153 because Rt is low when Vcc<VccUV. Internal bias current demand of IR2153 is also lower than for IR2151, especially during start-up when Vcc < VccUV+

How can I implement an auxiliary supply and take full advantage of bootstrapping?

An auxiliary supply can be conveniently derived from a charge pump connected to the half bridge output, or from an isolated secondary winding taken from a donor transformer elsewhere in the system. An example of charge pump implementation may be taken from our compact HF ballast reference design, IRPLCFL1 or from design tip DT94-10B. Making use of an auxiliary supply reduces static power dissipation, temperature rise in the bootstrap resistor and increases circuit efficiency. This difference is significant for low power designs where start-up bias significantly impacts overall efficiency, and is more noticeable if the bus voltage is comparatively high.

**IR2153 incorporates a fast Shutdown Mode:**

What is fast shutdown and why might I need it?

Most applications call for protective action against fault conditions that would otherwise destroy output switches. Fusing is the simplest option but is often ineffective at preventing damage to semiconductors and is not self-resetting, unless comparatively more expensive devices are used. If the load is capacitively coupled or resonant in nature, for example as in most Electronic Ballast designs, ample protection may be afforded by only halting the oscillator and preventing further switching cycles. However, adequate protection sometimes calls for both FETs to be rapidly turned off.

How can shutdown be implemented when using IR2151?

Vcc must be pulled below VccUV- To turn off both FETs when using IR2151. This requirement may to an extent conflict with the need to provide a healthy charge reservoir and solid decoupling. Any IR2151 shutdown network must be capable of rapidly pulling charge from the Vcc reservoir capacitor (and the decoupling capacitor, if present). Low holding current thyristors can be used to crowbar Vcc and latch the chip off until the supply is recycled in designs based on IR2151. This approach is both simple and inexpensive but does not support automatic power-on reset. If the circuit must reset after fault condition without manual supply interruption, IR2153 is preferable as fewer peripheral components are needed.

How does the IR2153 shutdown mode work?

The IR2153 offers a convenient shutdown solution by adding a second function to the Ct pin. A third functional threshold is added to Ct and set at Vcc/6. Below this threshold a fast shutdown mode is invoked and both output buffers are set low with minimal delay. This allows a simple open-collector NPN transistor or similar to be used as part of an inexpensive pro-

tection scheme.

Can IR2153 be driven directly as a slave device, for example to complete a full bridge?

The Ct input of IR2151,2152 or 2155 can be directly fed from a square wave source provided Vct high > 2/3 Vcc and Vct low < 1/3 Vcc.The Rt output of any Self Oscillating Control IC can generate a master clock to feed directly into the Ct input of another, effectively bypassing the internal oscillator of the slaved device. This can be a useful way to implement a full bridge using just one type of IC or Hybrid. The shutdown threshold of IR2153 should be noted when it is being used in this way. Square wave drive with zero DC offset will not cause outputs to switch alternately as would be the case with IR2151, because the shutdown condition will invoke when Ct is zero, however IR2153 can still be used as a slave by adding a simple passive circuit to add a small DC offset. A design tip is planned to address master/slave applications using Self-Oscillating Control IC's.

**IR2153 has Improved Dead-Time Accuracy with Zero Average Temperature Coefficient.**

What is dead-time and why is it important?

Dead-time is the period during which both HO and LO outputs are intentionally low. This period is fixed inside the IC and serves several essential functions. The primary function of dead-time is to prevent cross conduction or shoot-through in half-bridge designs. If the load is resonant in nature, such as in electronic ballasts and resonant mode power supplies, dead-time also helps maintain zero voltage switching (ZVS). Sometimes called soft switching, this technique significantly reduces switching losses.

How does dead-time prevent cross conduction, or shoot-through?

Cross-conduction will occur in half bridge circuits if both high and low side transistors are either fully or partially on at the same time.The resulting short across the supply exacerbates EMI, increases dissipation and may destroy power switches, control IC or both if extreme. MOSFET turn on / off times are often inequal and vary in production, so dead-time offers a guard band to account for these differences. IR215x is available with various dead time options, however switching times can be easily modified using small signal diodes across series resistors in the gate drive loop if necessary.

How does dead-time help to support soft switching?

When the load is inductive or resonant, circuit effeciency is generally highest when zero voltage switching (ZVS or soft switching) occurs. In ZVS, there is just enough time when both FETs are off (approximately equal to the dead-time) to allow load energy to swing the output to the opposite rail, where current will flow in the FET body drain diode. This desirable process is called self-commutation.

Why is soft switching (ZVS) more efficient than hard switching (Why do MOSFETs become hot when the load is removed?)

Self-commutation is almost completely lossless because output capacitance of the half bridge rings with the inductive component of the load when both half bridge transistors are off. When the next transistor turns on, the voltage across it is already at or close to zero, so its internal capacitance is already discharged. When its load is not resonant or inductive in nature, the output cannot self-commutate to the opposite rail during off time, so the voltage across the next transistor to turn on is high. It must therefore discharge its own output capacitance in addition to providing load current. This explains why half bridge transistors often get hot when there is no load at all or in ballasts, when the lamp is removed and the oscillator is allowed to continue running.

What is the optimum value of dead-time?

If ZVS is required but the dead-time is too short, there is insufficient time for the half-bridge output voltage to completely self-commutate to the opposite rail. This leaves a fraction of the bus voltage remaining across the output capacitance of both transistors which the next transistor to switch on must disharge. This is partial hard switching (or partial soft switching). Conversely, if the dead-time is too long, the output voltage will self-commutate to the opposite rail, but a short time later, the load current will reverse or ring, producing a voltage transient. Again, the result is partial hard switching and less

than optimal switching efficiency. For ZVS, optimal dead time occurs when there is just enough time for self commutation to occur. IR2153 is available with several dead-time options to help meet this requirement. If further adjustments are necessary, small signal diodes can be used in the gate drive loop to independantly change charge/discharge timing.

How does improved dead-time performance of IR2153 benefit my circuit?

IR2153 has a stringent specification for dead-time and has a zero average coefficient of temperature. This can be important for production repeatability and more easily supports ZVS under variable temperature conditions.

**IR2153 output buffers have a reduced di/dt output stage**

What is a reduced di/dt output stage?

This means that the peak rate of change of current (rate of current rise, and fall for turn-on and turn-off has been deliberately reduced. In effect the 2153 output buffers are turned on and off more slowly than with IR2151.

What are the benefits of reduced di/dt in the gate drive circuit?

Benefits of reduced di/dt output buffers include lower gate ringing (Vgs overshoot / undershoot) from combination of di/dt and gate circuit parasitics. In some cases gate resistors can

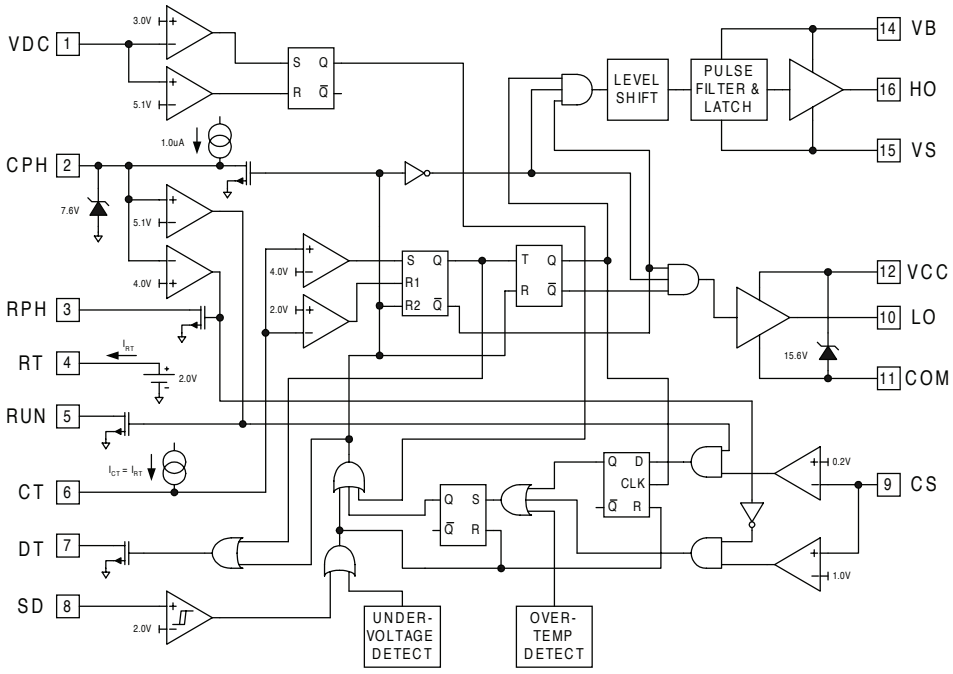
**Table 2: Parametric Comparison of IR2153 and IR2151**

Typical values @ Ta=25 C are listed unless stated otherwise

| Parameter | IR2151(D)(S)<br>IR51H(D)xxx | IR2153(D)(S)<br>IR53H(D)xxx | IR21531<br>IR531H(D)xxx |
|---|---|---|---|
| Quiescent Bias, Iqcc | 400uA + Vcc/Rt (Rt=Vcc; Ct=0V during start-up) | 150uA (Rt=0; Ct=0V during start-up) | 150uA (Rt=0; Ct=0V during start-up) |
| UVLO Thresholds<br>VccUV+<br>VccUV-<br>VccUVH | <br>8.5V<br>8.1V<br>0.4V | <br>9.0V<br>8.0V<br>1.0V | <br>9.0V<br>8.0V<br>1.0V |
| Shudown Method | Vcc < VccUV- | Vcc < VccUV-<br>*OR* Ct < Vcc/6 | Vcc < VccUV-<br>*OR* Ct < Vcc/6 |
| Dead-Time, Td<br>Typical<br>Min,Max<br>Temp. Coeffecient | <br>1.2 uSec<br>0.5, 2.25 uSec<br>+5000 ppm / C | <br>1.2 uSec<br>0.75, 1.65 uSec<br>+/- 1000 ppm / C | <br>0.6 uSec<br>See Data Sheet<br>+/- 1000 ppm / C |
| Output Buffer di/dt Typical | 0.3A / 20nS | 0.3A / 70nS | 0.3A / 70nS |

Note:
Data shown in this table is subject to change. Please consult latest product data sheets for latest specifications

**Figure 4 : IR2157 Block Diagram**




be eliminated altogether, however this depends on several factors such as layout and transistor type used. RF interference may also be reduced.

Will reduced di/dt increase switching loss and lower efficiency?

Provided a suitable series gate resistor is selected, efficiency will not be impaired. Peak output buffer current capability of IR2153 is comparable with IR2151 and so similar size FET's or IGBT's may be controlled without detrimental switching characteristics.

## 3. The IR2157 as an Advanced Variable Frequency Control IC

What is the IR2157?

The IR2157 Control IC is primarily intended to act as the core of a high frequency Electronic Ballast. The device Integrates a variable frequency oscillator, control functions and half-bridge drive delivering extremely low component count, reliability and reduced manufacturing costs. However many of the features incorporated in the IR2157 will benefit other applications, especially when resonant loads are involved. In this respect, the device can be categorised as an advanced Self-Oscillating Control IC suitable for more general application areas.

What applications suit the IR2157?

Beyond the primary use as an Electronic Ballast control IC, the IR2157 will demonstrate advantages in several applications where a variable frequency half bridge drive is required. For example, resonant mode circuits require frequency modulation and are increasingly found in high performance AC/DC power supplies.

As an advanced Self-Oscillating Control IC, how does IR2157 compare with IR2153?

In addition to IR2153 features noted in the prior section, the IR2157 offers the following enhancements for designs using resonant or inductive loads.

· Dynamically programmable dead-time

· Precise 50% duty cycle
· Variable frequency oscillator with sequential state control logic
· Programmable, high frequency start
· Fault shutdown with auto-restart

What is the advantage of dynamically programmable dead-time?

Self-Oscillating Control IC's such as IR2153 are available with several dead time options, however this parameter is fixed on-chip for all 8-pin ICs. IR2157 dead-time may be programmed with a single resistor and can therefore be tailored to the optimum value for zero-voltage switching or to meet other requirements.The control signal is ground referenced, so dynamic modulation of dead-time is convenient.

Why is the duty cycle precisely set at 50%?

When driving capacitively coupled resonant loads, such as the series-resonant load circuit of an Electronic Ballast, it is often important to maintain duty cycle at 50%. Departure from this duty ratio can couple a low frequency 'envelope' to the resonant load through the comparatively low impedance DC blocking capacitor.The resulting low-frequency modulation produces unwanted harmonics in the load and may saturate magnetics, if sufficiently extreme.

The IR2157 achieves 50% duty cycle by operating the oscillator at twice the frequency of other Self-Oscillating Control IC's. A T-type toggle flip-flop is used prior to the drive stage to accomplish this. 50% duty cycle can be maintained with IR2153, however precise control becomes difficult in practice with these parts if variable frequency is also required. Design-tip DT98-1 details this topic.

In what ways are the oscillator of IR2153 and IR2157 different?

The oscillator onboard Control IC's such as IR2153 is similar in some ways to the industry standard '555, except that the timing capacitor of IR2153 is both charged and discharged from the same pin. In applications that require fixed frequency 50% duty cycle the circuit is completed using a timing resistor connected between the oscillator output pin, Rt and the top plate of the timing capacitor. The Rt pin can source and sink current and under normal loading switches between Vcc and COM. A different approach is adopted by IR2157 in which a highly stable on-chip current mirror is used to derive charging current for the timing capacitor.

With IR2157, timing capacitor discharging occurs via a separate path to ground that does not involve the current mirror and this period controls dead-time. The sum of these two periods determines the run frequency. Charging time is controlled only by current flowing to ground (sink current) so frequency may be controlled with a programmable, ground referenced current sink. This can be practically implemented with a simple n-channel MOSFET or small signal bipolar transistor.

In Electronic Ballast application, the IR2157 oscillator is controlled by onboard state control logic. This logic drives integrated open-drain switches to connect resistors or simple R/C networks to ground at the appropriate time. This process can be duplicated using common emitter connected transistors controlled by an external circuit. Closed-loop regulation can also be achieved in this way using an opamp or a linear programmable shunt such as 3-pin TO-92 packaged TL431.

What is the benefit of programmable, high frequency start?

The IR2157 state logic provides a programmable duration, high frequency start. This is useful in cases where the resonant load is coupled to the half bridge through a DC blocking capacitor. Initial operation well above the resonant point ensures low current flow in the primarily inductive resonant tank circuit. This helps to eliminate unwanted spikes, saturation of magnetic components and allows time for the DC blocking capacitor to acquire static charge necessary for steady state operation.

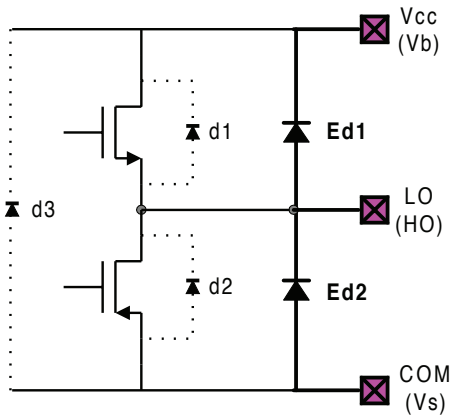
## 3. ESD, Latch Immunity and Hidden Value within IR Control ICs

What is ESD and what can it do?

Static charge is something we're all familiar with. A form of potential energy generated by friction between moving materials and gases such as air and stored on both objects and people. Electro Static Discharge occurs when this stored charge finds a path through the IC, either by direct contact with pins or indirectly via dielectric breakdown (spark) usually through air. In manufacturing environments, devices are

generally at greatest risk from ESD damage during handling or automatic insertion when they are removed from packaging but not yet electrically connected with the remainder of the system. When soldered in place, semiconductors are usually reasonably well protected because potential conducting paths through the chip are often bridged. Left Unchecked, ESD can produce effects ranging from slight parameter shifts to complete destruction and all levels of damage between these two extremes.

**Figure 5 : Simplified Parasitic Structure of CMOS IC Output Buffer**




What can be done to reduce the risk of damage from ESD?

Anti-Static precautions and working regime should always form the primary barrier against ESD because these actions tackle the issue at source. However, all semiconductor manufacturers can influence ESD immunity of their product, though there is usually an additional cost associated with higher levels of protection. International Rectifier applies extremely conservative design margins and special circuit design techniques to maximise ESD immunity. Though ESD is given separate consideration, design philosophies adopted to increase latch-up immunity further benefit ESD reselience.

What is CMOS latch-up?

As in circuit design, building blocks used to create any IC inherently contain parasitic elements that occur consequentially rather than by choice. For example, MOSFETs always contain a parasitic diode between drain and source. Parasitic elements can be useful, irrelevant or disadvantageous, depending on where and what they are used for in circuit. Common to the basic building blocks of all CMOS IC's is an undesirable parasitic structure that can latch in the conducting state in a similar way to an SCR (thyristor) under some abnormal circumstances. Latch-up is a failure mode that is said to occur if the SCR shown in figure 1 is triggered. It can be avoided by careful design of both the IC itself and peripheral circuitry.

What can happen as a result of CMOS latch-up?

During latch-up in any CMOS IC uncontrolled currents can flow within the IC through the parasitic SCR structure. This can cause permanent damage to the chip, loss of functionality or undefined behavior. If latch-up occurs when bias is derived from a weak supply which would easily collapse under abnormal loading, the IC may recover when the bias supply is recycled, however cummulative damage or undefined operation are still possible under these circumstances. Also possible is a situation in which the IC is destroyed as a second order effect. For example: Undefined operation ->MOSFET damage -> IC damage.

How does International Rectifier add value in CMOS latch-up prevention?

As with ESD immunity measures, all semiconductor manufacturers can influence latch immunity of their product, though there is usually an additional cost associated with higher levels of protection. International Rectifier applies extremely conservative design margins and special circuit techniques to maximise latch immunity. Though latch immunity is given separate consideration, design philosophies adopted to increase ESD immunity further benefit latch-up reselience. Output buffers used in International Rectifier Control ICs provide latch immunity to +/- 500mA. This is considered to be an excellent level of protection.