Innovative CooliR^{2}™ Packaging Platform with Dual-Sided Cooling Advances HEVs and EVs Progress

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International Rectifier

Innovative CooliR^{2}™ Packaging Platform

AGENDA

- HEV/EV power electronics challenges
- CooliRIGBT™, CooliRDiode™- Application specific semiconductor devices
- CooliR^{2}™ - Paradigm shift in packaging technology
    - "Building block" approach
    - Electrical performance improvements
    - Thermal performance improvements
    - Increased reliability
    - High power density
- Conclusions

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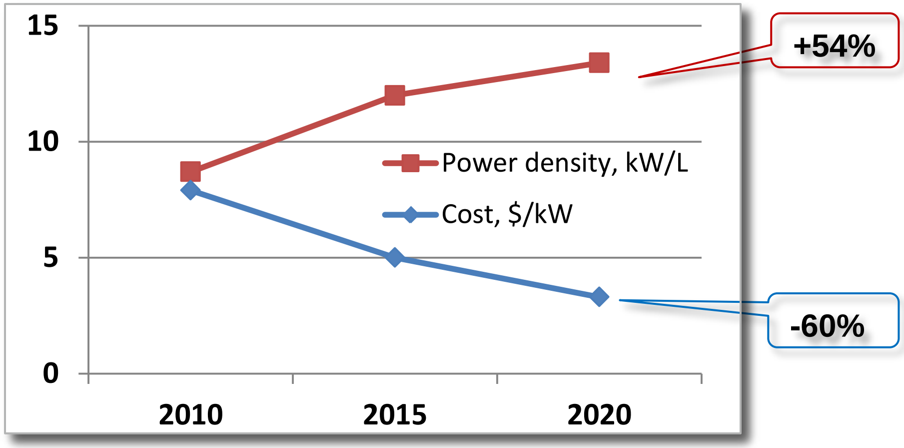
Challenges for the HEV and EV traction inverters

General trends and requirements for HEV/EV power electronics

Size, volume	↓
Weight	↓
Cost	↓
Reliability	↑



USCAR targets

	R&D Status	Targets		Change
	2010	2015	2020	
Coolant Temperature	90 °C	105 °C	105 °C	**+ 15 °C**
Cost, $/kW	<7.9	<5.0	<3.3	**> - 60%**
Specific power, kW/kg	>10.8	>12.0	>14.1	**> +30%**
Power density, kW/L	>8.7	>12.0	>13.4	**> +54%**

Source: The United States Council for Automotive Research LLC (USCAR)—U.S. DRIVE Electrical & Electronics Tech Team (EETT).

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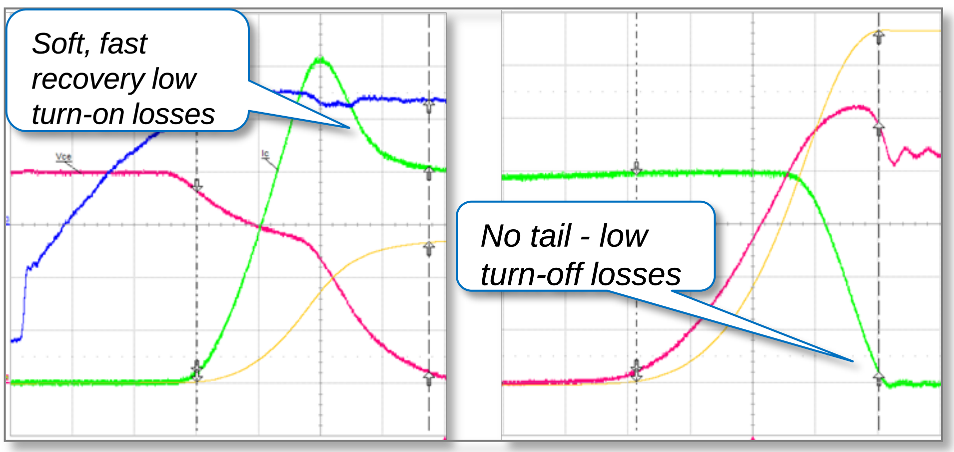
A comprehensive and innovative approach is needed to address the challenges of modern HEV/EV inverters.

International Rectifier's ***CooliR™*** *high-power packaging platform addresses all challenges.*

Typical switching waveforms

Turn-on Turn-off



Vdc = 400V, Ic = 400A, 100ns/div

Optimized devices for inverters

CooliRIGBT™ and CooliRDiode™

- **Large die** (e.g. IGBT – 12x12 mm)
- **Reduced conduction and switching losses**
  - Switching frequency up to 20kHz
- **Robust**
  - High breakdown voltage 680V
  - Increased temperature $Tj_{MAX} = 175^oC$
  - Short circuit capability 6us
  - Square RBSOA
- **Wirebondless interconnection**
  - Solderable Front Metal (SFM)
- **Dual-sided cooling**

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COOLiR²™ Packaging Platform for HEV/EV Inverters

Objective:

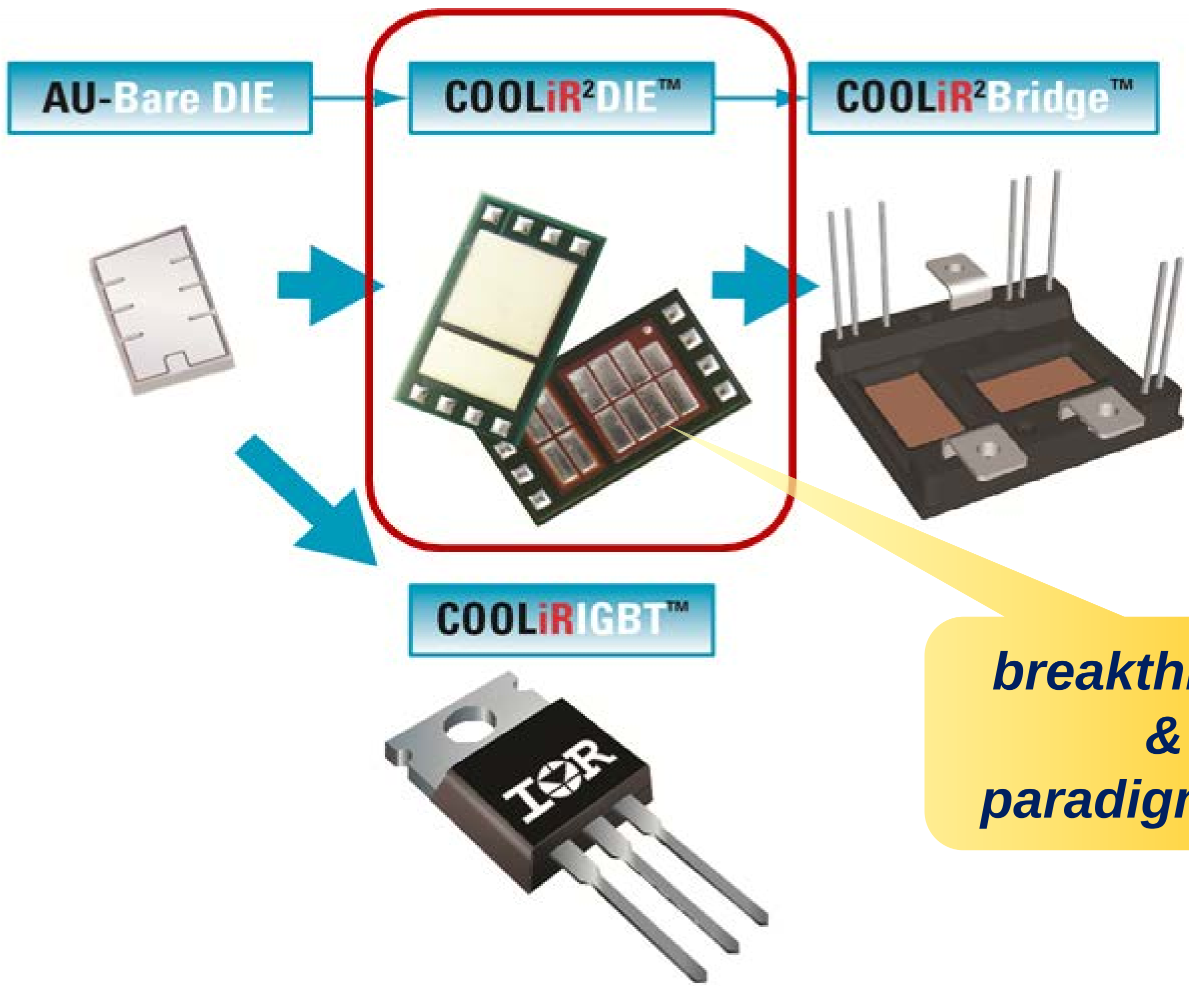
Create an innovative power semiconductor packaging concept

- *optimized for HEV/EV traction inverter applications*
- *maximizing the utilization of semiconductor devices*

Performance objective	Design goal
High current density	High current interconnections
High power density	Effective heat removal
Max. utilization of voltage rating	Low inductance
Low losses	Fast switching speed
High operating temperature	Increased max. junction temperature

COOLiR²™ Packaging Platform for HEV/EV Inverters

Packaging Levels:	1. Bare DIE	2. Packaged DIE	3. Module



breakthrough
&
paradigm shift

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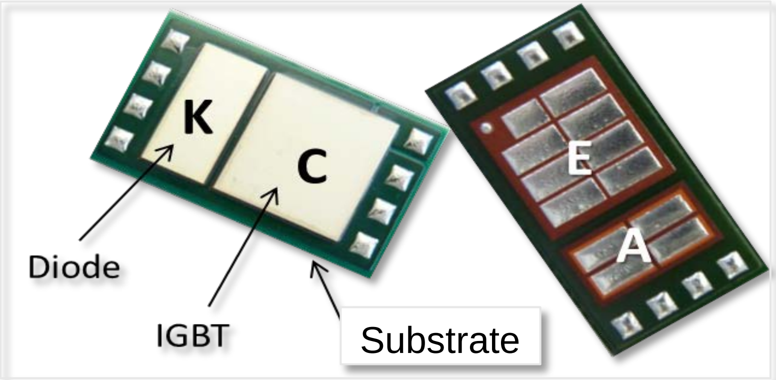
COOLiR²™ Packaging Platform for HEV/EV Inverters

CooliR²Die™ - very large die "discrete" SMT component



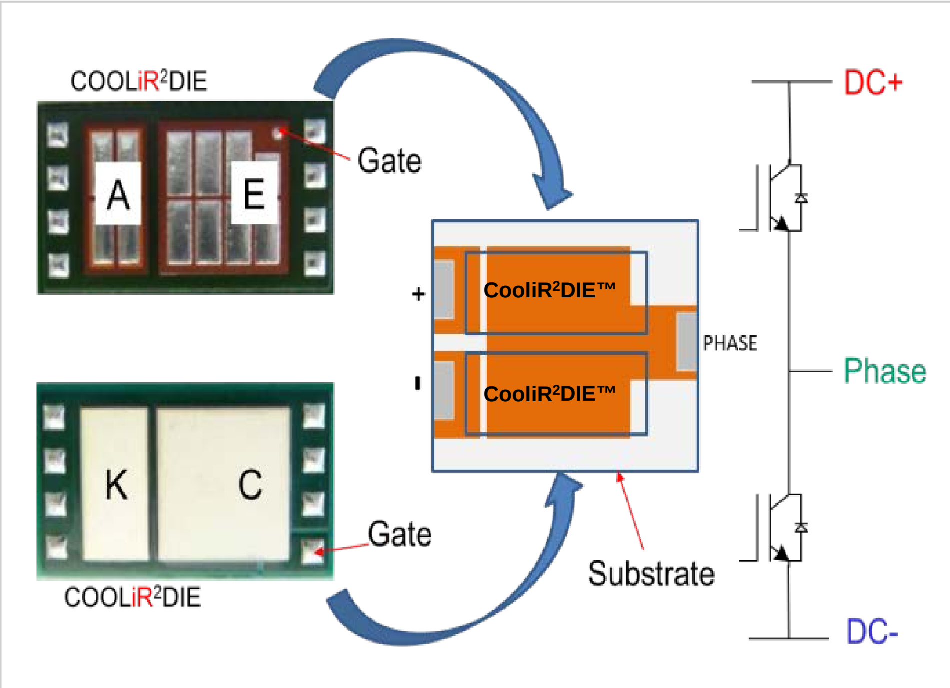
- The 680V/300A CooliR²Die™ package dimensions: **12.5mm x 29mm x 1mm**
- Two types of CooliR²DIE™ developed to simplify construction of different power circuit topologies
- Different substrates (e.g. DBC) can be used as the carrier for the CooliR²DIE™

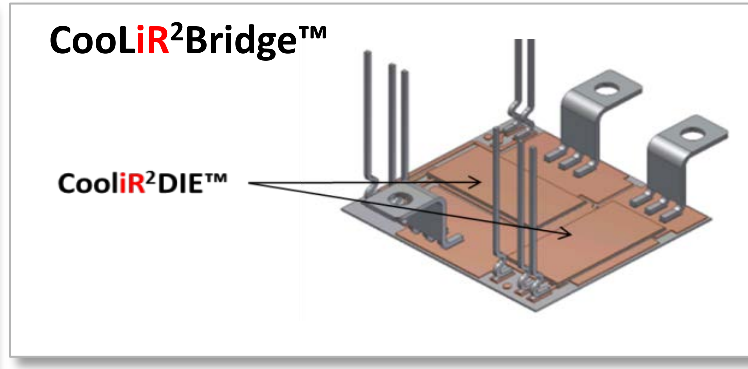
CooliR²DIE™ ***building blocks***

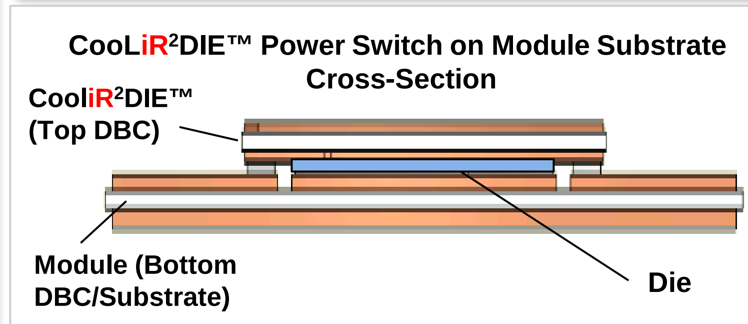
Bridging the gap between "discretes" and modules

COOLiR^{2}™ Packaging Platform for HEV/EV Inverters

Power circuit construction using CooliR^{2}Die™



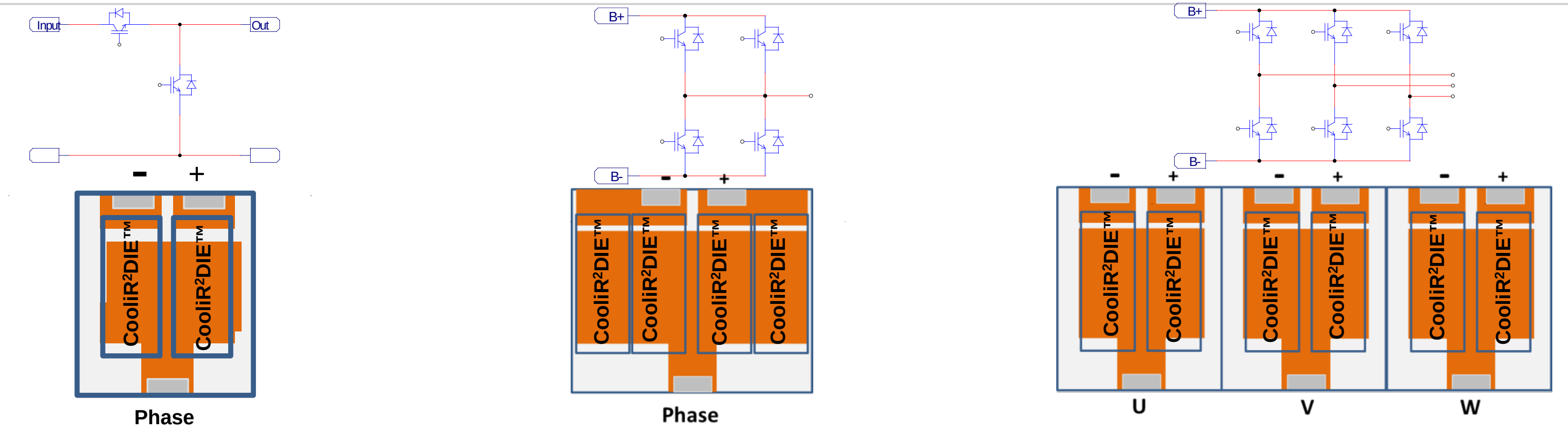




- Wirebonds eliminated
- Parasitic R and L reduced
- Compatibility with different die attach techniques including soldering or sintering
- CooliR^{2}DIE™ assemblies can be over-molded or protected by a gel-filled housing

COOLiR²™ Packaging Platform for HEV/EV Inverters

Power circuit construction using CooliR²Die™



Half-bridge, Buck or Boost *Double current rating* *3-Phase Bridge*

FLEXIBILITY and ***CONVENIENCE*** of ***CooliR²Die™***

- parallelable → higher current rating
- pre-packaged → no need to handle the super-thin bare die
- fully tested → higher yield of final assembly
- Various circuit topologies possible
- High power circuits implementation without the use of power modules
- Compatibility with baseplates or heatsinks
- Cooled on one or two sides

Innovative CooliR^{2}™ Packaging Platform

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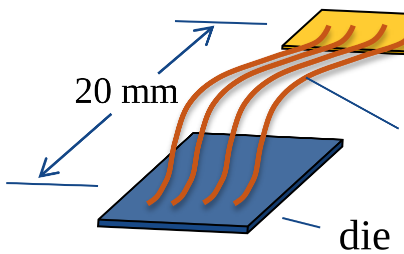
COOLiR^{2}™ - Electrical Performance

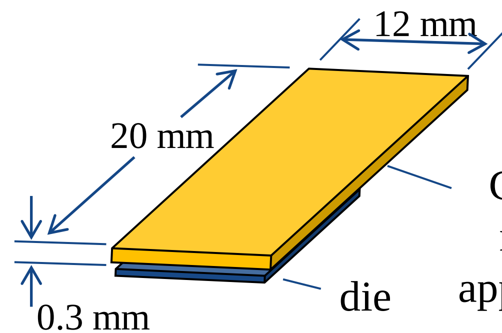
Resistance of wirebonds vs. wirebond-less interconnections

Approx. <u>20 wires with 20mil dia.</u> are needed to achieve the low resistance of CooliR^{2}DIE™

(more than could be placed on the die)



20 mil. bondwire resistance is approx. **2.6** mΩ ea.



Copper plane resistance is approx. **0.13** mΩ

CooliR^{2}Bridge™ total resistance
(incl. DBC and leadframe)

- Approx. **0.5 mOhm** (from DC+ to DC- terminals)
- Approx. **1 mOhm** for wirebonded modules

__0.5 mΩ__ of additional wirebonds resistance at 300A results in __0.15V__ more voltage drop across the module

This causes __45W__ of additional power dissipation per phase (approx. __5%__ increase of the overall inverter losses)

COOLiR²™ - Electrical Performance

Inductance of wirebonds vs. wirebond-less interconnections

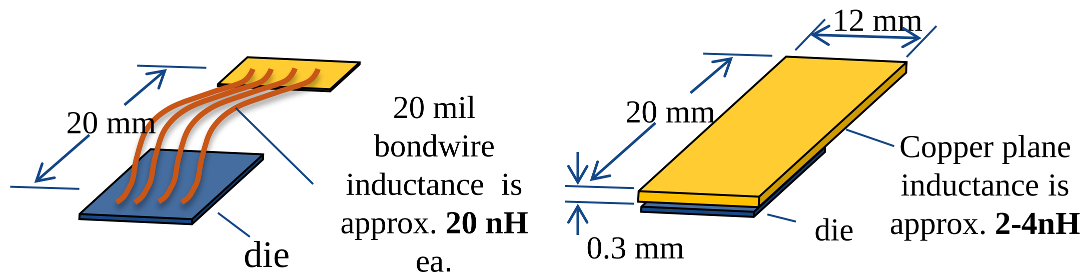
The inductance of Cu plane is approx. 5 to 10 times lower than the inductance of one wirebond

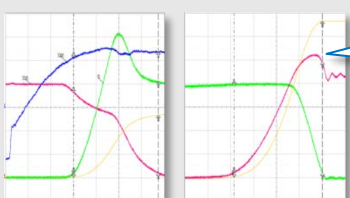
Paralleling multiple wirebonds doesn't reduce the inductance proportionally due to mutual coupling effect.

480A CooliR²Bridge™
total inductance is approx. 12 nH
and can be reduced further.

Main inductance contributors:

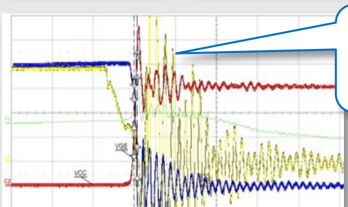
- leadframe
- main DBC substrate layout





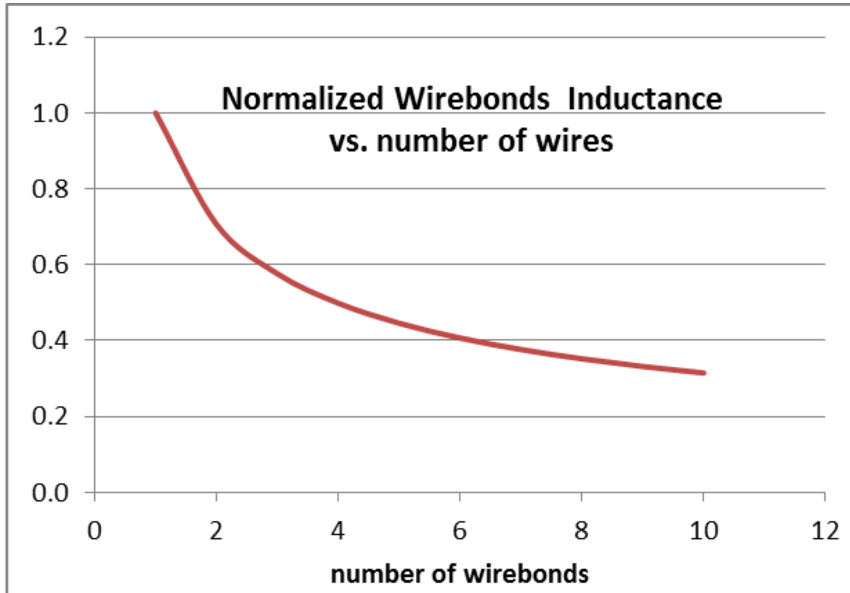
Small overshoot, reduced ringing

Effects of low stray inductance



High overshoot, severe ringing

Effects of high stray inductance



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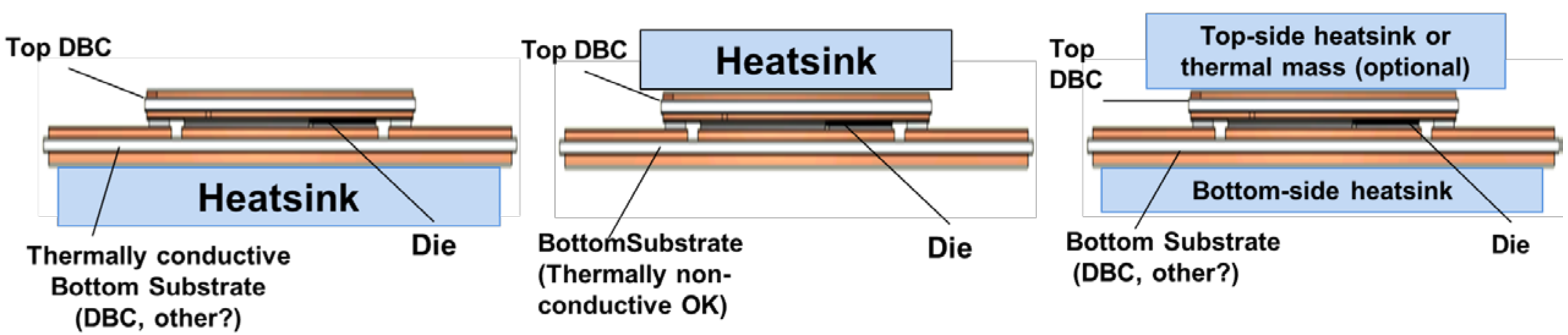
COOLiR²™ - Thermal Performance

Cooling Method Flexibility

- Traditionally, only one side of the semiconductor die is used for heat removal.
- Increasing current and power density + smaller die area → high heat flux density.
- Dual-sided cooling will become a necessity in modern high-power density inverters.

Cooling method flexibility in the CooliR²™ packaging platform



Bottom-side cooling | *Top-side cooling* | *Dual-sided cooling*

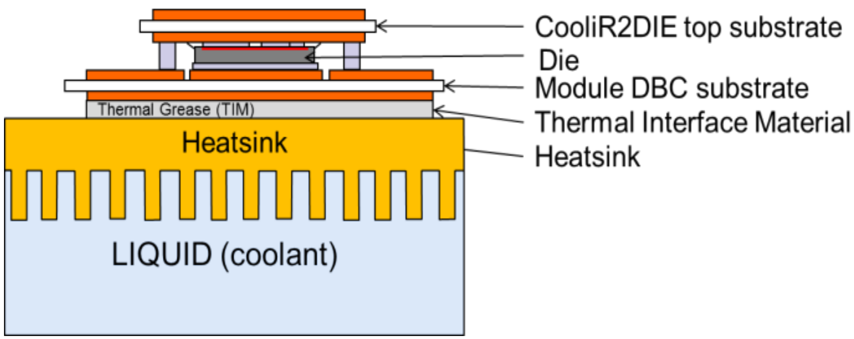
Dual-side cooling → Rth j-c reduced by up to 50%

- Thermal mass reduces the transient thermal resistance Zth.
- CooliR²™ modules can be attached to a baseplate or direct liquid cooled heatsink.

COOLiR²™ - Thermal Performance

Effect of standard base plate and direct liquid cooling

Estimated Rth junction-heatsink for different configurations with single sided-cooling



The best result achieved with

direct-liquid-cooled heatsink

- Approx. 10% to 15% lower Rth j-coolant
- The durability of the direct-liquid-cooled heatsink is the main concern.

without base plate

Layer	thickness Z [mm]	conductivity K [W/mK]	Rth [K/W]	contribution %
IGBT solder	0.1	25	0.040	8%
DBC Cu	0.3	380	0.007	1%
DBC Al2O3	0.38	24	0.141	27%
DBC Cu	0.3	380	0.007	1%
TIM (thermal grease)	0.05	3	0.133	25%
		Rth j-sink	**0.328**	

with base plate

Layer	thickness Z [mm]	conductivity K [W/mK]	Rth [K/W]	contribution %
IGBT solder	0.1	25	0.040	9%
DBC Cu	0.3	380	0.007	2%
DBC Al2O3	0.38	24	0.141	30%
DBC Cu	0.3	380	0.007	1%
Solder	0.15	25	0.047	10%
Baseplate (Copper)	3	380	0.038	8%
TIM (thermal grease)	0.1	3	0.109	23%
		Rth j-sink	**0.388**	

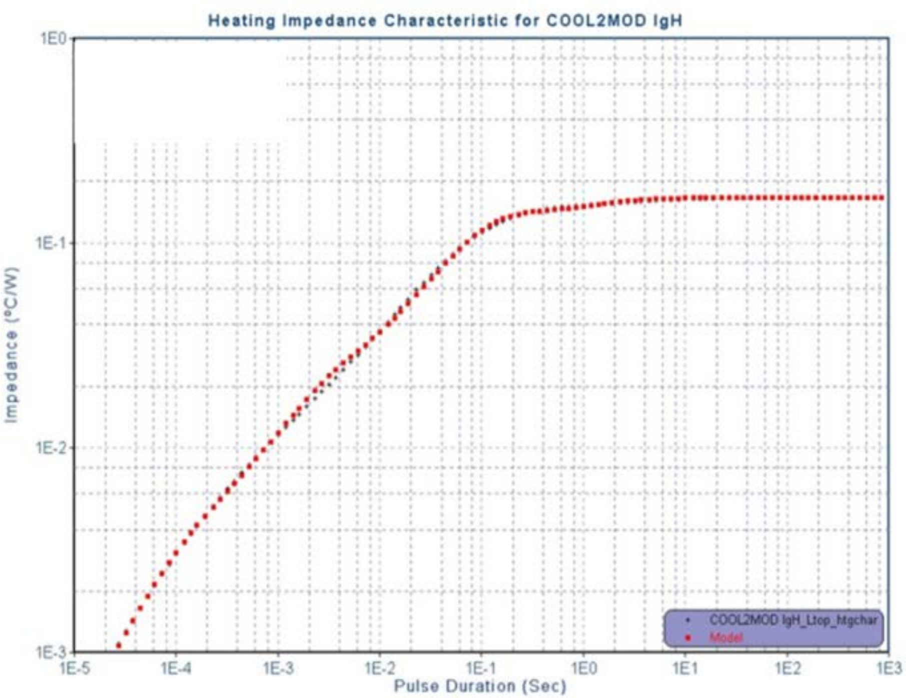
with direct liquid-cooled baseplate

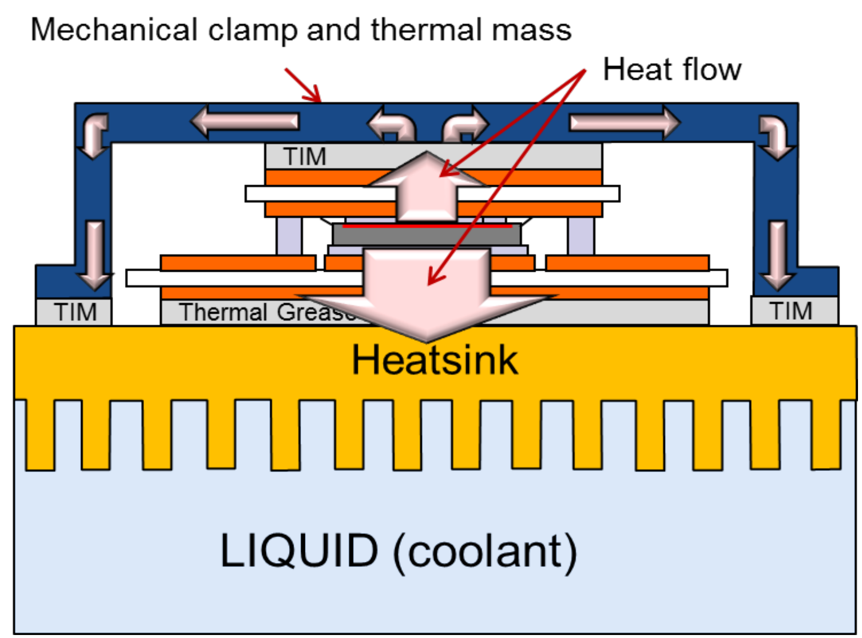
Layer	thickness Z [mm]	conductivity K [W/mK]	Rth [K/W]	contribution %
IGBT solder	0.1	25	0.040	8%
DBC Cu	0.3	380	0.007	1%
DBC Al2O3	0.38	24	0.141	27%
DBC Cu	0.3	380	0.007	1%
Solder	0.15	25	0.047	9%
		Rth j-sink	**0.242**	

Improving transient thermal performance

The thermal mass of **CooliR²DIE™** is larger than that of a conventional wirebonded die.

CooliR²Bridge™ provides the option to utilize the mechanical clamp as a thermal mass





COOLiR^{2}™ - Thermal Performance

Improving performance with dual-sided cooling capability

Thermal resistance with dual-sided cooling

For $Rth\ j-c\ BOTTOM = Rth\ j-c\ TOP$

$$Rth\ j-c\ DUAL-SIDED = \frac{Rth\ j-c\ BOTTOM}{2}$$

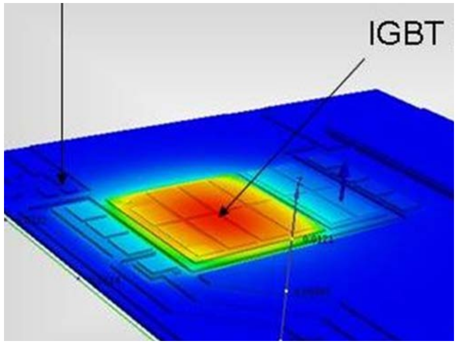
It may not be possible to achieve the same thermal resistance on both sides.
*Assuming the thermal resistance of one side is **60**% higher, the overall Rth j-coolant is still reduced by approx. **39**%.*

$$Rth\ j-c\ DUAL-SIDED = $$

$$= \frac{1}{\frac{1}{Rth\ j-c\ BOTTOM} + \frac{1}{1.6 * Rth\ j-c\ BOTTOM}} =$$

$$\approx 0.61 * Rth\ j-c\ BOTTOM$$

The “sandwich” structure of the CooliR^{2}DIE™ results in more uniform die surface temperature.



The copper planes on both sides help the lateral heat spreading.

The elimination of hot spots results in safer operation and increased current rating.

*Rth j-coolant reduced by **39%** → **50%** higher current rating.*

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COOLiR^{2}™ - Reliability

Improving reliability by eliminating failure mechanisms

Power Cycling results

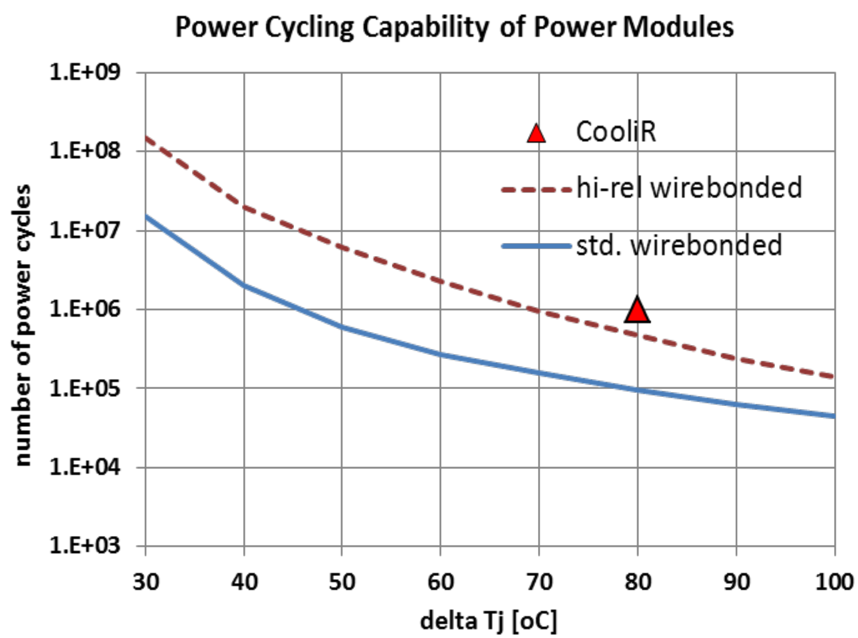
CooliR^{2}Bridge™ modules power cycling test conditions:

- constant current
- 2 s on-time and 4 s off-time
- delta Tj of **80ºC**
- Tj max of 150ºC

Reached **998,000** cycles

CooliR^{2}Bridge™ is expected to reach even higher number of cycles in the next trial.

*High reliability of **CooliR^{2}™** technology achieved by elimination of the primary failure mode – wirebonds failure*



Additional reliability improvements of **CooliR^{2}™** technology:

- increased maximum junction operating temperature (**Tjmax=175ºC**)
- more uniform die temperature distribution

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COOLiR²™ - High Power Density

Power density improvements

CooliR²™ technology power density improvement in comparison with conventional wirebonded and gel-filled power module technology

	Improvement	Effect on Power Density	Improvement Factor
Dual-sided cooling	~ 50% higher current density	+ 50%	1.5
Tj_{MAX}	from 150 ^{o}C to 175 ^{o}C	+ 20%	1.2
Module size	~ 50%	+100%	2.0
	Total:	> + 300%	3.6

Combined effect of
dual-sided cooling + Tjmax. increase
→ approx. 80% increase of power module current rating.

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CONCLUSIONS

CooliR^{2}™ HEV/EV Power Modules Platform addresses all challenges posed by the demanding HEV/EV inverter applications

ACHIEVEMENTS

- **Improved electrical performance**
- **Improved thermal performance**
- **Increased reliability**
- **Increased power density**
- **Reduced size and weight**
- **Lower system cost**

Challenges	
Size, volume	↓
Weight	↓
Cost	↓
Reliability	↑

CooliR^{2}™ platform has the potential to break-away from traditional single-side cooled wirebonded power modules and revolutionize the way automotive power converters are being build.