SIEMENS

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Errata Sheet

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Device : **SAB 80C166E**
Stepping Code / Marking : **CC**

This errata sheet describes the functional problems and the deviations from the electrical and timing specification known in this step. The problems described in section A and C may also be found in the target devices SAB 80C166/83C166 and 88C166. For easier reference, the numbering of the problems in sections A and C is the same as in the Errata Sheets for the SAB 80C166. See also the Crossreference List of open and fixed problems.

Changes from Errata Sheet **Rel. 1.5** for devices with stepping code/marking CA this Errata Sheet **Rel. 1.0** for devices with stepping code/marking CC:

- Functional Problems A15, A17, A19, A20 fixed
- Bondout Specific Problem B4 fixed
- Electrical Problem C3 fixed
- P3.12/BHE# in Sigle Chip Mode (see Appendix, item 5)
- Serial Channel Start Bit Detection (see Appendix, item 6)

A) Functional Problems

The following malfunctions are known in this step:

Problem A22: A/D Converter Overrun Error Generation

When the result of an A/D conversion has not been read from register ADDAT by the time the next conversion is complete (e.g. because reading of ADDAT was blocked by a higher priority interrupt), the following problem may occur for read operations from ADDAT within a time window of 6 TCL after completion of an A/D conversion:

A read operation which was triggered by the last ADC conversion complete interrupt (flag ADCIR) may already read the result of the just finished conversion, however the ADC overrun error interrupt (flag ADEIR) is **not** generated. Note that flag ADCIR is set again, so that another conversion complete interrupt or PEC transfer (which will deliver the same result) will be generated.

Workaround:

Assign an interrupt priority to the ADC conversion complete interrupt which is high enough to avoid an overrun error situation. Or, in the autoscan modes, check the channel number information in the 4 MSBs of the converted result to see whether the results of one channel are missing in the autoscan sequence.

This problem will be fixed in one of the next steps.

Problem 23: Serial Channel Overrun Error Generation

When the last character received has not been read from register SxRBUF by the time reception of the next character is complete (e.g. because reading of SxRBUF was blocked by a higher priority interrupt), the following problem may occur for read operations from SxRBUF within a time window of 4 TCL after reception of a character:

A read operation which was triggered by the last receive interrupt (flag SxRIR) may already read the next character received, however the overrun error flag (SxOE) is **not** set and the overrun interrupt (flag SxEIR) is **not** generated. Note that flag SxRIR is set again, so that another receive interrupt or PEC transfer (which will read the same character) will be generated.

Workaround:

Assign an interrupt priority to the receive interrupt which is high enough to avoid an overrun error situation.

This problem will be fixed in one of the next steps.

C) Deviations from the Electrical and Timing Specification

The following electrical and timing parameter deviations from the specification in the SAB 80C166 Data Sheet 3.90 are known in this step:

Problem C4: ALE Rising to CLKOUT Falling Edge Time, t_{34}

The ALE signal is leading the CLKOUT signal by about 5ns. This means that the minimum time specification of t_{34} is not met: The ALE Rising to CLKOUT Falling Edge Time, t_{34}, is about -5ns instead of 0ns minimum time as specified.

Appendix

In this appendix, some architectural items are described which are not yet documented in a very detailled manner in the current release of the SAB 80C166 User's Manual and/or Data Sheet. In the next revisions, these items will be integrated.

1.) Synchronous READY#: When the 'Synchronous Ready' mode has been selected for external memory accesses, for example by the following instruction sequence,

```
BCLR  DP3.14      ;     Pin direction = INPUT
BCLR  SYSCON.3    ;     Select 'Synchronous Ready' Mode
BSET  RDYEN       ;     Enable READY function
```

this mode will only work properly if the system clock output pin CLKOUT is enabled in addition (P3.15 = 1, DP3.15 = 1, SYSCON.CLKEN = 1). The reason for this is that the system clock is normally required externally as synchronous reference signal.

2.) MDL Register: From the **CA-step** on, the MDL register may also be read via a short 'reg' addressing mode immediately after a divide instruction. This means that the note concerning the pipeline side effect in the Appendix of previous Errata Sheets must no longer be taken into account.

E.g., both of the following instruction sequences will always work correctly:

```
a)    DIV   Rx
      MOV   Ry, MDL     ;     'reg, mem' addressing mode

b)    DIV   Rx
      MOV   ext_mem, MDL;     'mem,reg' addressing mode
```

3.) Uninterruptable Instruction Sequences: To be absolutely sure that an instruction (sequence) can not be interrupted, at least 2 instructions (e.g. NOPs) must be programmed after the instruction disabling the interrupts, as shown in the following example (see also the application note *Interrupt System #1* in the SAB 80C166 Family ApNotes collection):

```
BCLR  IEN
NOP               ;     or other appropriate instructions
NOP
...               ;     Start of the uninterruptable range
```

4.) JBC/JNBS Instructions: From the **CA-step** on, the operation of the semaphore instructions JBC/JNBS has been changed such that these instructions only write back to the bit to be tested when the branch condition is true. This modification has no effect on bits in the internal RAM or on SFR bits which are not modified by hardware. However, the use of these instructions on SFR bits which may be changed both by hardware and software is now directly possible without any special considerations (see also the application note on *JBC/JNBS* in the SAB 80C166 Family ApNotes collection).

The modified operation of the JBC/JNBS instructions is as follows:

JBC:

```
IF (bit) = 1 THEN
        (bit) := 0
        (IP) := target
ELSE
        next instruction
END IF
```

JNBS:

```
IF (bit) = 0 THEN
        (bit) := 1
        (IP) := target
ELSE
        next instruction
END IF
```

5.) P3.12 (BHE#) in Single Chip Mode: From the **CC-step** on, when the Single Chip mode is selected during reset (pin BUSACT# = 1, pins EBC0 = EBC1 = 0), P3.12/BHE# is floating as all other I/O port pins during and after reset. In earlier steps of the 80C166, P3.12/BHE# was driving a low level after reset until bit SGTDIS was set to '1'.

This means that the special considerations which were mentioned in the Appendix of previous Errata Sheets are no longer required for the CC-step and following steps of the 80C166. Now, P3.12 may be used also in Single Chip Mode the same way as any other I/O pin.

6.) Serial Channel Start Bit Detection: From the **CC-step** on, a real edge detection circuit has been implemented on pins RxD0/P3.11 and RxD1/P3.9. This means that reception of data in the asynchronous modes is started whenever an actual high-to-low transition is detected on the respective pins.

In previous steps of the 80C166, reception was started whenever a low level was detected on the RxD0/1 pins. This meant that it was implicitly assumed that the RxD0/1 line was held in the high state when no data were transferred. However, if the RxD0/1 line went low for longer than the time for one character (including start/stop bits), a (framing) error interrupt was generated and another reception was started. This procedure was continued until the RxD0/1 line went high.

From the **CC-step** on, if the RxD0/1 line goes low for longer than the time for one character (including start/stop bits), a (framing) error is generated, but **no** other reception is started.