Microcontrollers

Errata Sheet

5 July 2001 / Release 1.3

Device:	**C513AO-2E**
Stepping Code / Marking:	**AB**
Package:	**P-DIP-40, P-LCC-44, P-MQFP-44**

This Errata Sheet describes the deviations from the current user documentation. The classification and numbering system is module oriented in a continual ascending sequence over several derivatives, as well already solved deviations are included. So gaps inside this enumeration could occur.

The current documentation is: C513AO User's Manual 05.99
C513AO Data Sheet 02.00
Instruction Set Manual 05.98

Note: ***Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.***

The specific test conditions for EES and ES are documented in a separate Status Sheet.

Change summary to last Errata Sheet Rel. 1.2:

- New item numbered OTP.1.

Functional Problems:

WDT.1: Watchdog Timer is not halted in idle mode

The Watchdog Timer (WDT) is not halted in the idle mode as defined. However, during the idle mode, an overflow condition of the WDT does not initiate an internal reset. In such a case the WDT starts a new count sequence.

Workaround:

1. Do not use the WDT function in combination with the idle mode.
2. In case of WDT is running before entry into idle mode, to avoid a WDT initiated reset upon exit of the idle mode, the following methods can be used.

(A) The WDT is refreshed immediately upon exit from idle mode.

(B) A timed interrupt can be used to exit the idle mode before the WDT reaches the counter state 7FFCh. This can be achieved by using Timer 0, 1 or 2. This timer can be programmed to generate an interrupt at a WDT counter state prior to overflow, for e.g., at 7F00h. Prior to entering idle mode, the WDT can be refreshed and the timer 0, 1or 2 can be started immediately to synchronize the WDT. In the interrupt service routine of the Timer 0, 1 or 2, the WDT must be refreshed. If required, idle mode could be entered again.

WDT.2: Setting WDT and SWDT bits in WDCON Register by using Immediate Addressing mode instruction may not refresh the Watchdog Timer

To initiate a refresh of the Watchdog timer, the WDT bit should be set directly before the SWDT bit in WDCON register (WDCON.1 and WDCON.0). However, using the Immediate Addressing mode instruction to set the WDT and SWDT bits may not refresh the Watchdog timer, the Watchdog timer may keep counting until overflow and reset the device.

For example:

```
MOV   WDCON, #02h
MOV   WDCON, #01h
```

These instructions will not refresh the Watchdog timer.

Workaround:

Use the Bit Manipulation Instruction to set the WDT and SWDT bits.

For example:

```
SETB  WDCON.1
SETB  WDCON.0
```

OTP.1: OTP module may fail under special conditions, leading to undefined operation

The OTP module may malfunction, causing the chip to enter an undefined state with unsteady operation, if there is a remaining voltage at the V_{DD} pin before powering up. The critical remaining voltage is approximately 100-400mV. The undefined state can only be left by a complete power off (V_{DD}=0V) and not by any RESET-source (e.g. hardware reset, WDT-reset). The problem is due to variation in technology and manufacturing parameters.

Workaround:

The device should always be powered up from V_{DD}=0V, ensuring that there is no voltage at any pins which leads to a remaining voltage level at V_{DD} pin (coupling over the ESD-structure).

Deviation from Electrical- and Timing Specification:

DC.1: Increased I_{IL} maximum current

The maximum value of the logic 0 input current for ports 1,2 and 3 pins, $\mathbf{I_{IL}}$, is -70µA instead of -50µA as stated in the specification.
The new value will be worked into future documentation.

DC.2: V_{DD} is valid for a smaller range than specified on documents

$\mathbf{V_{DD}}$ is valid in the range from 4.5V to 5.5V at all specified temperatures, instead of 4.25V to 5.5V as specified on the documents. This smaller range is effective on devices with date code starting from *0116*.

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