Errata Sheet

V 1.1, 2006-03

Device	**C505A-4RM,**
	C505CA-2RM/4RM/LM,
	C505CA-4RC
Marking/Step	**Step ES-CA, CA**
Package	**P-MQFP-44, Bare Die**

This Errata Sheet describes the deviations from the current user documentation.

The module oriented classification and numbering system uses an ascending sequence over several derivatives, including already solved deviations. So gaps inside this enumeration can occur.

Current Documentation

- C505(C) User's Manual 08.97
- C505A/C505CA Addendum to C505(C) User's Manual 09.97
- C505(A)/C505C(A) Data Sheet 12.02
- C505CA-4RC Step BB (Bare Die) Data Sheet V1.3 12.00
- Instruction Set Manual 05.98

Note: Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.

The specific test conditions for EES and ES are documented in a separate Status Sheet.

Contents

1 History List/Change Summary

(since last CPU Step ES-CA,CA, previous Errata Sheet V1.0)

Table 1 Functional Deviations

Functional Deviation	Short Description	Fixed in Step	Change
CAN.2	Unexpected Remote Frame Transmission (C505CA only)		
CAN.3	Description in User's Manual regarding the reception of remote frames and the data length code (DLC) field is incorrect (C505CA only)		
CAN.4	Flowchart sequence in figure in User's Manual regarding Micro-controller handling of the Last Message Object is partly incorrect (C505CA only)		
CAN.5	Description in User's Manual section 6.4.5 regarding the Configuration of the Bit Timing is partly incorrect (C505CA only)		
SWPD.1	Triggering of Software Power Down (SWPD) wake up immediately after SWPD entry via external interrupt on a frequent basis is not recommended.		

Table 2 AC/DC Deviations

AC/DC Deviation	Short Description	Fixed in Step	Change
DC.4	Minimum limit of logic 0 input current I_{IL} min is lower		

Table 3 Application Hints

Application Hint	Short Description	Fixed in Step	Change
HINT.1	Content of VR2 register is incremented		NEW

2 Functional Deviations

CAN.2: Unexpected Remote Frame Transmission (C505CA only)

The on-chip CAN module may send an unexpected remote frame with the identifier=0, when a pending transmit request of a message object is disabled by software.

There are three possibilities to disable a pending transmit request of a message object (n=1..14):

- Set CPUUPDn element
- Reset TXRQn element
- Reset MSGVALn element

Either of these actions will prevent further transmissions of message object n.

The symptom described above occurs when the CPU accesses CPUUPD, TXRQ or MSGVAL, while the pending transmit request of the corresponding message object is transferred to the CAN state machine (just before start of frame transmission). At this particular time the transmit request is transferred to the CAN state machine before the CPU prevents transmission. In this case the transmit request is still accepted from the CAN state machine. However the transfer of the identifier, the data length code and the data of the corresponding message object is prevented. Then the pre-charge values of the internal ìhidden bufferî are transmitted instead, this causes a remote frame transmission with identifier=0 (11 bit) and data length code=0.

This behavior occurs only when the transmit request of message object n is pending and the transmit requests of other message objects are not active (single transmit request). If this remote frame loses arbitration (to a data frame with identifier=0) or if it is disturbed by an error frame, it is not retransmitted.

Effects to other CAN nodes in the network

The effect leads to delays of other pending messages in the CAN network due to the high priority of the Remote Frame. Furthermore the unexpected remote frame can trigger other data frames depending on the CAN node's configuration.

Workaround:

1. The behavior can be avoided if a message object is not updated by software when a transmission of the corresponding message object is pending (TXRQ element is set) and the CAN module is active (INIT = 0). If a re-transmission of a message (e.g. after lost arbitration or after the occurrence of an error frame) needs to be cancelled, the

TXRQ element should be cleared by software as soon as NEWDAT is reset from the CAN module.

2. The nodes in the CAN system ignore the remote frame with the identifier=0 and no data frame is triggered by this remote frame.

CAN.3: Description in User's Manual regarding the reception of remote frames and the data length code (DLC) field is incorrect

It is inaccurately described in the User's Manual on page 6-94 under *'Arbitration Registers'* that *'When the CAN controller stores a remote frame, only the data length code is stored into the corresponding message object'*. The correct should be that the DLC field remains unchanged in the receiving message object, and that the CPU has the responsibility to define the DLC of the answering data frame.

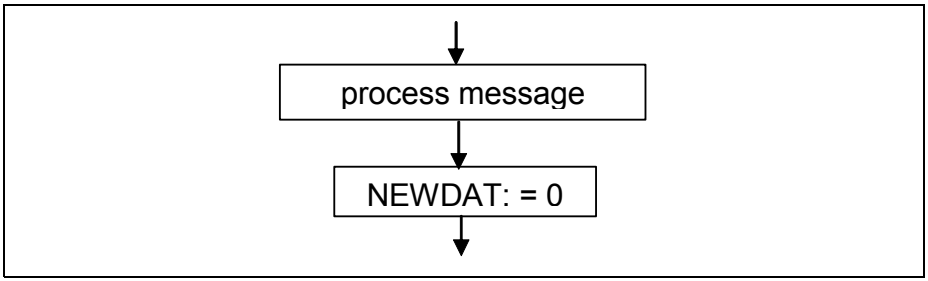
This correction will be updated to the future versions of the User's Manuals.

Workaround:

Not applicable.

CAN.4: Flowchart sequence in figure in User's Manual regarding Micro-controller handling of the Last Message Object is partly incorrect

For the software flowchart figure 6-48 in User's Manual 11.97, the correct would be to first 'process message contents' and then to 'clear bit NEWDAT'.



This correction will be updated to the future versions of the User's Manuals.

Workaround:

Not applicable.

CAN.5: Description in User's Manual section 6.5.5 regarding the Configuration of the Bit Timing is partly incorrect (C505CA only)

As described for the CAN Bit Timing Register High BTR1, the minimum total time requirement for segment 1 and segment 2 is as follows:

$$t_{TSeg1} \geq 3 \times t_q$$
$$t_{TSeg2} \geq 2 \times t_q$$

The total bit time remains at ($t_{TSeg1} + t_{TSeg2} \geq 7 \times t_q$).

This correction will be updated to the future versions of the User's Manuals.

Workaround:

Not applicable.

SWPD.1: Triggering of Software Power Down (SWPD) wake up immediately after SWPD entry via external interrupt on a frequent basis is not recommended.

When the micro-controller is running at frequencies lower than 10MHz and the external wake up from SWPD occurs very soon (e.g. <200ms) after entering this mode and this happens on a regular basis, the internal clock may still be valid when the wake up trigger occurs. In this rare case, the micro-controller may get confused with its state and program execution becomes unpredictable.

Workaround:

In applications running at 10MHz or below, that enters and exits the SWPD mode on a frequent basis, it is recommended to enter Slow Down mode before Power Down mode entry. On SWPD wake up, the first instruction in the interrupt routine at 07bH should disable Slow Down mode. This method would only cause an insignificant delay in the range of s and would ensure specified behavior of the micro-controller. Note that when Slow Down mode has been entered, there is no longer a minimum time requirement before SWPD external wake up is triggered.

3 Deviations from Electrical- and Timing Specification

DC.4: Minimum limit of logic 0 input current I_{IL} min is lower

The minimum for the logic 0 input current at the ports is lower than the specified values:

I_{IL} min. is –5 µA (instead of –10 µA)

4 Application Hints

No application hints are known for this step.

Hint 1: Content of VR2 register is incremented

The VR2 register has a reset value of 34_H.

Workaround:

None.