This Errata Sheet describes the deviations from the current user documentation. The module oriented classification and numbering system uses an ascending sequence over several derivatives, including already solved deviations. So gaps inside this enumeration can occur.

**Current Documentation**

- C504 User's Manual 11.97
- C504 Data Sheet May 2000
- Instruction Set Manual 07.2000

*Note: Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.*

The specific test conditions for EES and ES are documented in a separate Status Sheet.

**Contents**

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>History List/Change Summary</td>
<td>2</td>
</tr>
<tr>
<td>Functional Deviations</td>
<td>4</td>
</tr>
<tr>
<td>Deviations from Electrical- and Timing Specification</td>
<td>7</td>
</tr>
<tr>
<td>Application Hints</td>
<td>10</td>
</tr>
</tbody>
</table>
1 History List/Change Summary

(since last CPU Step ES-BB/BB, previous Errata Sheet V1.5)

Table 1 Functional Deviations

<table>
<thead>
<tr>
<th>Functional Deviation</th>
<th>Short Description</th>
<th>Fixed in Step</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCU.1</td>
<td>Spike at CCx / COUTx pins</td>
<td>ES-CA/CA</td>
<td></td>
</tr>
<tr>
<td>EH.1</td>
<td>Emulation Mode not supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RST.1</td>
<td>Figure in User’s Manual and Data Sheet regarding the Reset Circuitries is incorrect</td>
<td></td>
<td>New</td>
</tr>
<tr>
<td>T2.1</td>
<td>Timer 2 - Concurrent Access on T2CON</td>
<td>ES-CA/CA</td>
<td></td>
</tr>
<tr>
<td>WDT.1</td>
<td>Watchdog Timer is not halted in the Idle Mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WDT.2</td>
<td>To refresh the Watchdog Timer, the WDT and SWDT bits in WDCON Register can not be set by using Immediate Addressing Mode instruction</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OTP.1</td>
<td>ROM Verification Mode 2 and verification error signaling at Port 3.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OTP.2</td>
<td>OTP module may fail under special conditions, leading to undefined operation</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2 AC/DC Deviations

<table>
<thead>
<tr>
<th>AC/DC Deviation</th>
<th>Short Description</th>
<th>Fixed in Step</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC.1</td>
<td>Minimum Oscillator Clock Frequency</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC.1</td>
<td>[4 \text{ LSB Total Unadjusted Error (TUE) of A/D Converter}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC.2</td>
<td>Power Down Mode supply current</td>
<td>ES-CA/CA</td>
<td></td>
</tr>
<tr>
<td>DC.3</td>
<td>Maximum value of - 70 (\mu\text{A}) for the logic 0 input current (Ports 1, 2, 3)</td>
<td></td>
<td>Updated</td>
</tr>
<tr>
<td>DC.5</td>
<td>Output low voltage ((V_{OL})) of the output pin COUT3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 2 AC/DC Deviations (cont’d)

<table>
<thead>
<tr>
<th>AC/DC Deviation</th>
<th>Short Description</th>
<th>Fixed in Step</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC.6</td>
<td>± 6 LSB Total Unadjusted Error (TUE) of A/D Converter at 40 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC.8</td>
<td>Minimum value of -3 µA for the logic 0 input current (Ports 1, 2, 3)</td>
<td></td>
<td>New</td>
</tr>
<tr>
<td>DC.9</td>
<td>Maximum limit values of the power supply current (I_{DD}) for Active Mode</td>
<td></td>
<td>New</td>
</tr>
<tr>
<td>DC.10</td>
<td>Maximum limit values of the power supply current (I_{DD}) for Idle Mode</td>
<td></td>
<td>New</td>
</tr>
</tbody>
</table>

### Table 3 Application Hints

<table>
<thead>
<tr>
<th>Application Hint</th>
<th>Short Description</th>
<th>Fixed in Step</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>None.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2 Functional Deviations

EH.1: Emulation Mode not supported
The “Enhanced Hooks Technology” Emulation Mode is not supported by the C504-2E.

Workaround:
None.

RST.1: Figure in User’s Manual and Data Sheet regarding the Reset Circuitries is incorrect
Figure 5-1 in User’s Manual and Figure 6 in Data Sheet show incorrectly that the RESET pin has an internal pullup resistor connected to the $V_{DD}$. Instead, at the RESET pin, an internal pulldown resistor is connected to the $V_{SS}$. The correct implementation is illustrated in Figure 1.

![Figure 1 Reset Circuitries](image)

This correction will be updated to the future versions of the User’s Manual and Data Sheet.

Workaround:
Not applicable
**WDT.1: Watchdog Timer is not halted in Idle Mode**

The Watchdog Timer (WDT) is not halted in the Idle Mode as defined. However, during the Idle Mode, an overflow condition of the WDT does not initiate an internal reset. In such a case, the WDT starts a new count sequence.

**Workaround:**

1. Do not use the Watchdog Timer function in combination with the Idle Mode
2. In case of WDT is running before entry into idle mode, to avoid a WDT initiated reset upon exit of the Idle Mode, the following methods can be used.
   a) The WDT is refreshed immediately upon exit from Idle Mode.
   b) A timed interrupt can be used to exit the Idle Mode before the WDT reaches the counter state 7FFCh. This can be achieved by using Timer 0, 1 or 2. This timer can be programmed to generate an interrupt at a WDT counter state prior to overflow, for e.g., at 7F00h. Prior to entering Idle Mode, the WDT can be refreshed and Timer 0, 1 or 2 can be started immediately to synchronize the WDT. In the interrupt service routine of Timer 0, 1 or 2, the WDT must be refreshed. If required, Idle Mode could be entered again.

**WDT.2: Setting WDT and SWDT bits in WDCON Register by using Immediate Addressing Mode instruction may not refresh the Watchdog Timer.**

To initiate a refresh of the Watchdog Timer, the WDT bit should be set directly before the SWDT bit in WDCON register (WDCON.1 and WDCON.0). However, using the Immediate Addressing Mode instruction to set the WDT and SWDT bits may not refresh the Watchdog Timer, the Watchdog Timer may keep counting until overflow and reset the device.

For example:

```assembly
MOV    WDCON, #02h
MOV    WDCON, #01h
```

These instructions will not refresh the Watchdog Timer.

**Workaround:**

Use the Bit Manipulation Instruction to set the WDT and SWDT bits.

For example:

```assembly
SETB   WDCON.1
SETB   WDCON.0
```
**OTP.1: ROM Verification Mode 2 and verification error signaling at Port 3.5**

The last block of 16 bytes will always return verification error in the ROM Verification Mode 2.

**Workaround:**

None.

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**OTP.2: OTP module may fail under special conditions, leading to undefined operation**

The OTP module may malfunction, causing the C504 to enter an undefined state with unsteady operation, if there is a remaining voltage at the $V_{DD}$ pin before powering up. The critical remaining voltage is approximately 100-400mV. The undefined state can only be left by a complete power off ($V_{CC}$=0V) and not by any RESET-source (e.g. hardware reset, WDT-reset). The problem is due to variation in technology and manufacturing parameters.

**Workaround:**

The device should always be powered up from $V_{DD}$=0V, ensuring that there is no voltage at any pins which leads to a remaining voltage level at $V_{DD}$ pin (coupling over the ESD-structure).
3 Deviations from Electrical- and Timing Specification

**AC.1: Minimum Oscillator Clock Frequency**
The minimum oscillator clock frequency $1/t_{CLCL}$ is increased to 4 MHz (instead of 3.5 MHz).

**Workaround:**
None.

**DC.1: ± 4 LSB Total Unadjusted Error (TUE) of A/D Converter**
The total unadjusted error of the A/D Converter does not meet the specified value of the DC characteristics. The value for TUE is limited as follows:

$$TUE = \pm 4 \text{ LSB} \quad \text{in the } V_{\text{IN}} \text{ range: } V_{\text{SS}} < V_{\text{IN}} < V_{\text{CC}}$$

**Workaround:**
None.

**DC.3: Maximum value of - 70 \( \mu \text{A} \) for the logic 0 input current (Ports 1, 2, 3)**
The maximum value of the logic 0 input current for ports 1, 2, and 3 is higher than the specified value:

$$I_{IL \text{ max}} = -70 \ \mu\text{A} \quad \text{(instead of } -50 \ \mu\text{A})$$

*Note: This DC deviation is updated from previous Errata Sheet V1.5, where it was previously documented as fixed in Step ES-CA/CA.*

**Workaround:**
None.
**DC.5: Output low voltage (V\text{OL}) of the output pin COUT3**

The maximum output low voltage of the output pin COUT3 (pin #28) is increased:

\[ V_{\text{OL}}(\text{max}) = 0.7 \text{ V} \quad \text{(instead of 0.45 V)} \]

**Workaround:**

None.

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**DC.6: \pm 6 \text{ LSB Total Unadjusted Error (TUE) of A/D Converter at 40 MHz}**

The total unadjusted error of the A/D Converter at 40 MHz operating frequency does not meet the specified value of the DC characteristics. The value for TUE is limited as follows:

\[ \text{TUE} = \pm 6 \text{ LSB} \quad \text{in the } V_{\text{IN}} \text{ range: } V_{\text{SS}} < V_{\text{IN}} < V_{\text{CC}} \quad \text{at 40 MHz} \]

**Workaround:**

None.

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**DC.8: Minimum value of - 3 \mu\text{A for the logic 0 input current (Ports 1, 2, 3)}**

The minimum value of the logic 0 input current for ports 1, 2, and 3 is lower than the specified value:

\[ I_{\text{IL \ min.}} = -3 \mu\text{A} \quad \text{(instead of -10 \mu\text{A})} \]

**Workaround:**

None.
**DC.9: Maximum limit values of the power supply current ($I_{DD}$) for Active Mode**

The maximum limit values of the power supply current ($I_{DD}$) for Active Mode are shown in the table below, instead of the specified values stated in the Data Sheet.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Maximum Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Mode</td>
<td>$I_{DD}$</td>
<td>32.11 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>40 MHz</td>
<td>49.87 mA</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Workaround:**

None.

**DC.10: Maximum limit values of the power supply current ($I_{DD}$) for Idle Mode**

The maximum limit values of the power supply current ($I_{DD}$) for Idle Mode are shown in the table below, instead of the specified values stated in the Data Sheet.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Maximum Limit Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle Mode</td>
<td>$I_{DD}$</td>
<td>19.02 mA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>40 MHz</td>
<td>27.79 mA</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Workaround:**

None.
4 Application Hints

No application hints for this step.

Application Support Group, Singapore