SIEMENS

Microcomputer Components
Technical Support Group Munich
HL MCB PD/AT1

Errata Sheet

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Device : SAB 80C515A

Marking : BB

These parts of the SAB 80C515A can be identified by the letters "BB" below the part number. The parts are mounted in a Plastic Leaded Chip Carrier (P-LCC-68) or in a Plastic Metric Quad Flat Pack (P-MQFP-80-2) package.

This errata sheet describes both the *functional problems* (see part 1) and the *deviations from the electrical and timing specifications* (see part 2) known in this step.

If a problem was already introduced with an errata sheet of an earlier step, its initial number is still retained in this errata sheet. Thus, the numerical order of the problems described in the following may contain gaps.

At the end of this document, you will find two history tables showing the problems found in the SAB 80C515A up to now. Changes to the last revision are shaded light grey in the history tables.

1) Functional Problems

The following malfunctions are known in this step:

Problem 6: Oscillator Watchdog

The problem might occur only at external clock rates below 10 MHz (2.5 MHz ≤ fosc < 10 MHz). For all other specified clock rates (10 MHz ≤ fosc ≤ 18 MHz) this problem cannot occur.

When leaving an activated oscillator watchdog reset the following problem might occur:

Conditions:

The Oscillator Watchdog is activated by:

- a fast internal reset after power on or
- a restart from hardware- or software power down mode or
- a short drop of the external clock source below the specified minimum clock rate of fosc = 2.5 MHz (e.g. in case of a short lost connection of the crystal).

The part then enters the specified reset state until the external clock source becomes stable.

Failure:

In the moment when the clock system switches over from the internal RC-oscillator to the external clock source, a spike at the internal clock system might occur. This might create an undefinded behaviour of the controller when starting up program execution (e.g. the program execution will not start at the defined reset address 0000H).

Note: A **hardware activated** watchdog timer (PE#/SWD = 1) can reset the system when missing the corresponding refresh-sequence and therefore restart the system correctly.

2) Electrical- and Timing-Spec. Deviations

The following deviations of electrical and timing parameters from the specification are known in this step:

Problem 5: f_{OSC}, Minimum Limit Value

The minimum oscillator frequency is restricted to 2.5 MHz (2.5 MHz ≤ f_{OSC} ≤ 18 MHz).

Note:

When using an external oscillator circuit with 1MHz ≤ f_{OSC} ≤ 2.5 MHz, the internal ocillator watchdog (always enabled) might initiate an internal reset.

Problem 6: ADC-Total Unadjusted Error TUE

The total unadjusted error (TUE) of ± 2 LSB in the A/D Converter Characteristics is not met. The total unadjusted error is defined in this step to TUE = ± 3 LSB.

Functional Problem No.	Marking	Description	Remarks
6	AD, ES-AE, BA, BB	Oscillator Watchdog	
5	AD, BA	Entering the Hardware Power Down Mode	fixed in ES-AE and BB
4	AD, BA	Start of Watchdog-Timer	fixed in ES-AE and BB
3	AC	Port0/Port2, XRAM Access using DPTR	fixed in AD and later
2	AC	Port 6 - Used as Digital Input	fixed in AD and later
1	AC	Busy-bit Problem	fixed in AD and later

Table 1: History of Functional Problems

Electrical- / Timing- Problem No.	Marking		Remarks
6	BA, BB	ADC - Total Unadjusted Error TUE	
5	AD, ES-AE, BA, BB	f_{OSC}, Minimum Limit Value	
4	AC	Power Supply Current in Hardware Power Down Mode	fixed in AD and later
3	AC	Input Low Current PE#/SWD, OWE, I_{IL4}	changed in data sheet 11.92
2	AC	Input Low Current XTAL2, I_{IL3}	changed in data sheet 11.92
1	AC	Logic 0 Input Current, I_{IL}	changed in data sheet 11.92

Table 2: History of Electrical- and Timing-Spec. Deviations