

To satisfy the control needs, the IR2520D uses the frequency sweep circuit showed in Fig. 4.

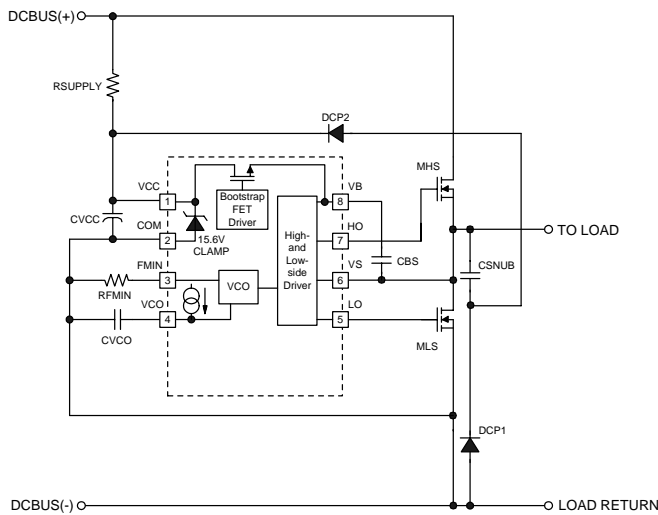


Figure 4. Frequency Sweep Mode Circuit

At startup, the internal current source charges CVCO and the voltage on pin VCO starts ramping up linearly. The oscillator starts at very high frequency, about 2.5 times the minimum frequency. The frequency ramps down towards the resonant frequency of the high-Q ballast output stage. While the frequency decreases, the voltage across the lamp increases, causing the ignition of the lamp when the frequency becomes close to the resonant frequency. If the lamp ignites successfully, the voltage on pin VCO continues to increase until it internally limits at 6V. The frequency stops decreasing and stays at the minimum frequency as programmed by an external resistor, RFMIN, on pin FMIN. The external capacitor CVCO programs the preheat time.

As for the protection needs, the challenge has been to detect over-current and hard switching without an additional Current Sensing (CS) pin. IR introduced the VS sensing circuit, the non Zero Voltage Switching (non-ZVS) protection and the current crest factor shutdown. The VS sensing circuit, the non-ZVS protection and the current crest factor shutdown circuits are shown in Fig. 5.

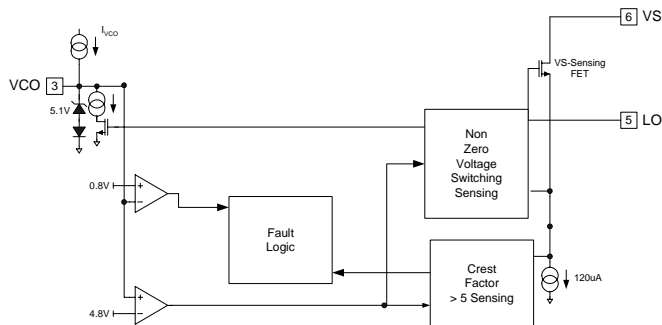


Figure 5. VS sensing, non-ZVS and current crest factor circuits

The IC uses the VS pin for over-current protection and to detect hard switching. The RDSon of the low-side

MOSFET serves as the current-sensing resistor and VS serves as the current sensing pin on the IC. In this way, the IR2520D eliminates the need for a high-precision current sensing resistor that is typically used to detect over current. An internal 600V FET connects the VS pin to the VS sensing circuitry and allows for the VS pin to be measured during the time when pin LO is high, while withstanding the high DC bus voltage when VS is at the DC bus potential.

During run mode, if the voltage at the VS pin has not slewed entirely to COM during the dead-time such that there is voltage between the drain and source of the external low-side half-bridge MOSFET when LO turns-on, then the system is operating too close to, or, on the capacitive side of, resonance. The result is non-ZVS capacitive-mode switching that causes high peak currents to flow in the half-bridge MOSFETs that can damage or destroy them. This can occur due to a lamp filament failure(s), lamp removal (open circuit), a dropping DC bus during a brown out or mains interrupt, lamp variations over time, or component variations. When non-ZVS is detected, the frequency will automatically increase to maintain ZVS. If ZVS cannot be achieved and VCO falls below 0.85V, the IC will enter Fault Mode and latch the LO and HO gate driver outputs 'low'.

During a mains brownout, when the mains voltage decreases, the resonant frequency increases, becoming close to the run frequency. This will cause non-ZVS. The IR2520D will detect non-ZVS and increase the run frequency to maintain ZVS. The system will work at a higher frequency (lower power) during low AC line conditions. The ballast will continue to work at the nominal power after the brownout.

During a lamp removal or filament failure, the lamp resonant tank will be interrupted causing the half-bridge output to go open circuit. This will cause capacitive switching (hard-switching) resulting in high peak MOSFET currents that can damage them. The IR2520D will increase the frequency in attempt to satisfy ZVS until the VCO pin decreases below 0.85V. The IC will enter Fault Mode and latch the LO and HO gate driver outputs 'low' for turning the half-bridge off safely before any damage can occur to the MOSFETs.

In order to detect deactivated lamp or failure to strike conditions, the IR2520D performs an additional measurement of the VS pin during the entire on-time of the low-side MOSFET. This voltage at the VS pin during the on-time of LO is given by the low-side MOSFET current, and therefore the output stage current, flowing through the on-resistance (RDSon) of the low-side MOSFET. However, the over current condition has to be based on a relative measure because the over current threshold has to be independent on the MOSFETs used in the circuit. The IC performs an internal crest factor measurement for detecting excessive dangerous currents or inductor saturation, which can occur during a lamp non-strike fault condition. Performing the crest factor measurement provides a relative current measurement, which cancels temperature and/or tolerance variations of the RDSon of the low-side half-bridge MOSFET. Should the peak current

exceed the average current by a factor of 5 times during the on-time of LO, the IC will enter Fault Mode and both gate driver outputs will be latched 'low'.

As a result of the IR2520D features, the circuits using the IR2520D are complete fluorescent ballast solutions offering better reliability and longer lamp life than self oscillating solutions while reducing component count and ballast size.

IV. LOW POWER FACTOR BALLAST

An electronic ballast for driving 26W compact fluorescent lamps from 220VAC has been designed and tested for performance. The circuit is shown if Fig. 6.

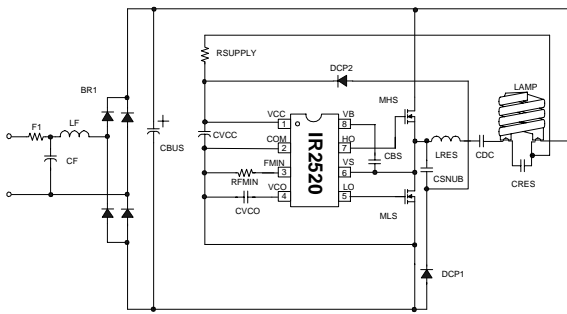


Figure 6. Low PF Ballast using the IR2520D HVIC.

The circuit provides all of the necessary functions for preheat, ignition and on-state operation of the lamp and also includes the EMI filter and the rectification stage. The circuit is built around the IR2520D Ballast Control IC. The IR2520D provides adjustable preheat time, adjustable run frequency to set the lamp power, high starting frequency for soft start and to avoid lamp flash, fault protection for open filament condition and failure to strike, low AC line protection and auto-restart after line brownout conditions and auto-restart after lamp replacement. The functionality of the IR2520D allows the component count for the complete ballast to be reduced down to 19 components.

Features of the ballast include programmable run frequency, programmable preheat time, open filaments and no-lamp protection, failure to strike and deactivated-lamp protection, low AC line protection, auto-restart after lamp replacement. The limits of these configuration are low PF, about 0.6 and high THD > 100%.

Fig. 7 shows the voltage across the lamp and the current in the resonant inductor at Startup and Fig. 8 shows the lamp voltage and the lamp current during running conditions. The Bill Of Materials (BOM) is shown in Table I.

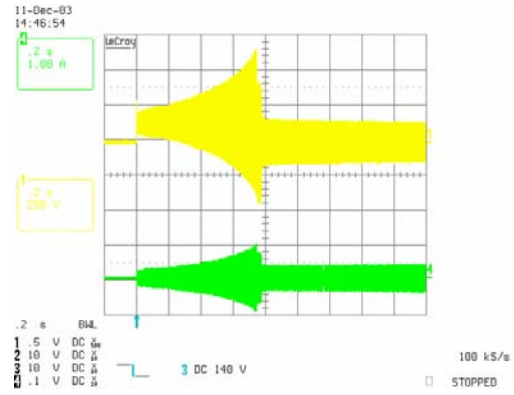


Figure 7. Voltage across the lamp (yellow) and current in the resonant inductor (green) at Startup

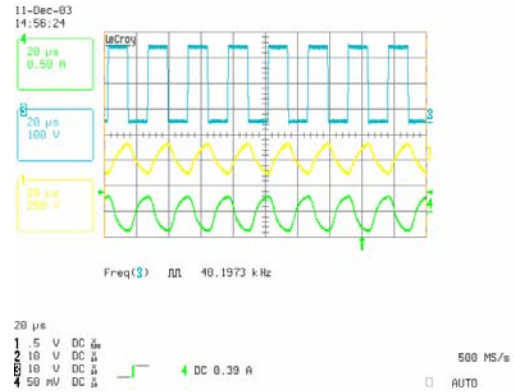


Figure 8. VS (HB) Voltage (blue), Lamp Voltage (yellow) and the Lamp Current (green) during Run Mode.

TABLE I

BOM Low PF Ballast, Lamp type: Spiral CFL 26W, Line Input Voltage: 190-240 VAC.

Description	Reference
Bridge Rectifier, 1A 1000V	BR1
Resistor, 0.5Ohm, 1/2W	F1
Capacitor, 0.1uF 275 VAC	CF
EMI Inductor, 1mH 370mA	LF
Capacitor, 47nF 400V	CDC
Capacitor, 10uF 350VDC 105C	CBUS
Capacitor, 0.1uF 50V 1206	CBS
Capacitor, 0.47uF 25V 1206	CVCO
Capacitor, 1uF 25V 1206	CVCC
Capacitor, 680pF 1KV SMT 1812	CSNUB
Capacitor, 4.7nF 1KV Polypropylene	CRES
IC, Ballast Driver IR2520D	IC BALLAST
Inductor, 2.25mH, 5%, 1Apk	LRES
Transistor, MOSFET IRFU430	MHS, MLS
Resistor, 1M, 1206, 100V	RSUPPLY1, RSUPPLY2
Resistor, 68.1K, 1%, 1206	RFIN
Diode, 1N4148 SMT DL35	DCP1, DCP2

V. HIGH POWER FACTOR BALLAST

In applications requiring high PF and low THD the circuit can be modified by adding an external active power factor correction front-end. This configuration allows for high PF (> 0.9) and low THD (< 10). The resulting circuit is shown in Fig. 9.

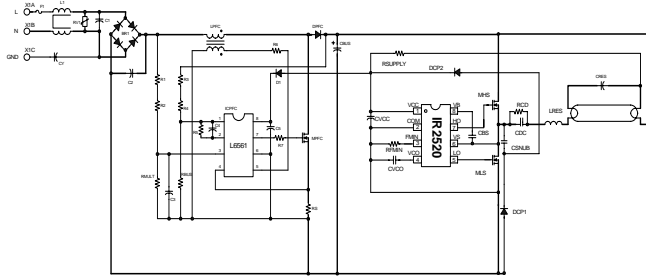


Figure 9. High PF Ballast using an external active PFC IC.

The circuit consists of an EMI filter, an active power factor correction front-end, a ballast control section and a resonant lamp output stage. The active power factor correction section is a boost converter operating in critical conduction, free-running frequency mode. The power factor front end provides regulated bus voltage, generally 400VDC. The ballast control section provides frequency modulation control of the traditional RCL lamp resonant output circuit and is easily adaptable to a wide variety of lamp types. This solution is better than alternative solutions from the performance point of view and can be used up to high power because a regulated and boosted bus voltage allow to limit the current in the HB FETs and maintain a good crest factor also with high load (this cannot be achieved using the following passive PFC configuration) and comply with EN-61000-3-2 also for high power (this is not verified with the low PF configuration.)

VI. PASSIVE POWER FACTOR BALLAST

A 14W CFL ballast has been designed and tested for performance. The circuit is shown in Fig. 10.

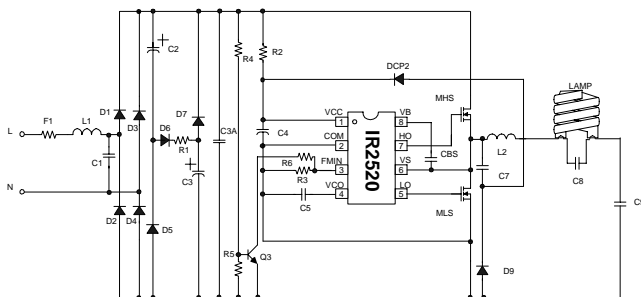


Fig. 10: Passive PF ballast using the IR2520D HVIC

The circuit is based on a resonant topology driven by a MOSFET half bridge. The circuit is controlled by the IR2520D Ballast Control IC that provides lamp preheat, lamp ignition, running mode and fault protection (lamp fault, open filaments, failure to strike, deactivated lamp and low AC line). To achieve high PF a Passive Valley Fill configuration has been used on the input stage, a diode and resistor has been added at the standard Passive Valley Fill configuration to reduce THD. High Crest Factor of the lamp current is intrinsic in a Passive Valley Fill Configuration because of the bus shape. The crest factor is very high because the bus voltage change between 2 different values, very different between each other: about V_{ACpk} and $\frac{1}{2} V_{ACpk}$. The current associated at the minimum bus voltage will be more than the double of the current associated to the maximum bus voltage and the intrinsic crest factor will be higher than 2. This is valid in case of constant frequency. Using a resistor to limit the harmonics increases the crest factor even further because the minimum bus voltage decreases.

To limit the crest factor an additional circuit (R5, R6, Q3 and R4) has been used to modulate the frequency of the Half Bridge versus the DC Bus Voltage value. The circuit increases the frequency when the DC bus increases above a threshold, limiting the crest factor of the current. With this configuration one can get $THD < 30\%$, $PF > 0.85$, Lamp Current Crest Factor I_{pk}/I_{rms} (CF) < 1.7 with input: 220-240VAC. The idea of the crest factor control method is to avoid constant frequency operation and to use 2 different frequencies: minimum frequency for minimum bus voltage and an higher frequency for maximum bus voltage. An higher frequency will cause a lower voltage and current on the lamp, decreasing the maximum value the current will reach at the maximum bus voltage. The crest factor control circuit generates 2 different frequencies adding a resistor R6 in parallel to the resistor R3 when the transistor Q3 is on. The new working frequency of the IR2520D will depend on the parallel between R6 and R3 and will be bigger than the frequency determined by R3 alone. The transistor Q3 will turn on when the voltage between base and emitter, which is determined by R5, will exceed the conduction threshold of the transistor Q3. Summarizing, when the bus is low the IR2520D will oscillate at the minimum frequency, determined by R3 and when instead the bus voltage exceeds a certain value (determined by R5 and R4), the IR2520D will oscillate at higher frequency, determined by the parallel of R3 and R6.

Fig. 11 shows the bus voltage shape, the lamp current and the lamp voltage. Table 2 shows the BOM

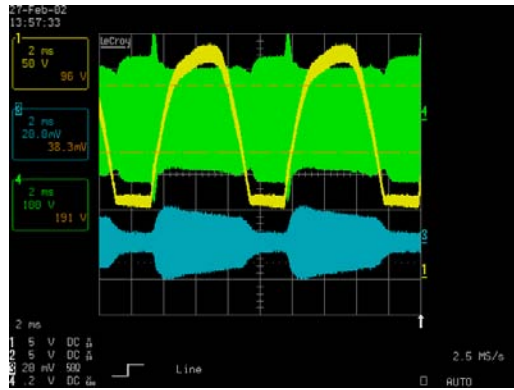


Figure 11. The bus voltage (in yellow), the lamp current (in blue) and the lamp voltage (in green).

TABLE II

BOM Passive PF Ballast, Lamp type: Spiral CFL 14W, Line Input Voltage: 200-240 VAC.

Description	Reference
Bridge Rectifier, 1A 1000V	BR1
Resistor, 0.5Ohm, 1/2W	F1
Capacitor, 0.1uF 275 VAC	CF
EMI Inductor, 1mH 370mA	LF
Capacitor, 47nF 400V	CDC
Capacitor, 10uF 350VDC 105C	CBUS
Capacitor, 0.1uF 50V 1206	CBS
Capacitor, 0.47uF 25V 1206	CVCO
Capacitor, 1uF 25V 1206	CVCC
Capacitor, 680pF 1KV SMT 1812	CSNUB
Capacitor, 4.7nF 1KV Polypropylene	CRES
IC, Ballast Driver IR2520D	IC BALLAST
Inductor, 2.25mH, 5%, 1Apk	LRES
Transistor, MOSFET IRFU430	MHS, MLS
Resistor, 1M, 1206, 100V	RSUPPLY1, RSUPPLY2
Resistor, 68.1K, 1%, 1206	RFMIN
Diode, 1N4148 SMT DL35	DCP1, DCP2

VII. DESIGN PROCEDURE

The quickest and easiest method to select the components values is in each case is to use version 4 (or higher) of the International Rectifier Ballast Design Assistant software which can be downloaded from IR's website at www.irf.com. The BDA supports the IR2520D. It can calculate approximate values of all external resistors and capacitors. These values may be used to make an initial breadboard type ballast setup. The final refining and obtaining of the exact component values must be carried out in the lab by experimentation.

Designing with the IR2520D is very simple because it only has 2 control pins: VCO (0-5VDC oscillator voltage input) and FMIN (minimum frequency setting). To modify the design for a higher lamp power, you will need to modify RFMIN, CVCO, LRES and CRES. Make sure that the FETs and inductors are rated for the current you need with the new

lamp and that VCC is stable. To modify the design to a lower lamp power, you will need to decrease RFMIN and, in some cases, to also modify CVCO, LRES and CRES. In most cases you can use FETs and inductors with lower current ratings.

The FMIN pin is connected to ground through a resistor (RFMIN). The value of this resistor programs the minimum frequency (fmin) of the IC and the starting frequency of the IC (about 2.5xfmin). The IR252D will work in run mode at the minimum frequency unless non-ZVS is detected. Generally, to work with constant frequency, the minimum frequency needs to be chosen above the resonant frequency of the low-Q R-C-L circuit. In this case, one can increase the value of RFMIN to decrease the frequency and increase the lamp power, or, decrease the value of RFMIN to increase the run frequency and decrease the lamp power.

The VCO pin is connected to ground through a capacitor (CVCO). The value of this capacitor programs the time the frequency needs to ramp down from 2.5 times fmin to fmin. One can increase the capacitor value to increase the preheat time, or, decrease the capacitor value to decrease the preheat time.

The suggested design procedure is as follows:

- 1) Use the Ballast Design Assistant (BDA) software to calculate LRES, CRES, RFMIN and CVCO. Select the input configuration without PFC or with PFC, select the IR2520D and select single lamp current mode configuration. Select the new lamp in the database or add the lamp parameters by hand selecting the "Advanced" option. Calculate the operating point and chose the right values of L and C that satisfy:
 - 1.1) Run frequency (best working range) 40-50KHz
 - 1.2) C as small as possible to minimize losses (suggested value 4.7nF)
 - 1.3) L values you have available
- 2) While measuring LO, apply 15V between the VCC pin and the COM pin and adjust the value of RFMIN to obtain the right minimum frequency (it is suggested set fmin = run frequency obtained with the BDA software). Increase RFMIN to decrease the minimum frequency or decrease RFMIN to increase the minimum frequency.
- 3) Apply the AC input and check preheat, ignition and run states of the lamp.
 - 3.1) If the IC works at a frequency greater than fmin, increase CRES or LRES to decrease the resonant frequency avoiding hard-switching
 - 3.2) If VCC drops, increase the value of CSNUBBER
- 4) Adjust the value of RFMIN to have the right power on the lamp (increase RFMIN to increase power or decrease RFMIN to decrease power) and the value of CVCO to set the correct preheat time (increase

CVCO to increase the preheat time and decrease CVCO to decrease the preheat time).

- 5) Select the value of RSUPPLY to have startup at the correct AC line voltage. Increase the value of RSUPPLY to start the IC at higher AC voltages and decrease the value of RSUPPLY to start the IC at lower AC voltages.
- 6) Test your lamp life (number of starts). A good design should guarantee at least 5,000 starts. To increase the number of starts, increase CRES or the preheat time (CVCO).

Key point on the Passive Valley Fill Design:

- 1) Select the minimum frequency (f_{min}) to have Input Power slightly higher than the input power needed
- 2) R1 reduces the THD and the harmonics related to Passive Valley Fill configuration:
Start with $R1=0$ and increase R1 until THD is inside the spec. Higher R1 will cause lower minimum bus voltage and so higher crest factor of the current and can cause multiple ignition on the lamp, so R1 should be selected as low as possible.
- 3) R5 set the bus voltage threshold value. When the bus voltage exceed this threshold, the Half Bridge frequency will start to increase above f_{min}
Adjust the value of R5 so that the Vbus threshold is selected around $(V_{bus\ max} - V_{bus\ min}) / 2$
- 4) R6 set the maximum frequency when the bus voltage is maximum, determined by R3 parallel R6

VIII. CONCLUSIONS

The IR2520D is a very versatile and flexible building block to design the typical functions of electronic ballast in a cheap and easy way. In this paper three different circuits have been discussed: low PF ballast is low end low cost, passive PFC ballast is medium end medium cost and active PFC ballast is high-end higher cost. The right solution can be chosen based on a trade-off between performance needs (PF, Crest Factor and THD requirements) and cost requirements. Table III shows a comparison between the three circuits.

Table III
Comparison PF Circuits

LOW PF	PASSIVE VALLEY FILL	ACTIVE PF
THD > 100%	THD < 30%	THD < 10%
PF around 0.55	PF around 0.95	PF > 0.98
Limited AC Input Range	Limited AC Input Range	Wide AC Input Range
- Bad Harmonics - Low PF + Cost	-Excessive HB current and difficult ignition at minimum bus voltage (power limitation)	-Cost + PF and THD performance
-no Power regulation vs AC line	Difficult to conform to EN61002-3 for single harmonics	

REFERENCES

- [1] *IR2520D Ballast Control IC Datasheet, International Rectifier 2004*
- [2] *IRPLCFL5E Reference Design, International Rectifier 2004*
- [3] *IRPLMB1E Reference Design, International Rectifier 2004*
- [4] *AN1066, 220V CFL design with the IR2520D, International Rectifier 2004*
- [5] *Ballast Design Software, PCIM Europe 2002*