International
IOR Rectifier

Dec. 13, 2009

Automotive Grade AUIRS211(0,3)S

HIGH- AND LOW-SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +500 V or +600 V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V input logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground ±5 V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Output in phase with inputs
- Leadfree, roHS Compliant
- Automotive qualified*

Typical Applications

- Hybrid electric vehicles
- Air condition drives, pumps, fans
- Automotive general purpose dual LS/HS driver
- Automotive motor drives
- Automotive DC/DC converters
- Automotive injection control

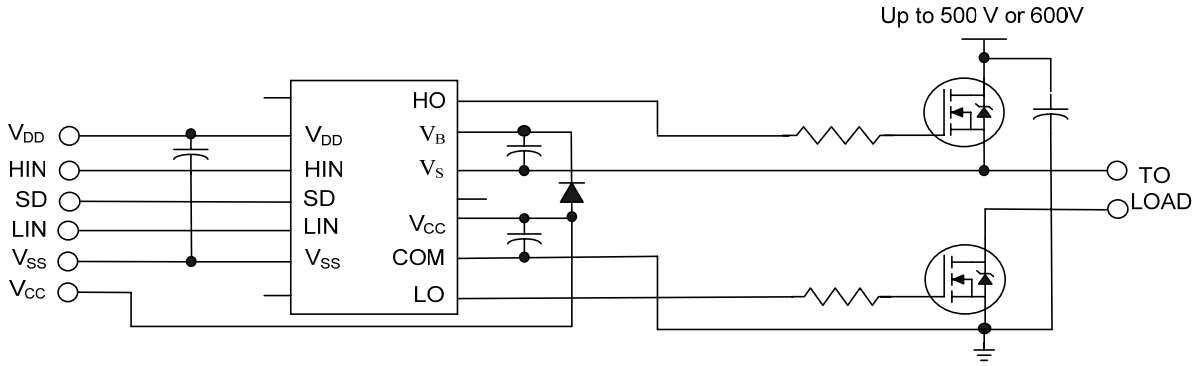
Product Summary

Topology		2 channels
V_{OFFSET}	AUIRS2110	500 V max
	AUIRS2113	600 V max
V_{OUT}		10 V – 20 V
I_{o+} & I_{o-} (typical)		2.5 A / 2.5 A
t_{ON} & t_{OFF} (typical)		140 ns & 120 ns
Delay Matching (max.)		35 ns max

Package Option

16-Lead SOIC
AUIRS211(0,3)S

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

Description

The AUIRS211(0,3)S are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 V or 600 V.

Qualification Information†

Qualification Level		Automotive (per AEC-Q100††)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC16W	MSL3††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (Pass +/-200V) (per AEC-Q100-003)	
	Human Body Model	Class H1B (Pass +/-1000V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/
†† Exceptions to AEC-Q100 requirements are noted in the qualification report.
††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating supply voltage	(AUIRS2110)	-0.3	520 (†)	V
		(AUIRS2113)	-0.3	620 (†)	
V_S	High-side floating supply offset voltage		V_B - 20	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side fixed supply voltage		-0.3	20	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage		-0.3	V_{SS} + 20 (†)	
V_{SS}	Logic supply offset voltage		V_{CC} - 20	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS} -0.3	V_{DD} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (Fig. 2)		—	50	V/ns
P_D	Package power dissipation @ TA ≤ 25°C		—	1.25	W
Rth_{JA}	Thermal resistance, junction to ambient		—	100	°C/W
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

† All supplies are fully tested at 25 V, and an internal 20 V clamp exists for each supply.

Recommended Operating Conditions

The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15 V differential.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating supply absolute voltage		V_S +10	V_S +20	V
V_S	High-side floating supply offset voltage	(AUIRS2110)	†	500	
		(AUIRS2113)	†	600	
V_{HO}	High-side floating output voltage		V_S	V_B	
V_{CC}	Low-side fixed supply voltage		10	20	
V_{LO}	Low-side output voltage		0	V_{CC}	
V_{DD}	Logic supply voltage		V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic ground offset voltage		-5 (††)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS}	V_{DD}	
T_A	Ambient temperature		-40	125	°C

† Logic operational for V_S of -4 V to +500 V. Logic state held for V_S of -4 V to – V_{BS}. (Please refer to the Design Tip DT97 -3 for more details).

†† When V_{DD} < 5 V, the minimum V_{SS} offset is limited to $-V_{DD}$.

Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V, V_{SS} = COM. The V_{IL}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O, and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	9.5	—	—	V	
V_{IL}	Logic "0" input voltage	—	—	6.0		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.4		I_O = 0 A
V_{OL}	Low level output voltage, V_O	—	—	0.15		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 500 V/600 V
I_{QBS}	Quiescent V_{BS} supply current	—	70	130		V_{IN} = 0 V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	—	125	230		
I_{QDD}	Quiescent V_{DD} supply current	—	5	30		
I_{IN+}	Logic "1" input bias current	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" input bias current	—	—	5.0		V_{IN} = 0 V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current (†)	2.0	2.5	—	A	V_O = 0 V, V_{IN} = V_{DD} PW ≤ 10 us
I_{O-}	Output low short circuit pulsed current(†)	2.0	2.5	—		V_O = 15 V, V_{IN} = 0 V PW ≤ 10 us

(†) Guaranteed by design

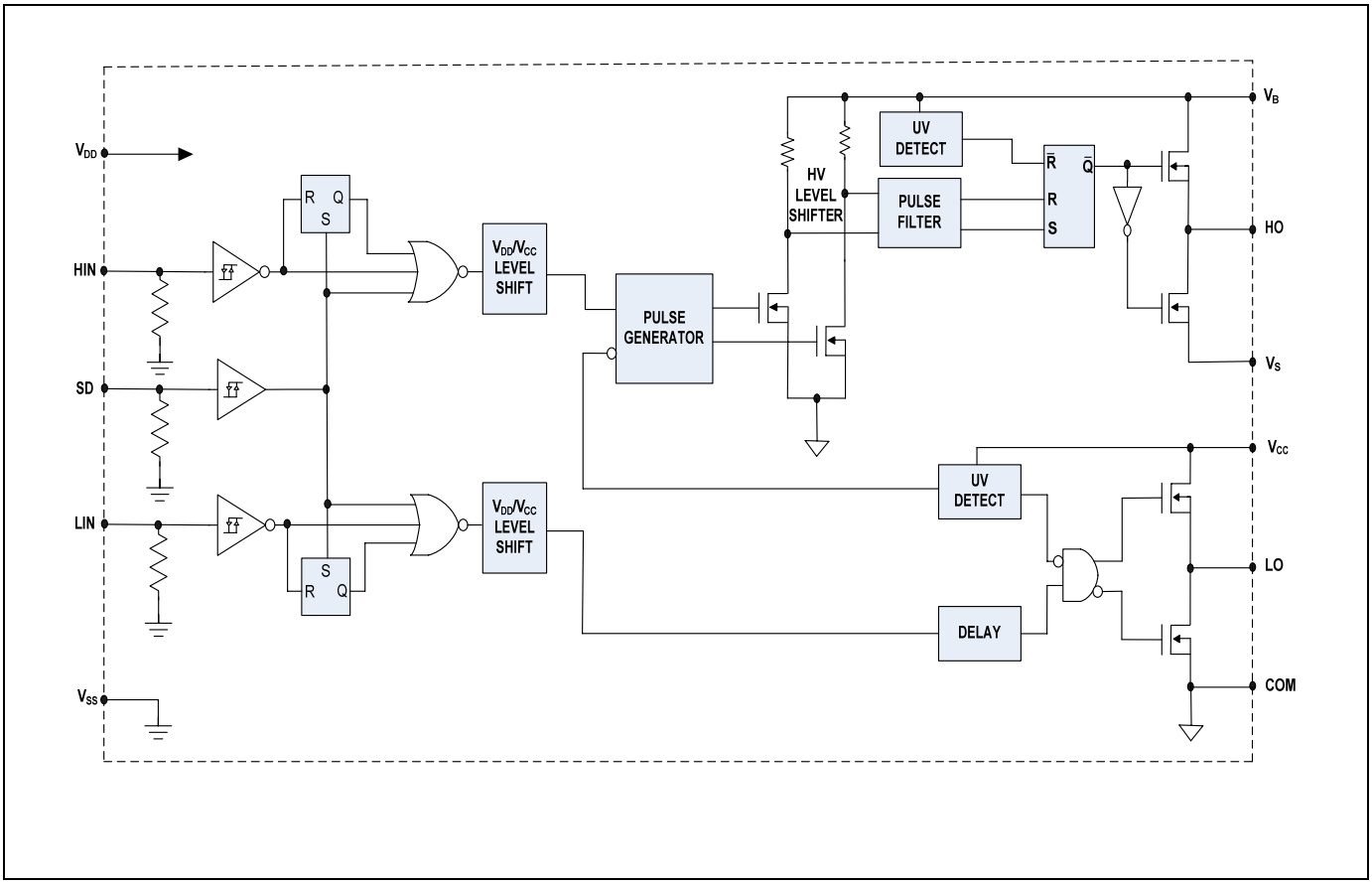
Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V, C_L = 1000 pF, and V_{SS} = COM. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

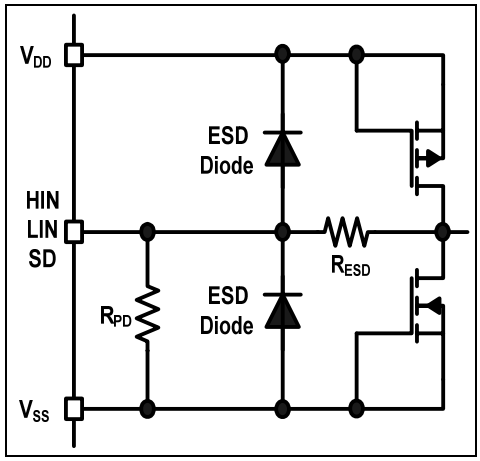
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	140	230	ns	V_S = 0 V
t_{off}	Turn-off propagation delay	—	120	210		V_S = 500 V/600 V
t_{sd}	Shutdown propagation delay	—	125	220		
t_r	Turn-on rise time	—	25	40		
t_f	Turn-off fall time	—	15	30		
MT	Delay matching, HS & LS turn on/off	—	—	35		

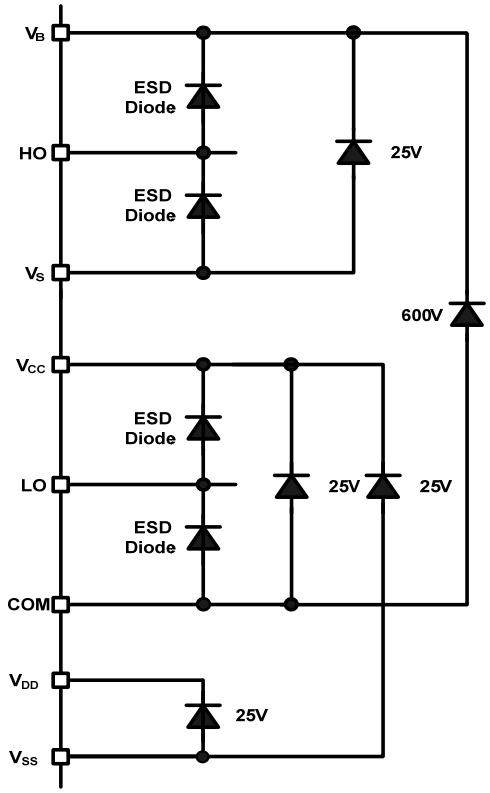
Note: Please refer to figures in Parameter Temperature Trends section

Functional Block Diagram



Input/Output Pin Equivalent Circuit Diagrams

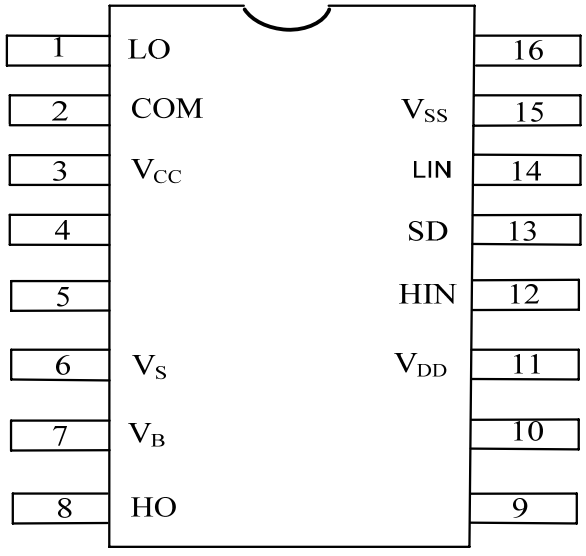




Lead Definitions

Pin	Symbol	Description
1	LO	Low-side gate drive output
2	COM	Low-side return
3	V_{CC}	Low-side supply
4	NC	Not connected
5	NC	Not connected
6	V_S	High-side floating supply return
7	V_B	High-side floating supply
8	HO	High-side gate drive output
9	NC	Not connected
10	NC	Not connected
11	V_{DD}	Logic supply
12	HIN	Logic input for high-side gate driver output (HO), in phase
13	SD	Logic input for shutdown
14	LIN	Logic input for low-side gate driver output (LO), in phase
15	V_{SS}	Logic ground
16	NC	Not connected

Lead Assignments



16 Lead SOIC (Wide Body)

AUIRS2110S/AUIRS2113S

Part Number

Application Information and Additional Details

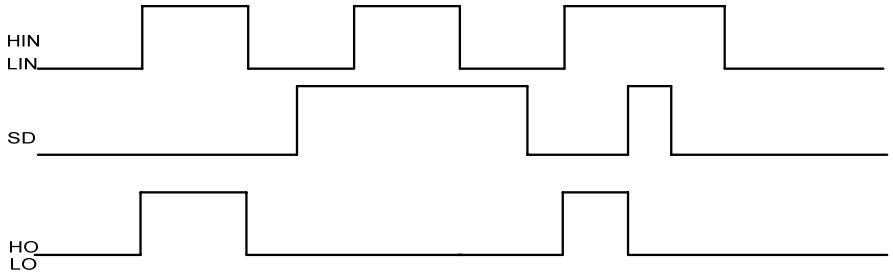


Figure 1: Input/Output Timing Diagram

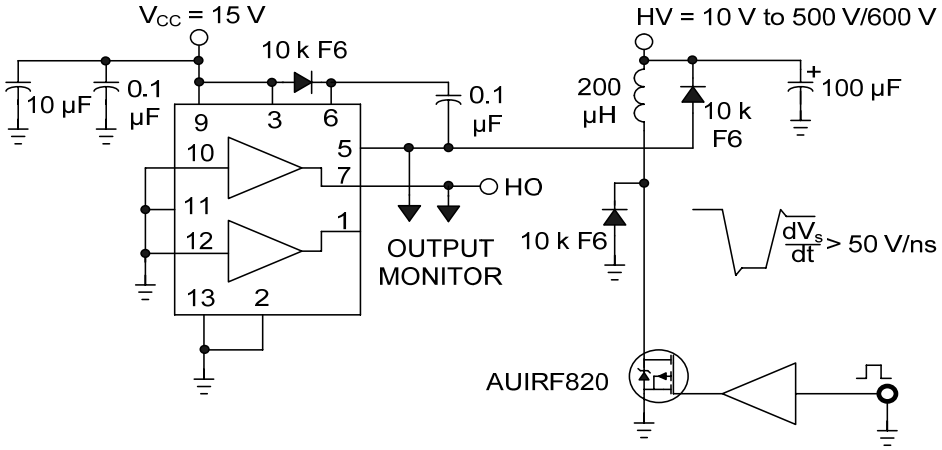


Figure 2: Floating Supply Voltage Transient Test Circuit

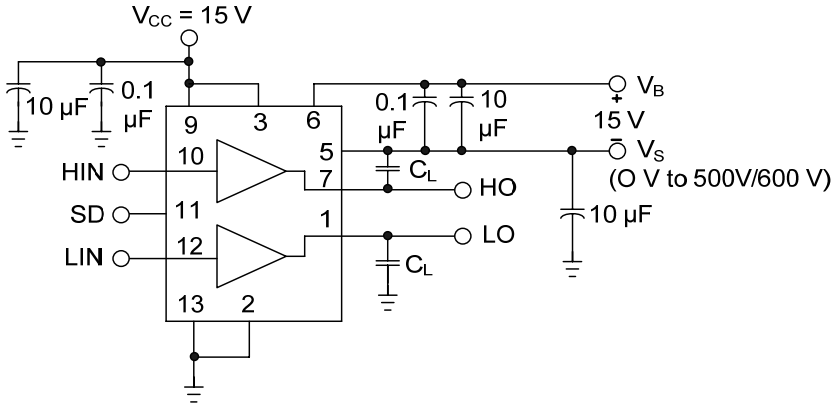


Figure 3: Switching Time Test Circuit

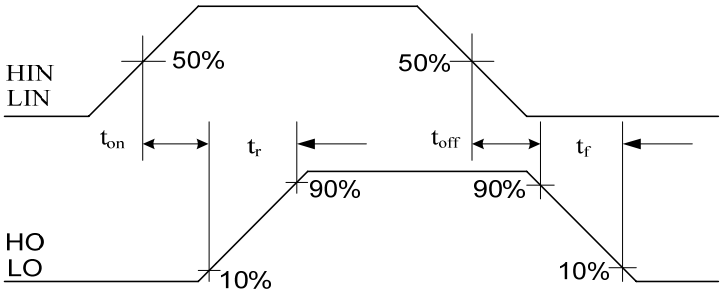


Figure 4: Switching Time Waveform Definitions

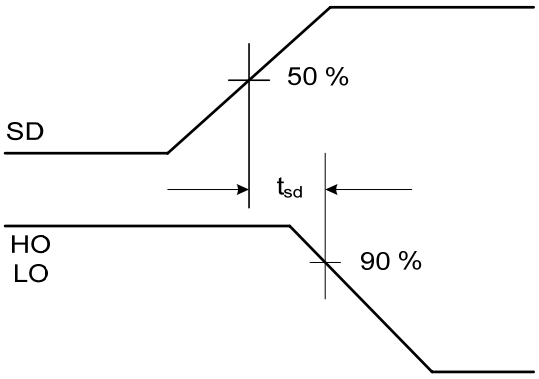


Figure 5: Shutdown Waveform Definitions

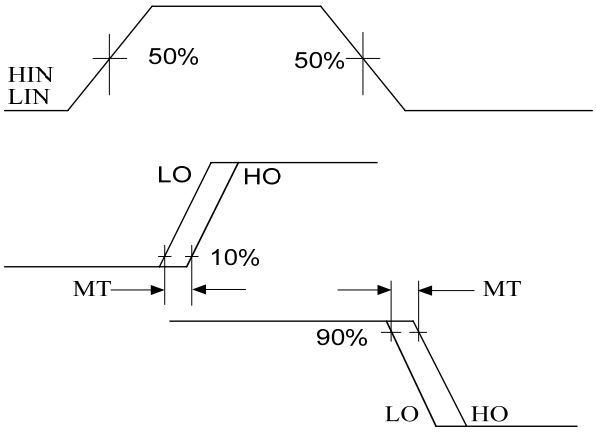


Figure 6: Delay Matching Waveform Definitions

Parameter Temperature Trends

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS211(0,3)S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

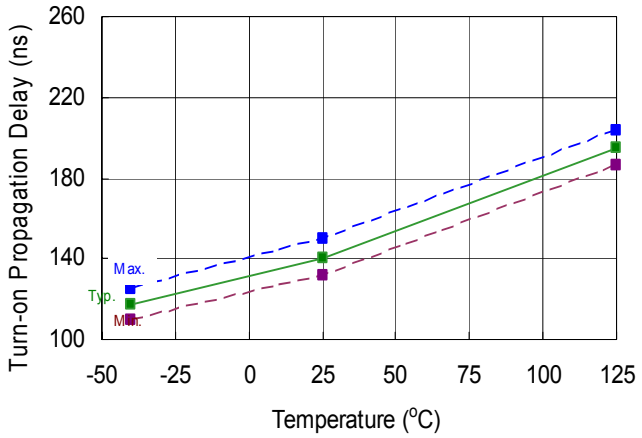


Figure 7. Turn-On Time vs. Temperature

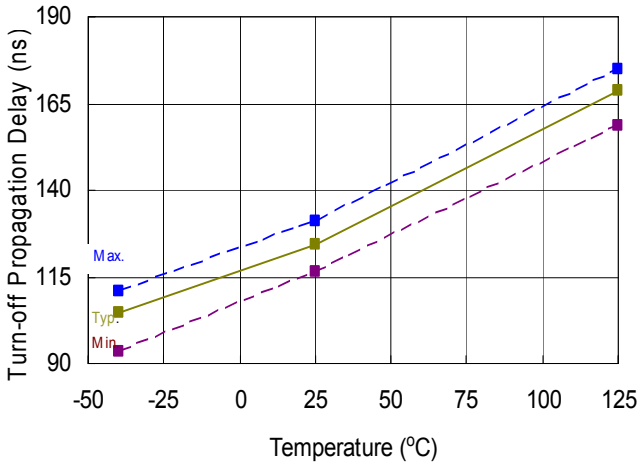


Figure 8. Turn-Off Time vs. Temperature

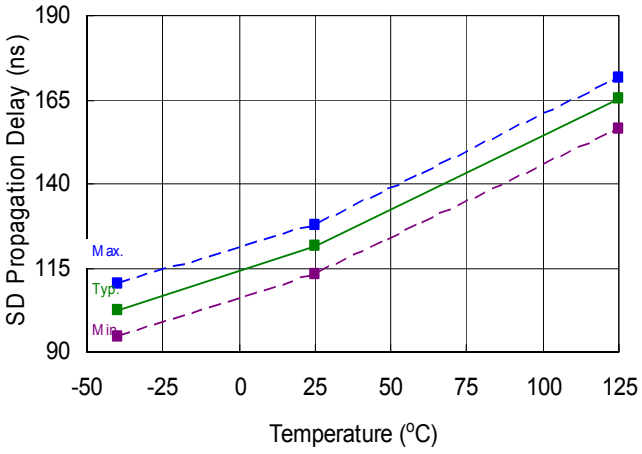


Figure 9. Shutdown Time vs. Temperature

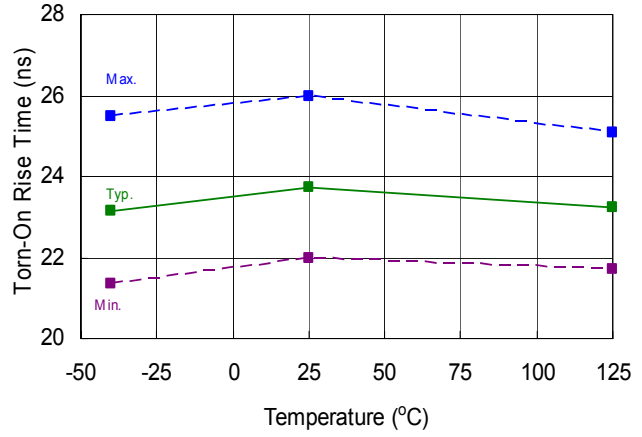


Figure 10. Turn-On Rise Time vs. Temperature

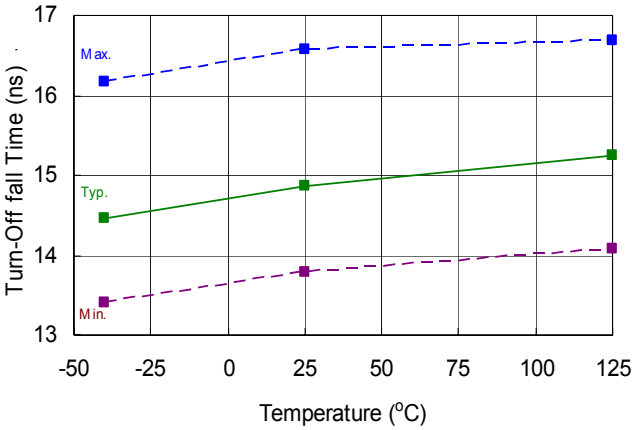


Figure 11. Turn-Off Fall Time vs. Temperature

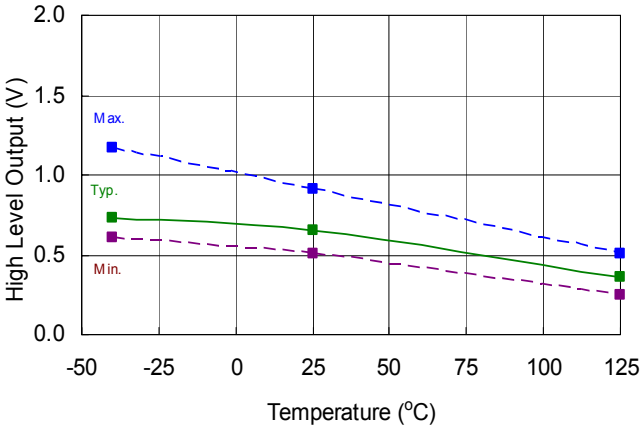


Figure 12. High Level Output Voltage vs. Temperature (I_O = 0 mA)

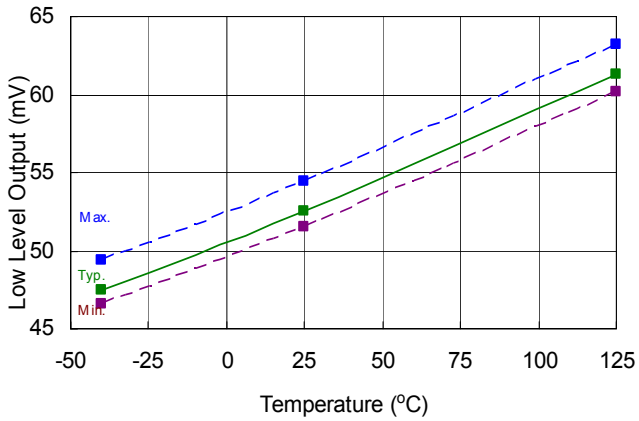


Figure 13. Low Level Output vs. Temperature

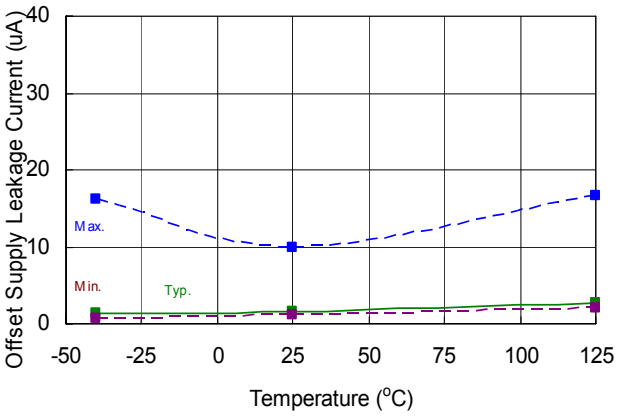


Figure 14. Offset Supply Current vs. Temperature

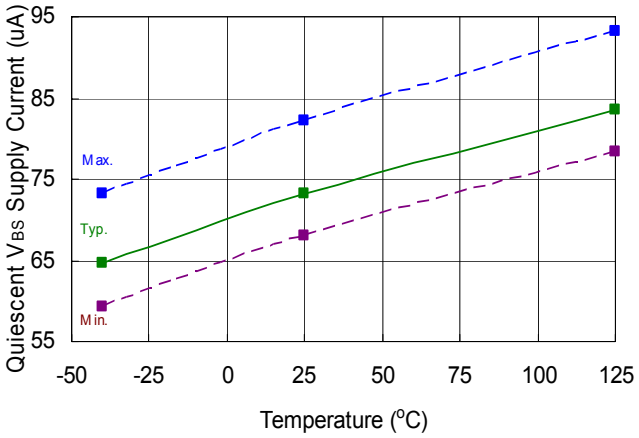


Figure 15. V_{BS} Supply Current vs. Temperature

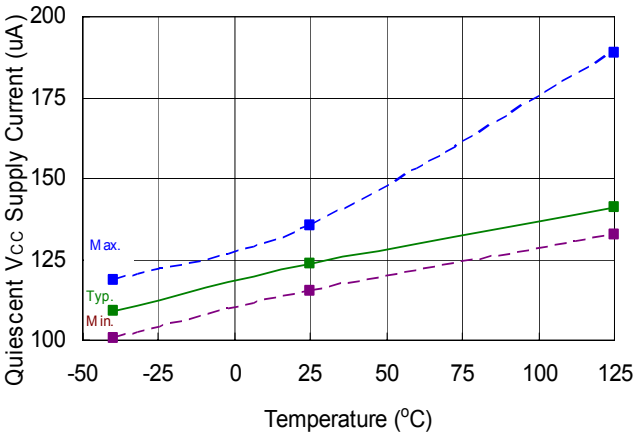


Figure 16. V_{CC} Supply Current vs. Temperature

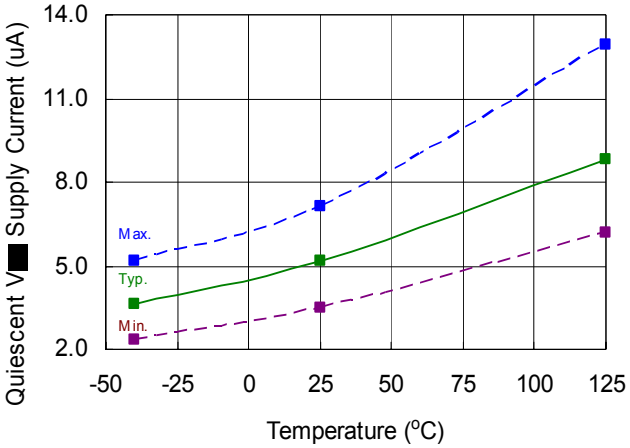


Figure 17. V_{DD} Supply Current vs. Temperature

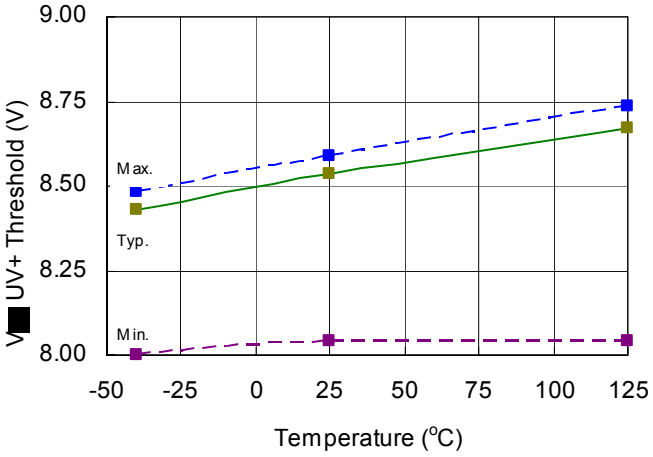


Figure 18. V_{BS} Undervoltage (+) vs. Temperature

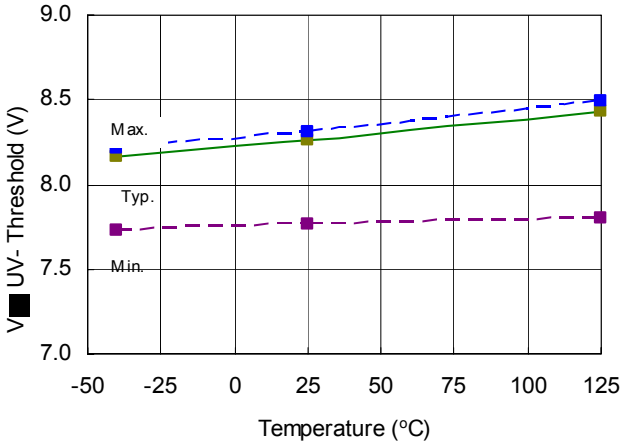


Figure 19. V_{BS} Undervoltage (-) vs. Temperature

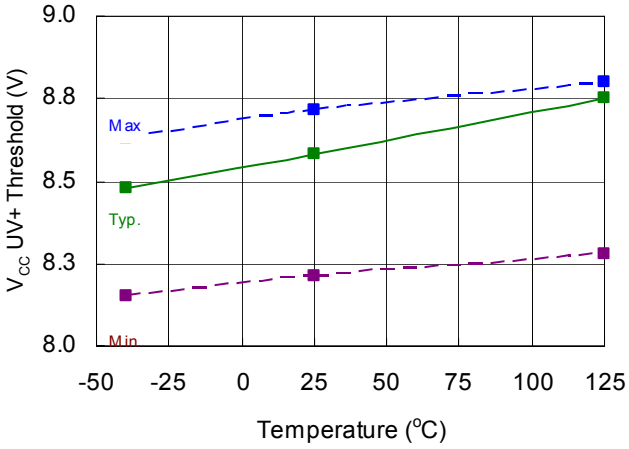


Figure 20. V_{CC} Undervoltage (+) vs. Temperature

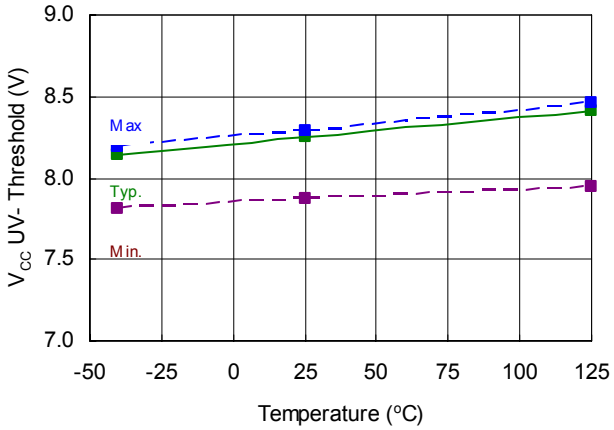
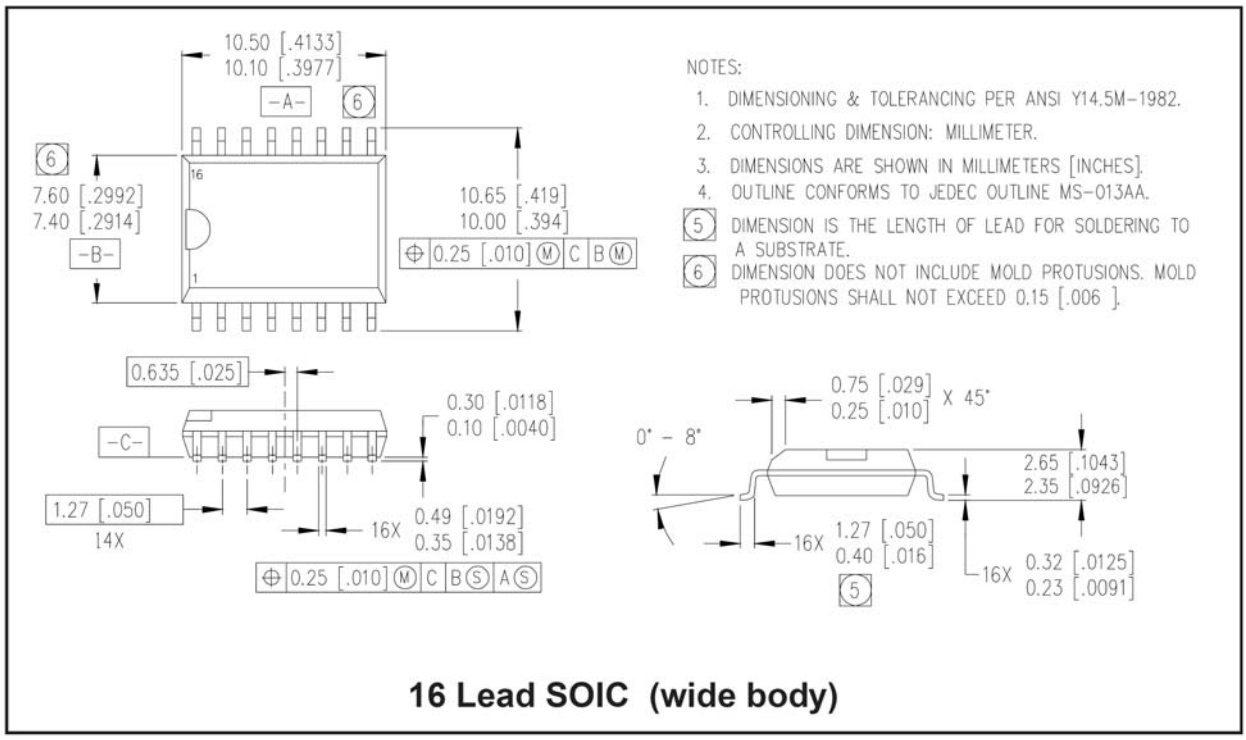


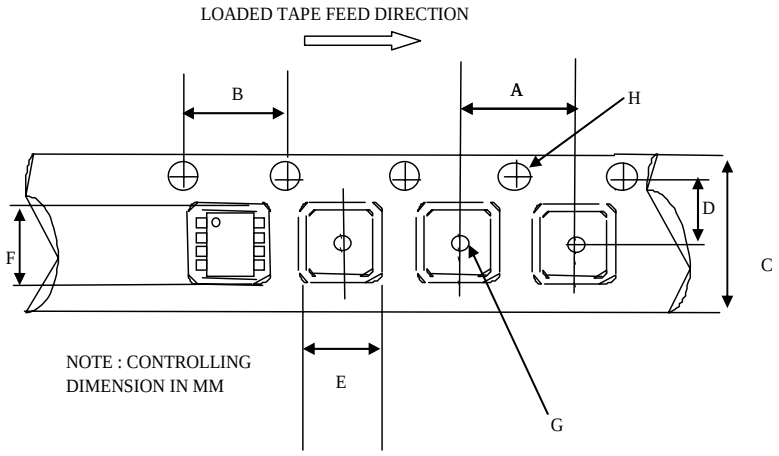
Figure 21. V_{CC} Undervoltage (-) vs. Temperature

Package Details: SOIC16WB



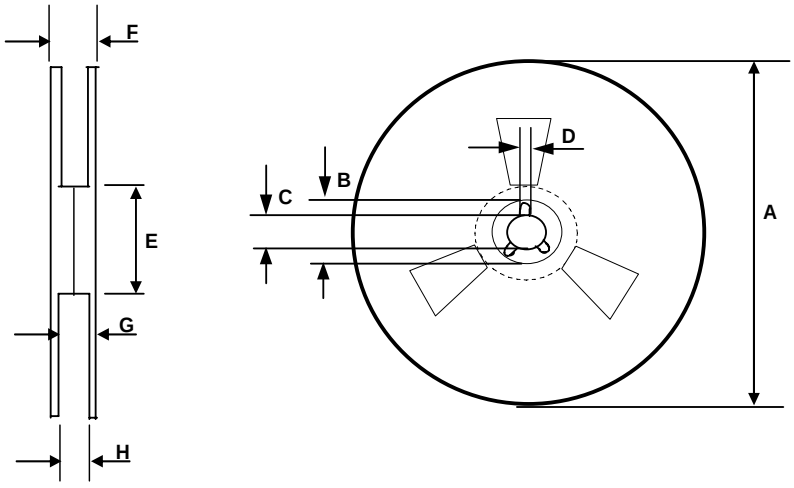
16 Lead SOIC (wide body)

Tape and Reel Details: SOIC16WB



CARRIER TAPE DIMENSION FOR 16SOICN

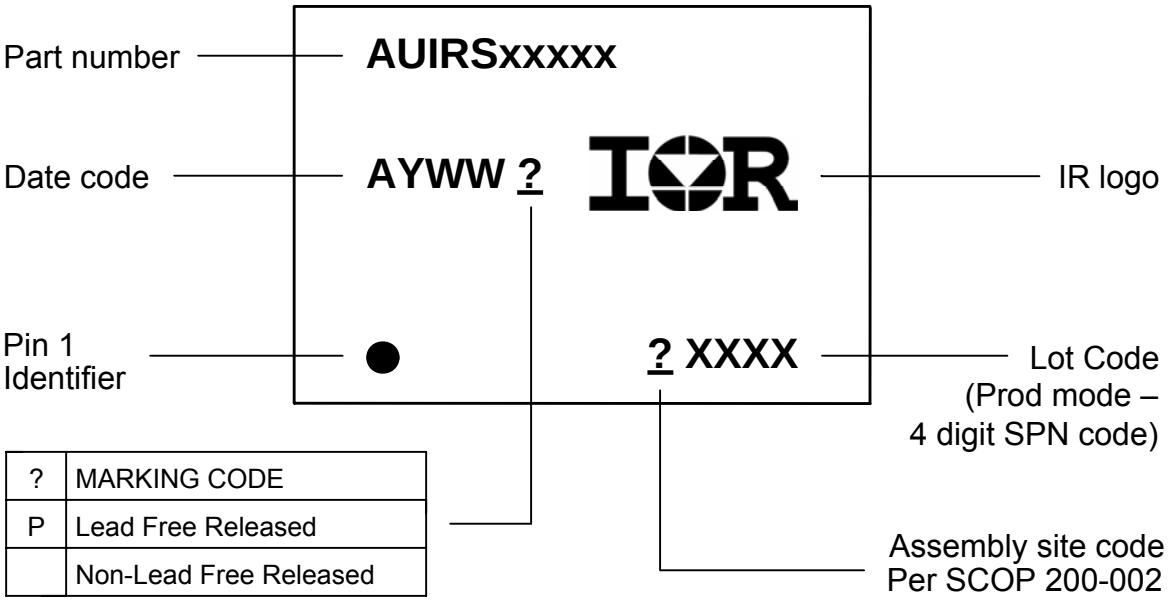
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2110S	SOIC16W	Tube/Bulk	25	AUIRS2110S
		Tape and Reel	***1000***	AUIRS2110STR
AUIRS2113S	SOIC16W	Tube/Bulk	25	AUIRS2113S
		Tape and Reel	***1000***	AUIRS2113STR

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