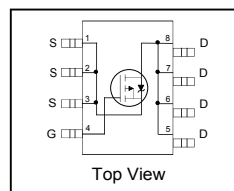


Features

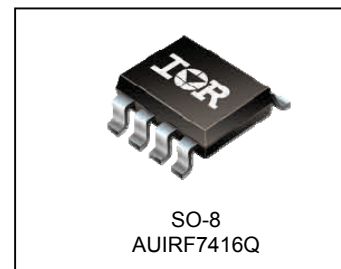
- Advanced Process Technology
- Low On-Resistance
- Logic Level Gate Drive
- P Channel MOSFET
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free, RoHS Compliant
- Automotive Qualified *

Description

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



V_{DSS}	-30V
$R_{DS(on)}$ max.	0.02Ω
I_D	-10A



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF7416Q	SO-8	Tape and Reel	4000	AUIRF7416QTR

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ $T_A = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ -10V	-10	A
I_D @ $T_A = 70^\circ\text{C}$	Continuous Drain Current, V_{GS} @ -10V	-7.1	
I_{DM}	Pulsed Drain Current ①	-45	
P_D @ $T_A = 25^\circ\text{C}$	Maximum Power Dissipation	2.5	W
	Linear Derating Factor	0.02	mW/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	370	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	50	°C/W

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*Qualification standards can be found at www.infineon.com

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.024	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.020	Ω	$V_{GS} = -10V, I_D = -5.6A$ ④
		—	—	0.035		$V_{GS} = -4.5V, I_D = -2.8A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.04	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Trans conductance	5.6	—	—	S	$V_{DS} = -10V, I_D = -2.8A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -24V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

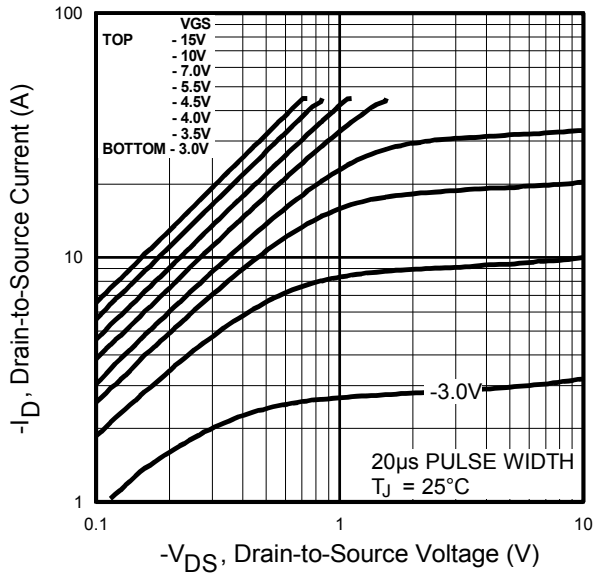
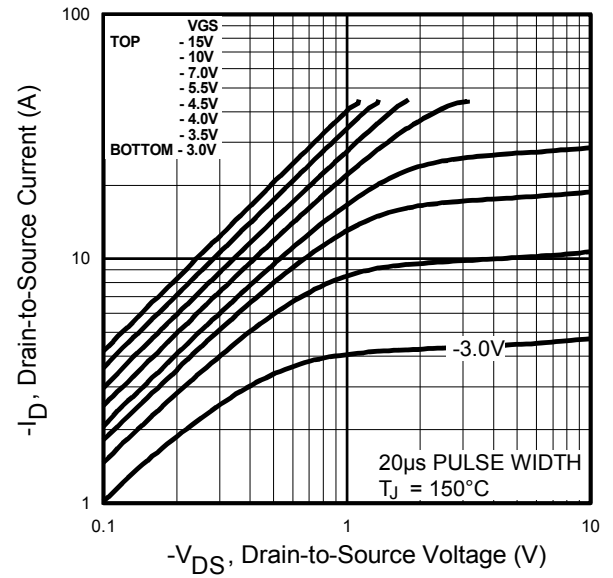
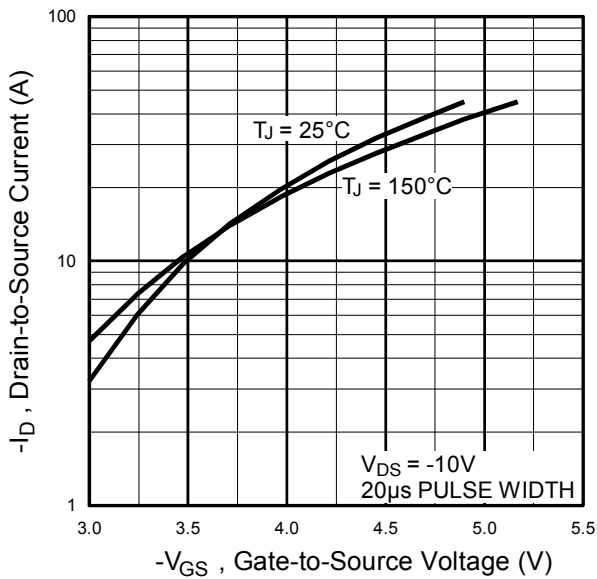
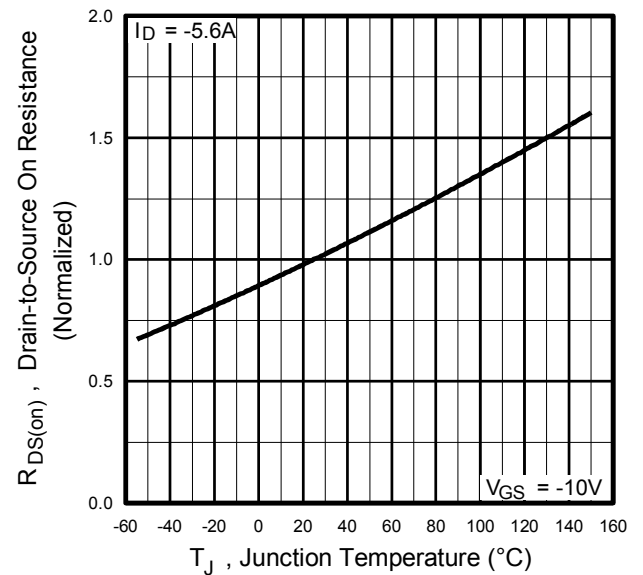
Q_g	Total Gate Charge	—	61	92	nC	$I_D = -5.6A$
Q_{gs}	Gate-to-Source Charge	—	8.0	12		$V_{DS} = -24V$
Q_{gd}	Gate-to-Drain Charge	—	22	32		$V_{GS} = -10V$, See Fig.6 & 9 ④
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = -15V$
t_r	Rise Time	—	49	—		$I_D = -5.6A$
$t_{d(off)}$	Turn-Off Delay Time	—	59	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	60	—		$R_D = 2.7\Omega$, See Fig.10 ④
C_{iss}	Input Capacitance	—	1700	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	890	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	410	—		$f = 1.0\text{MHz}$, See Fig.5

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-3.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-45		
V_{SD}	Diode Forward Voltage	—	—	-1.0	V	$T_J = 25^\circ\text{C}, I_S = -5.6A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	56	85	ns	$T_J = 25^\circ\text{C}, I_F = -5.6A$,
Q_{rr}	Reverse Recovery Charge	—	99	150	nC	$di/dt = 100A/\mu s$ ④

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 25\text{mH}$, $R_G = 25\Omega$, $I_{AS} = -5.6A$. (See Fig. 12)
- ③ $I_{SD} \leq -5.6A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance Vs. Temperature

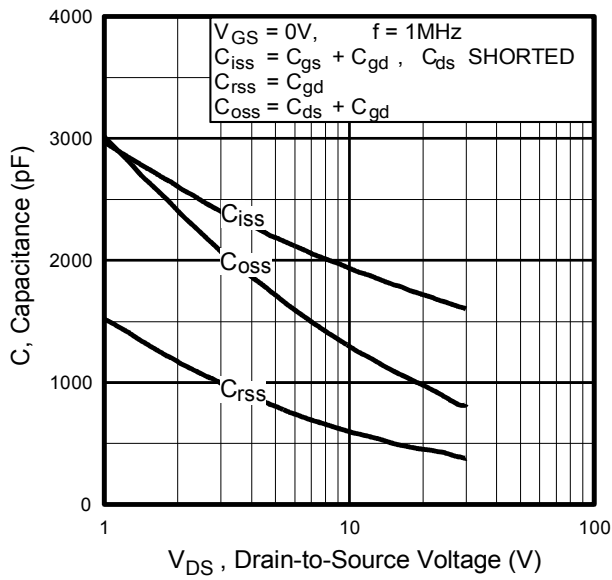


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

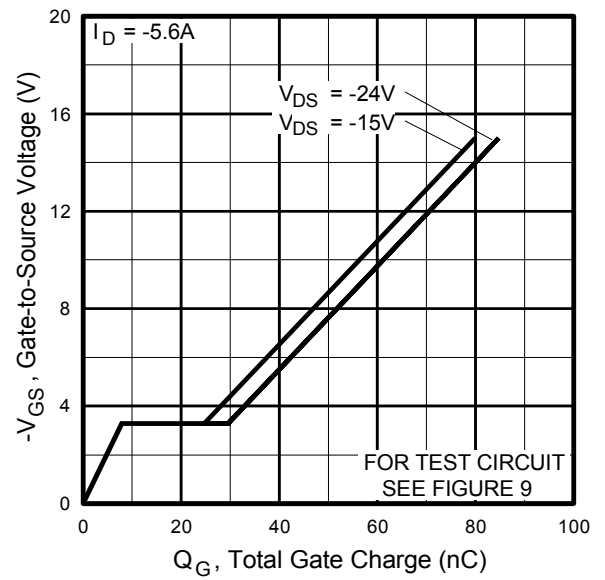


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

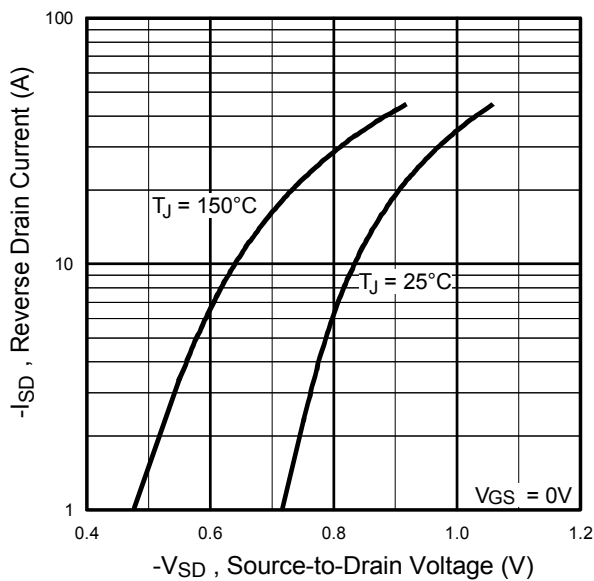


Fig. 7 Typical Source-Drain Diode Forward Voltage

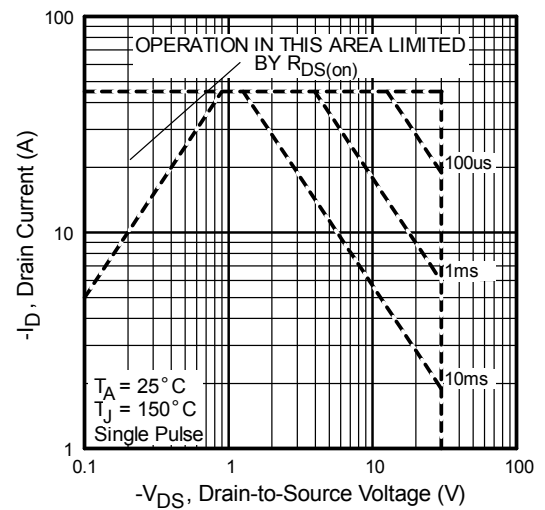
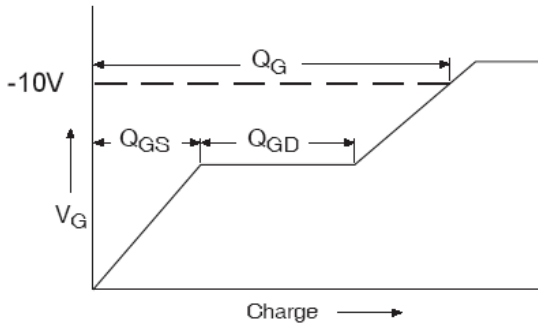
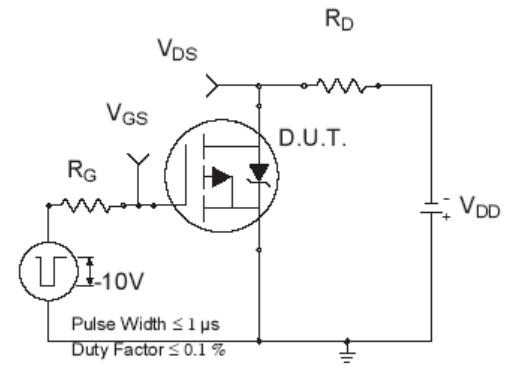
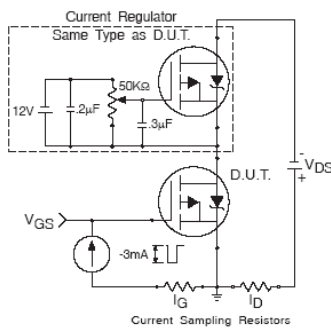
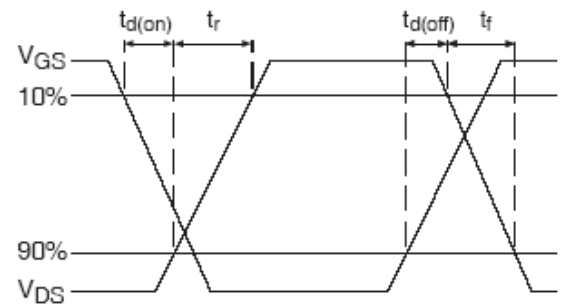
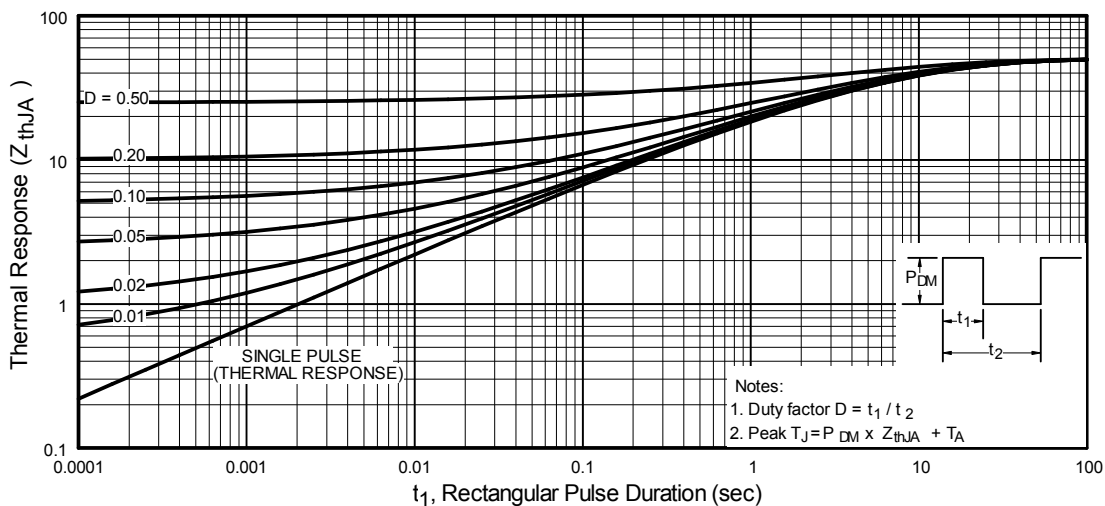


Fig 8. Maximum Safe Operating Area


Fig 9a. Gate Charge Waveform

Fig 10a. Switching Time Test Circuit

Fig 9b. Gate Charge Test Circuit

Fig 10b. Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

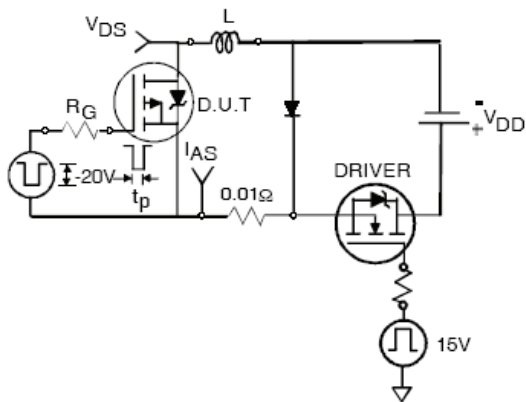


Fig 12a. Unclamped Inductive Test Circuit

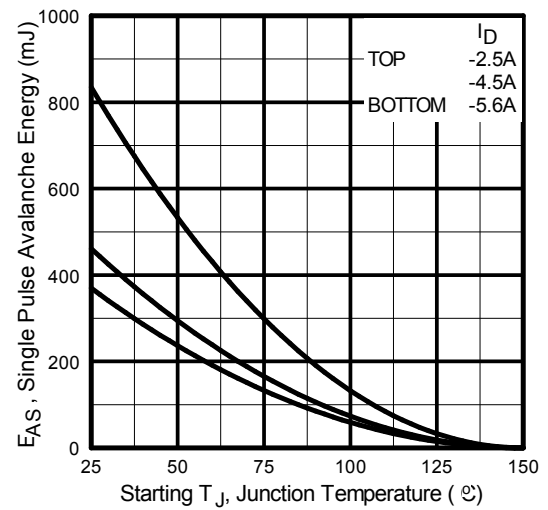


Fig 12c. Maximum Avalanche Energy vs. Drain Current

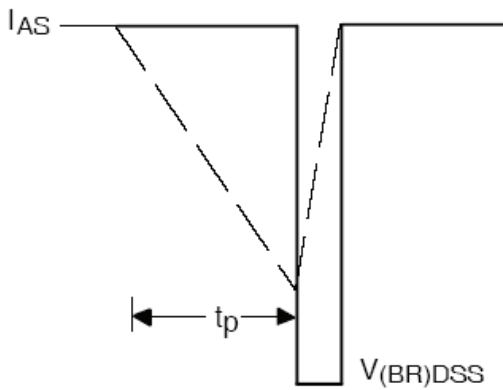


Fig 12b. Unclamped Inductive Waveforms

Peak Diode Recovery dv/dt Test Circuit

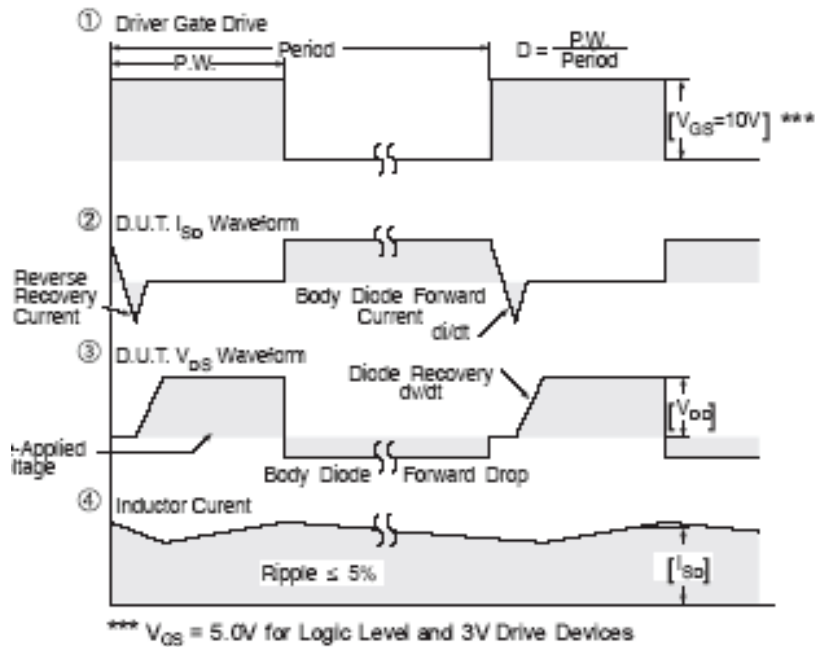
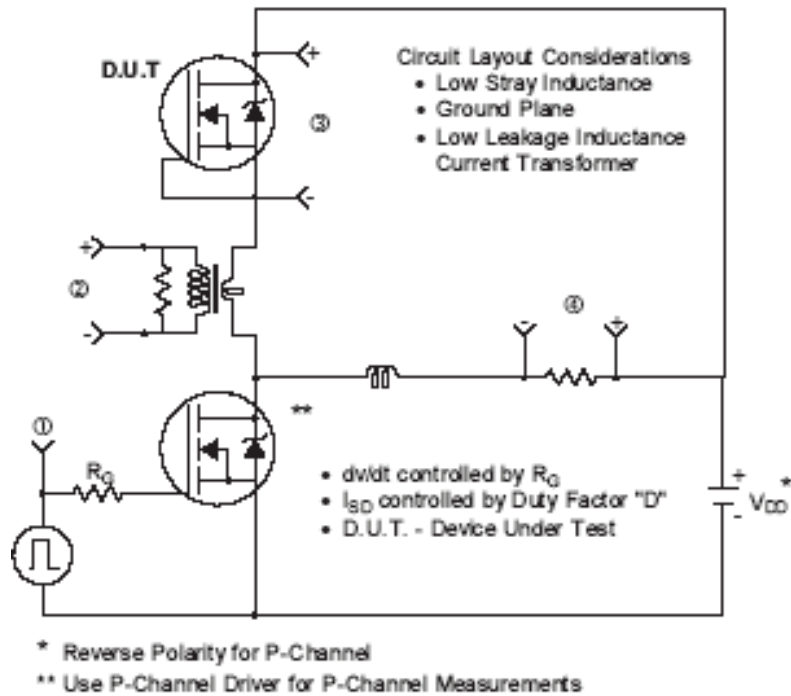
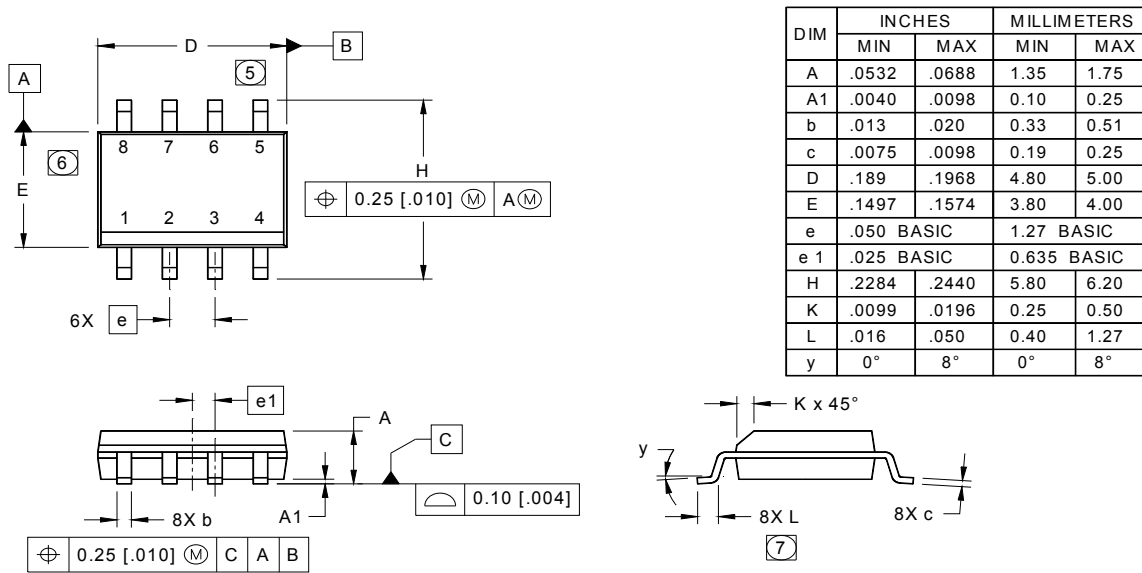


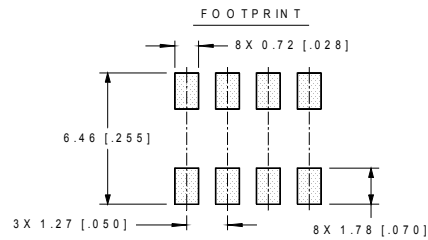
Fig 13. Peak Diode Recovery dv/dt Test Circuit for P-Channel HEXFET® Power MOSFETs

SO-8 Package Outline (Dimensions are shown in millimeters (inches))

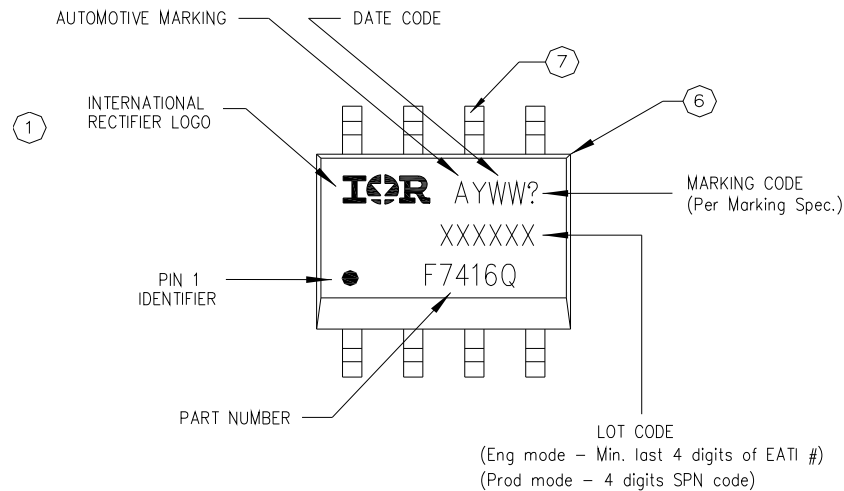


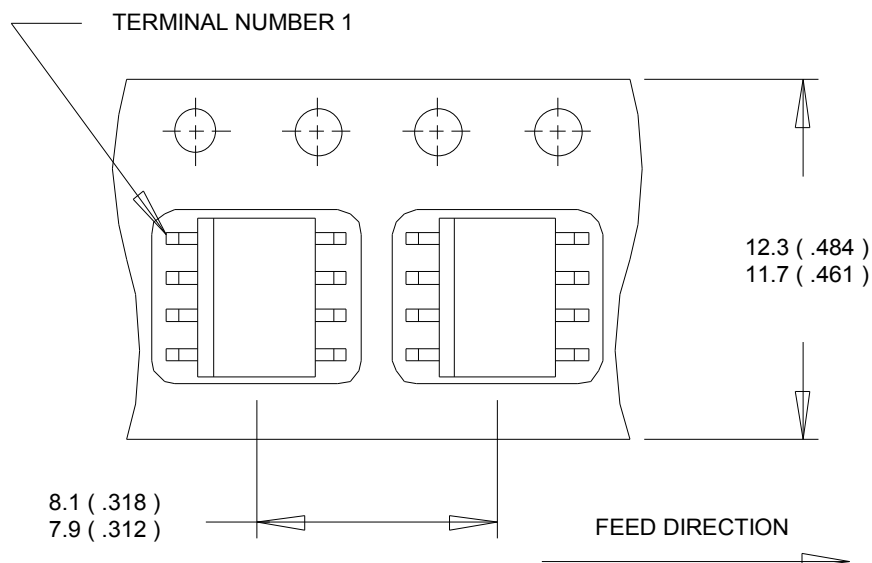
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

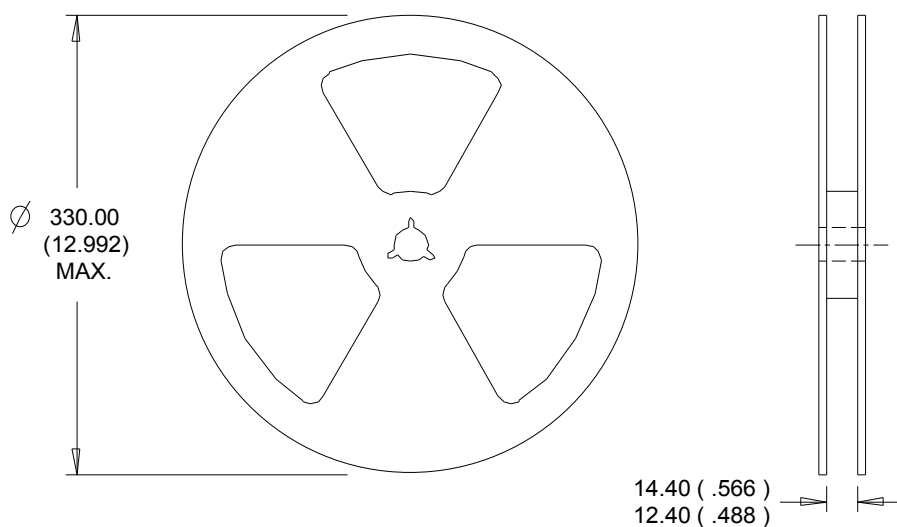


SO-8 Part Marking Information



SO-8 Tape and Reel (Dimensions are shown in millimeters (inches))

NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SO-8	MSL1
ESD	Machine Model	Class M4 (+/- 425V) [†] AEC-Q101-002	
	Human Body Model	Class H1B (+/- 1000V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
3/27/2014	- Added "Logic Level Gate Drive" bullet in the features section on page 1 - Updated part marking on page 6. - Updated data sheet with new IR corporate template
9/30/2015	- Updated datasheet with corporate template - Corrected ordering table on page 1.

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