



[www.infineon.com/tricore](http://www.infineon.com/tricore)

**TriCore™**  
UNIFIED PROCESSOR



Never stop thinking.

# Introduction

TriCore is the first single-core 32-bit MCU-DSP architecture optimized for real-time embedded systems. Developed by a team with over 300 collective years of processor experience, TriCore is an innovative, award winning architectural solution which truly unifies the best of three worlds - real-time capabilities of microcontrollers, computational prowess of DSPs, and the highest performance/price implementations of RISC load-store architectures. The TriCore architecture is implemented as a family of cores that offer tremendous scalability in terms of both price and performance. In fact, the native MCU-DSP capabilities of the architecture allow system designers to tune (in software), the MCU and DSP performance of each TriCore core. For instance, a 100 MHz TriCore-1 core with a sustained 130 MIPs rating, can deliver 80 MCU MIPs + 50 DSP MIPs, or 40 MCU MIPs + 90 DSP MIPs, depending on how the system designer implements load-sharing in software.

## Features & Benefits

### MCU Features

- › Fast context switch & low interrupt latency
- › 16-bit and 32-bit instruction formats
- › Powerful bit manipulation support

### Tricore Benefits

- › Integrated MCU-DSP instructions in one core
- › Fast and efficient processing of multiple tasks on one engine
- › Low code size and inherent high level language support
- › One development toolset for both MCU and DSP tasks
- › Higher flexibility and lower cost

### DSP Features

- › Sustained throughput of two 16x16 MACs per clock
- › SIMD packed arithmetic and zero overhead loops
- › DSP addressing modes and saturated math

### Processor Features

- › 32-bit load-store Harvard architecture
- › Superscalar execution
- › 16 address and 16 data registers

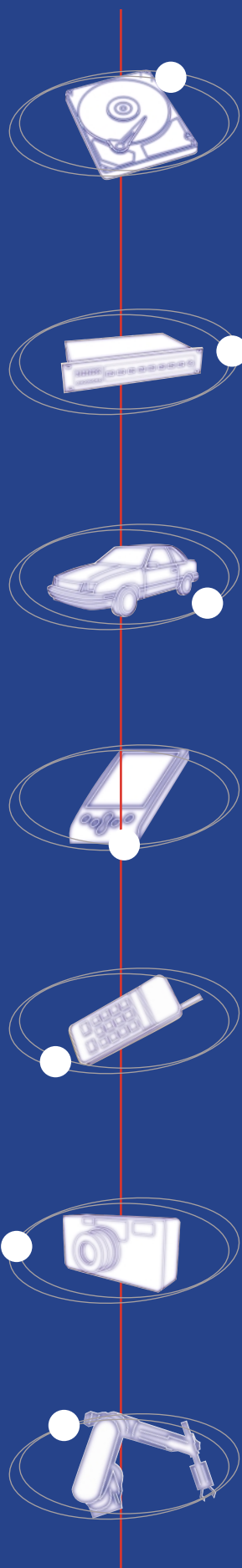
## Target Applications

TriCore has been optimized to meet the requirements of embedded applications such as computer peripherals, automotive & industrial, and communications. An increasing number of embedded designs employ both a microcontroller or microprocessor and a DSP or hard-wired ASIC. A TriCore based device can replace both these components due to its inherent MCU-DSP capabilities and its ability to switch between those tasks efficiently and quickly.

## TriCore System Architecture

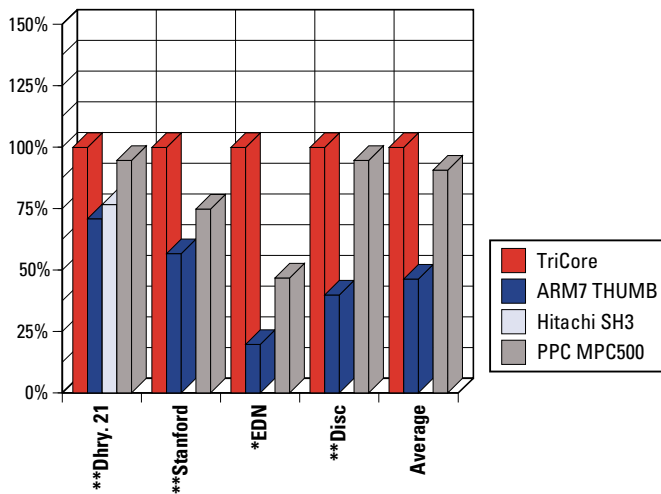
TriCore's modular system architecture facilitates the design of true system-on-chip solutions by enabling easy integration of a TriCore processor core with on-chip high-density memories, application specific peripherals and customer-specific logic. The figure below illustrates a typical TriCore based application specific device.

The backbone of the TriCore system architecture is the Flexible Peripheral Interconnect (FPI) bus. FPI is a core-independent demultiplexed bus with up to 32 address bits and 64 data bits, and a peak throughput of 800 Mbytes/sec at 100 MHz. In order to eliminate the memory bottleneck commonly found in RISC architectures, the TriCore system architecture is designed to efficiently utilize various types and sizes of on-chip memories (DRAM, SRAM, ROM, OTP and Flash). Another important facet of this system architecture is the on-chip debug mechanism for easy hardware-software integration. The components that make up this mechanism are: breakpoint support in the core, debug port that offers access to the breakpoints and other system resources, real-time trace port.



# Benchmarks

## RISC Performance

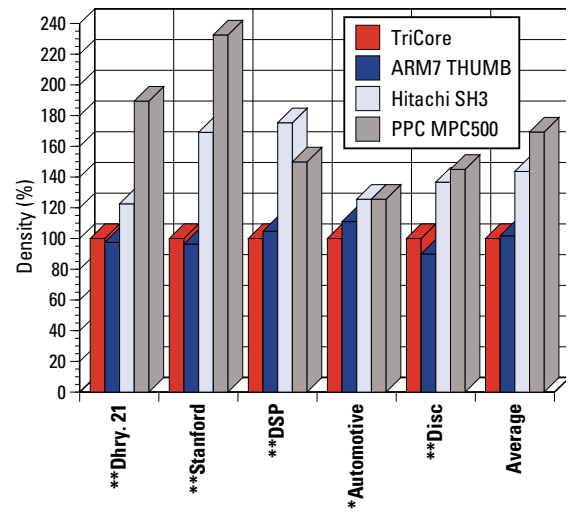


\*Based on TriCore Green Hills development tools 1.8.9

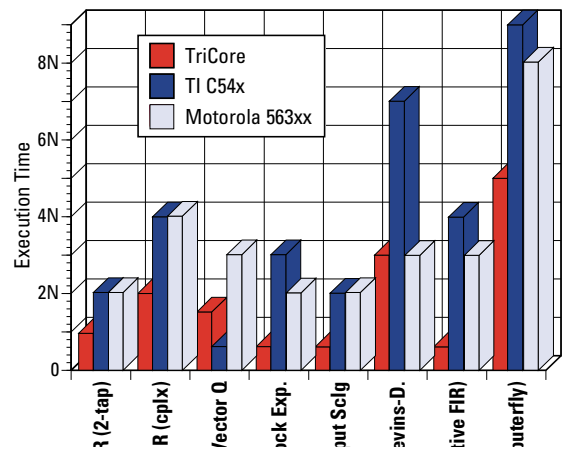
\*\*Based on TriCoreTasking development tools 0.9r9

Dhrystone results for Hitachi SH3 and PPC according published results, other obtained using available simulators.

## Code Size (lower is better)



## DSP Performance (lower is better)



# TriCore Development Tools

The TriCore architecture is well supported by a robust and comprehensive suite of development tools and services such as compiler-assembler tool chains, real-time operating systems, emulators, simulators, evaluation boards, training and consulting. Infineon developed the TriCore instruction set architecture and system architecture in close consultation with the third party providers of these tools. This enabled the fine tuning of TriCore to fully exploit the advanced capabilities of these development tools while giving developers a well-tuned, easy-to-use environment in which to unleash the power of the architecture. Additionally, Infineon has created a unique partnership program called the SPACE Program. For more information about our SPACE Program please go to [www.spacetools.com](http://www.spacetools.com).

# TriCore Third Party Partners

Applications, Boards, Software, Modeling Tools, Training, Consulting



Operating Systems



Software Generation and Debug Tools

[www.infineon.com/tricore](http://www.infineon.com/tricore)

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