TriCore™ AudoMax Derivatives TC1724, TC1728, TC1782, TC1784, TC1791, TC1793, TC1798

Electromagnetic Emission Summary

AP32193

Test Report

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1 Introduction

This application note describes the electromagnetic emission (EME) behaviour of all Infineon's AudoMax microcontrollers. Table 1 lists their main EME-relevant design and functional features.

- All microcontrollers are fabricated in a 90 nm CMOS process.
- The lead-frame packages (QFP) offer a centered "e-pad" which must be soldered to the PCB's ground plane. The ball-grid array packages (BGA) offer centered VSS balls which should also be soldered to PCB ground. This centered ground connection additionally serves as heat dissipation. E-pad and center ground balls help to keep noise current return paths short, thus reducing emission radiation.
- The system clock is the operating frequency of the TriCore CPU. Peripherals typically operate at lower clock rates while the PLL itself generates a higher frequency. Operating a microcontroller at lower clock rates reduces emission slightly. Because of the unchanged steepness of the clock edges, the general emission behaviour stays nearly the same.
- Some AudoMax devices support frequency modulation of the PLL clock. Note that the special operation mode of the AudoMax-FMPLL is an enhanced triangular modulation which reduces the accumulated jitter (or time interval error TIE) significantly, allowing reliable asynchronous serial data communication. For details please refer to the Infineon microcontroller application note AP32185 [1]. Frequency modulation of the system clock reduces emission significantly because the RF peak energy is then distributed along side bands. On Infineon microcontrollers, the modulation amplitude is not limited by TIE constraints.
- All AudoMax devices provide pad driver scaling. The DC driver strength and slew rates can be selected among two, four, or seven settings, depending on the respective I/O pin's driver class. For details please refer to the Infineon microcontroller application note AP32146 [2]. Driver scaling reduces emission significantly along with slower switching times. Therefore, scaling is limited according to target data rates and signal integrity.
- An embedded linear voltage regulator is implemented on two AudoMax microcontrollers. It helps to keep switching noise inside the microcontroller.

Product	Package	E-pad	System clock	Clock modulation	Scalable pads	Embedded voltage reg.
TC1724	QFP-144	soldered to GND	133 MHz	n/a	7 stages	VDD, VDDP
TC1728	QFP-176	soldered to GND	133 MHz	n/a	7 stages	VDD, VDDP
TC1782	QFP-176	soldered to GND	180 MHz	n/a	7 stages	no
TC1784	BGA-292	n/a	180 MHz	n/a	7 stages	no
TC1791	BGA-292	n/a	240 MHz	2.5 %	7 stages	no
TC1793	BGA-416	n/a	270 MHz	3.0 %	7 stages	no
TC1798	BGA-516	n/a	300 MHz	0.8 %	7 stages	no

Table 1 Main feature overview of the microcontrollers under test

For architectural details, please refer to the respective product specifications which can be downloaded from www.infineon.com.

2 Executive summary

2.1 Selected nets for emission comparison

The rating of microcontroller emission behaviour given in this document is based on much more comprehensive measurements. Those are documented in the product-specific emission test reports which are available on request. To be able to compare the emission characteristics of all AudoMax microcontrollers, the measurement results provided in chapters 6 and 7 systematically show the emission spectra of:

- conducted emission of core supply domain (VDD 1.3 V),
- conducted emission of I/O supply domain (VDDP 3.3V),
- minimum conducted crosstalk emission found on any tested pin ("quiet pin"),
- maximum conducted crosstalk emission found on any tested pin ("noisy pin"),
- radiated emission of the whole microcontroller facing into a mini-TEM cell.

2.2 Test procedure compliance

All EMI test results presented in this report are obtained from hardware and software test setups compliant to the "Generic IC EMC Test Specification" ("BISS paper") [7], open copyright by Robert Bosch GmbH, Infineon Technologies AG, Continental AG (former Siemens-VDO).

2.3 General emission result

Conducted and radiated emissions of the AudoMax 32-bit microcontrollers stay mostly below the BISS limits for application-typical operation modes and configurations, which are:

- All function units are active.
- Reduced pad drivers are used.
- FMPLL (clock modulation) is activated.
- Series resistor is used in oscillator circuit between XTAL2 pin and crystal.

2.4 Conducted emission result

BISS limits for conducted emission may be violated for the following cases:

- **TC1724** on supply net VDD (4^{th} harmonic 533 MHz: +4 dBµV). Thanks to the EVR, VDD is a local net which is not considered to be critical.
- **TC1728** on supply net VDD (5^{th} harmonic 666 MHz: +6 dBµV). Thanks to the EVR, VDD is a local net which is not considered to be critical.
- **TC1782** on e.g. P2.0 (base frequency 180 MHz and 2^{nd} harmonic 360 MHz: +2 dBµV). External filters should be considered for port pins close to the CPU which leave the application board.
- **TC1784** on supply net VDD (2^{nd}, 3^{rd}, 4^{th} harmonic 360-720 MHz: +5..10 dBµV). The power supply should be routed carefully; at least four PCB layers are recommended.
- **TC1791** on supply net VDD (system clock divided by 3 = 80 MHz: +3 dBµV).
- **TC1791** on port pins next to oscillator due to strong oscillator clock crosstalk (oscillator base frequency: +9 dBµV). Use series resistor (e.g. 1 kΩ) between XTAL2 pin and crystal. Reduce oscillator gain to level 2 if signals are rated critical.
- **TC1793** worst-case I/O emission might exceed the BISS limit at very low frequencies. External filters may be considered for port pins which leave the application board.
- **TC1798** on supply net VDD (system clock divided by 3 = 100 MHz: +3 dBµV).
- **TC1798** on port pins next to oscillator due to strong oscillator clock crosstalk (oscillator base frequency: +6 dBµV). Use series resistor (e.g. 1 kΩ) between XTAL2 pin and crystal. Reduce oscillator gain to level 2 if signals are rated critical.

2.5 Radiated emission result

BISS limits for radiated emission may be violated for the following cases:

- **TC1724** 7th system clock harmonic (933 MHz): +9 dBµV. Note: this emission peak is amplified by unintended GSM interference. Mere microcontroller emission is less and should stay below the BISS limit.
- **TC1728** 7th system clock harmonic (933 MHz): +3 dBµV. Note: this emission peak is amplified by unintended GSM interference. Mere microcontroller emission is less and should stay below the BISS limit.
- **TC1782** between 500 and 650 MHz: +2 dBµV.
- All other microcontrollers, i.e. those mounted in a ball-grid array package, show no radiated emission violations of the limit curve.

2.6 PCB design recommendations

Special care on PCB layout is advisable to prevent supply and I/O noise from being coupled to any antenna structures on the PCB. General PCB design guidelines are described in detail in the application note AP24026 [3]. Microcontroller-specific PCB design guidelines are described in detail in the related application notes [4]-[9].

- Use common GND plane.
- Design power islands below or around microcontroller in close vicinity.
- Reach lowest possible power/ground impedance by avoiding plane/island cheesing by vias.
- Solder the exposed die pad (e-pad) to the GND plane; see also chapter 8.1.
- Place decoupling capacitors close to supply pins in a way that current return paths are kept low, and the noise current is forced to flow through the capacitors.
- Keep signal traces short.
- Route “high-speed” signal traces as micro-strip or stripline (i.e. use ground shielding).
- Avoid signal trace vias through power or ground planes.

2.7 Microcontroller configuration recommendations

Several microcontroller configurations provide significant emission reduction:

- Use lowest permissable data rates.
- Use weakest permissable pad driver settings; details are provided in chapter 8.2.
- Activate the system clock modulation (FMPLL); details are provided in chapter 8.3.

For further recommendations please refer to Infineon’s application notes [1] and [2].

3 Emission measurement methods

3.1 Conducted emission measurement

The setup used for electromagnetic emission measurement complies fully with the BISS test specification which can be downloaded from the internet [10]. One test board was designed for every microcontroller under test with similar layout. The test board is used for conducted and radiated emission measurements.

Conducted emission is measured using the standardized 150 Ω network. This network is used for both port and power supply emission measurements. Only crosstalk noise is measured; i.e. the port pins under test are never actively switching. Frequency range is 150 kHz to 1 GHz.

Fig. 1 shows the schematic 150 Ω network connection to the microcontroller (IC under test) and the general layout of each 150 Ω probing net.

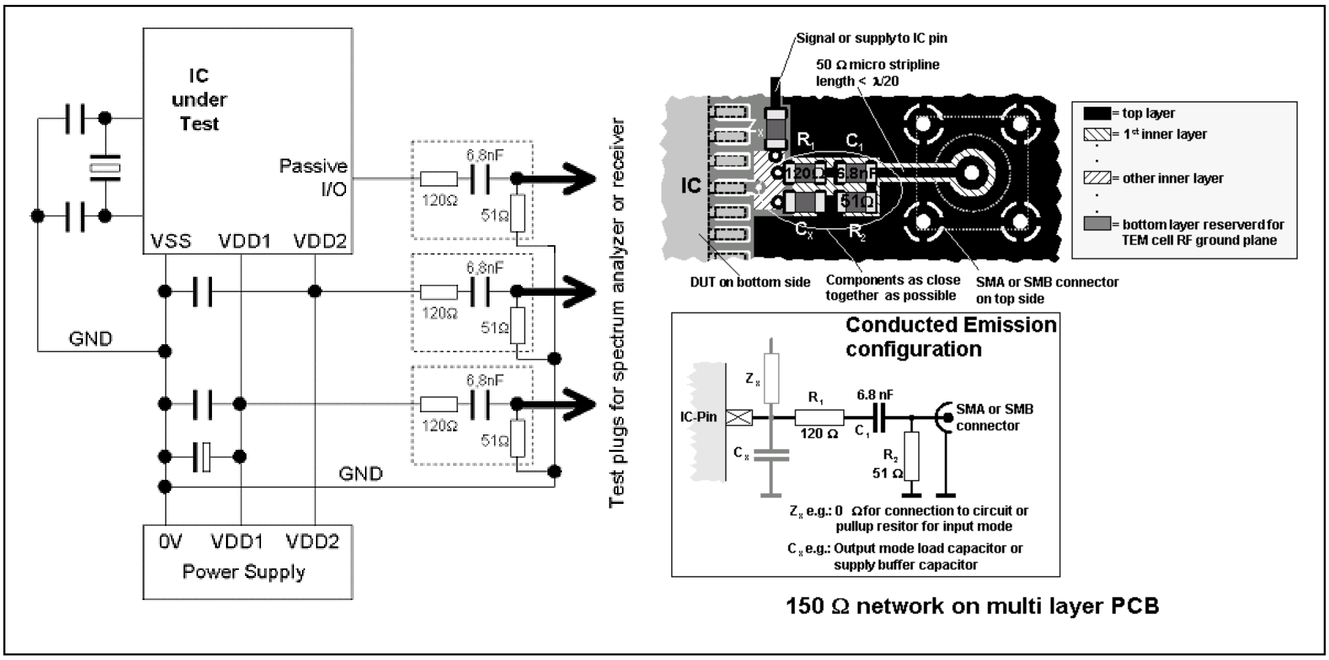

Figure 1 150 Ω probing networks for conducted emission measurement

150 Ω networks are provided for conducted emission measurements according to the international standard IEC 61967 part 4 and the BISS test specification for a set of signals and power supply nets. The electromagnetic emission comparison of various microcontrollers in this document is based on probing the main digital power supply nets plus a “best case” and a “worst case” I/O pin. In fact, many more pins have been measured and documented in the detailed product-specific EMC test reports which are available from Infineon on request.

3.2 Radiated emission measurement

Radiated emission is measured using the standard mini TEM cell according to the international standard IEC 61967 part 2 and BISS emission test specification. The frequency range is from 150 kHz to 1 GHz.

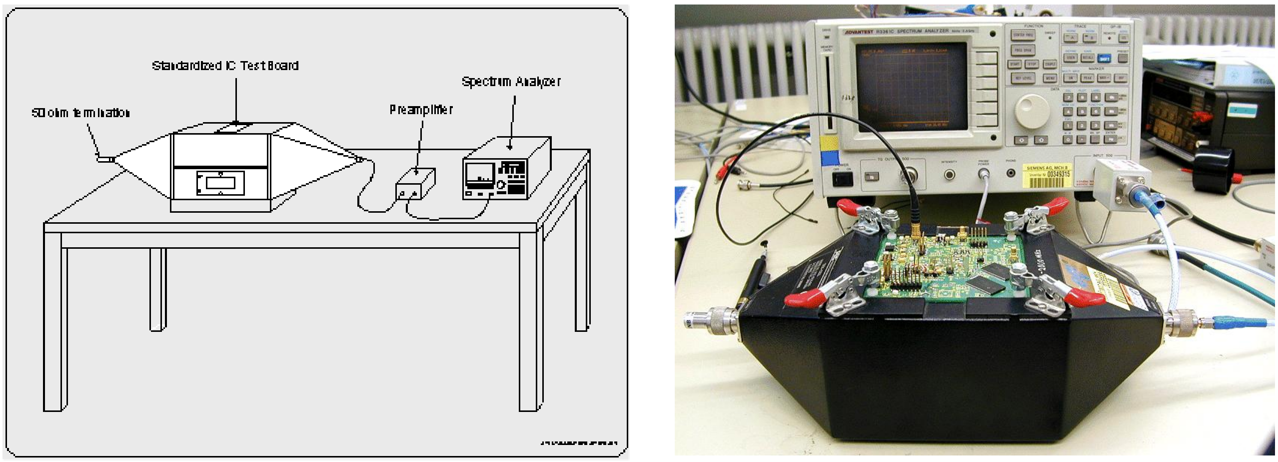

Figure 2 Measurement setup for radiated emission

3.3 Measurement conditions and instruments

Measurement were performed under well-defined and unchanged conditions to provide a reliable repeatability:

Spectrum analyzer: Rohde & Schwarz FSP7

Detector type: Peak detector

Measurement time: For all measurements, the emission measurement time (10ms) at one frequency is longer than the test software loop duration.

Pre-Amplifier: internal

Data generation software: Rohde & Schwarz EMIPAK 9950

Environment: Temperature 23°C ± 5°C

Supply: Nominal voltage ± 5%

For all measurements the noise floor is at least 6dB below the limit.

<table>
<tr><th colspan="5" rowspan="2">Frequency range</th><th colspan="2">Spectrum Analyzer</th></tr>
<tr><th>RBW</th><th>Sweep time*</th></tr>
<tr><td rowspan="3">150 Ω</td><td rowspan="3">TEM</td><td>150 kHz</td><td>to</td><td>30 MHz</td><td rowspan="3">10kHz</td><td rowspan="3">$t_s = \frac{NP \cdot LT \cdot FR}{RBW}$</td></tr>
<tr><td>30 MHz</td><td>to</td><td>200 MHz</td></tr>
<tr><td>200 MHz</td><td>to</td><td>1000 MHz</td></tr>
</table>

Table 2 Spectrum analyzer setting

*) NP = number of points; LT = loop time; FR = frequency range

4 Emission limit curves

For reference purpose, a respective limit curve is shown in all measured emission spectra. These curves are taken from the BISS specification [10]. Figures 3 and 4 introduce these 3 limit curves:

- Conducted emission 150 Ω, limit for supply pin emission (i.e. VDDx domains),
- Conducted emission 150 Ω, limit for port pin emission (i.e. I/O pins),
- Radiated emission, limit for mini-TEM cell emission (not domain or pin specific).

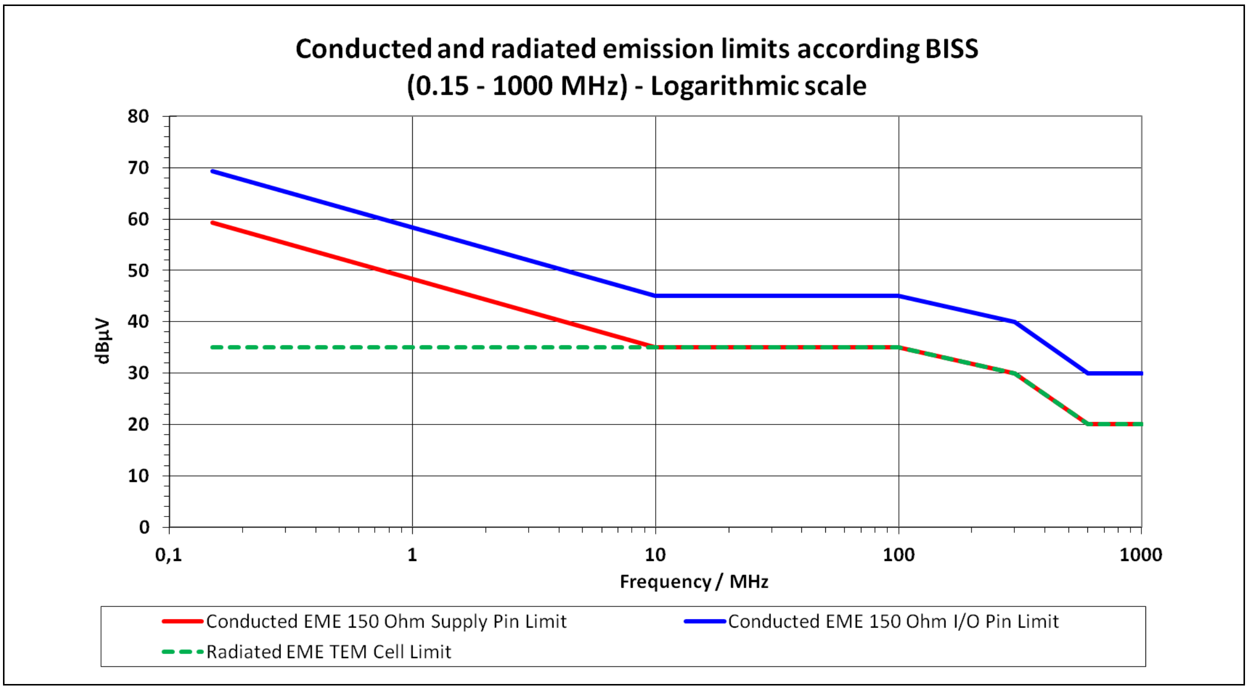

Figure 3 BISS limit curves in logarithmic scale

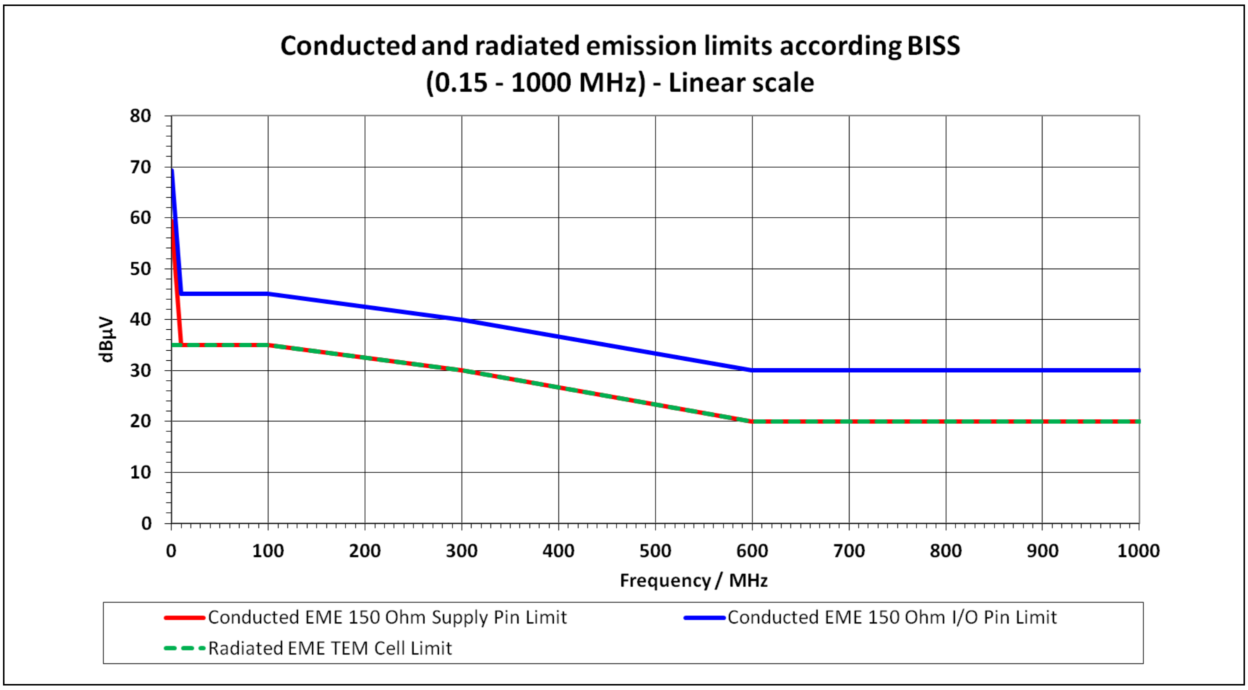

Figure 4 BISS limit curves in linear scale

As long as the measured emission stays below the respective limit, the measured supply or signal net is treated as “clean”. If the measured emission violates the respective limit for one or more frequencies, some more care must be taken for an EMC-friendly PCB layout. Infineon strongly recommends to use all microcontroller hardware and software settings as explained in chapter 8. They will provide a significant reduction of electromagnetic emission. Keep in mind that the usage of reduced pad drivers may be limited with respect to the required system performance and signal integrity:

- Reduce system clock frequency.
- Disable unused clocks (e.g. CLKOUT, EXTCLK [automatically disabled after reset]).
- Use frequency-modulated system clock (only available on TC1791, TC1793, TC1798) [1].
- Reduce output pad driver strength (two, four or seven settings available for all port pins) [2].
- Consider Infineon’s general and product-specific PCB design guidelines which propose optimized power supply layout and decoupling concepts [3]-[9].

5 Microcontroller operation during test

To get a realistic impression of the microcontroller's emission potential, an "application-typical" operating mode was configured during the tests. This means:

- Program is executed from on-chip flash memory
- CPU and all functional modules are active
- System clock output is disabled
- High-speed interfaces are active (e.g. FlexRay @ 10 Mbit/s, SPI @ 5 MBit/s, ASC / LIN / CAN @ 500 kBit/s)
- Other I/Os run at lower data rates
- EBU is active (available on TC1798 only)
- All output pad driver strengths are selected matching their data rates, driving 22 pF load. Table 3 shows the ratio of driver settings (all digital outputs without ADC channels) as it was used for the emission tests:

	TC1724		TC1728		TC1782		TC1784		TC1791		TC1793		TC1798	
Driver strength	abs.	%	abs.	%	abs.	%	abs.	%	abs.	%	abs.	%	abs.	%
Weak & Pulldown	0	*0*	0	*0*	14	*16*	0	*0*	0	*0*	0	*0*	0	*0*
Medium	20	*23*	30	*27*	48	*56*	40	*29*	24	*19*	59	*27*	58	*25*
Strong-soft	67	*77*	77	*69*	24	*28*	95	*68*	96	*75*	153	*69*	163	*71*
LVDS	0	*0*	4	*4*	0	*0*	4	*3*	8	*6*	8	*4*	8	*4*
Total	**87**	***100***	**111**	***100***	**86**	***100***	**139**	***100***	**128**	***100***	**220**	***100***	**229**	***100***

Table 3 Pad driver scaling of the microcontrollers under test

- Core supply voltage VDD = 1.30 V
- I/O supply voltage VDDP = 3.30 V
- The system clock is 133/180/240/270/300 MHz according to Table 1.
- The crystal frequency is 20 MHz in all cases.
- Devices from center fabrication lot were used, operating at nominal voltages and at room temperature.
- Emissions are slightly, but negligibly increasing with higher supply voltages and lower ambient temperature.
- The fabrication lot influence is negligible.

6 Conducted emission measurement results

6.1 Microcontroller TC1724

6.1.1 TC1724: Probed nets

Fig. 5 shows the location of the four nets selected for emission measurement:

- VDD 1.3V (embedded voltage regulator output)
- VDDP 3.3V (embedded voltage regulator output)
- P0.4 (min. noise level)
- P2.0 (max. noise level)

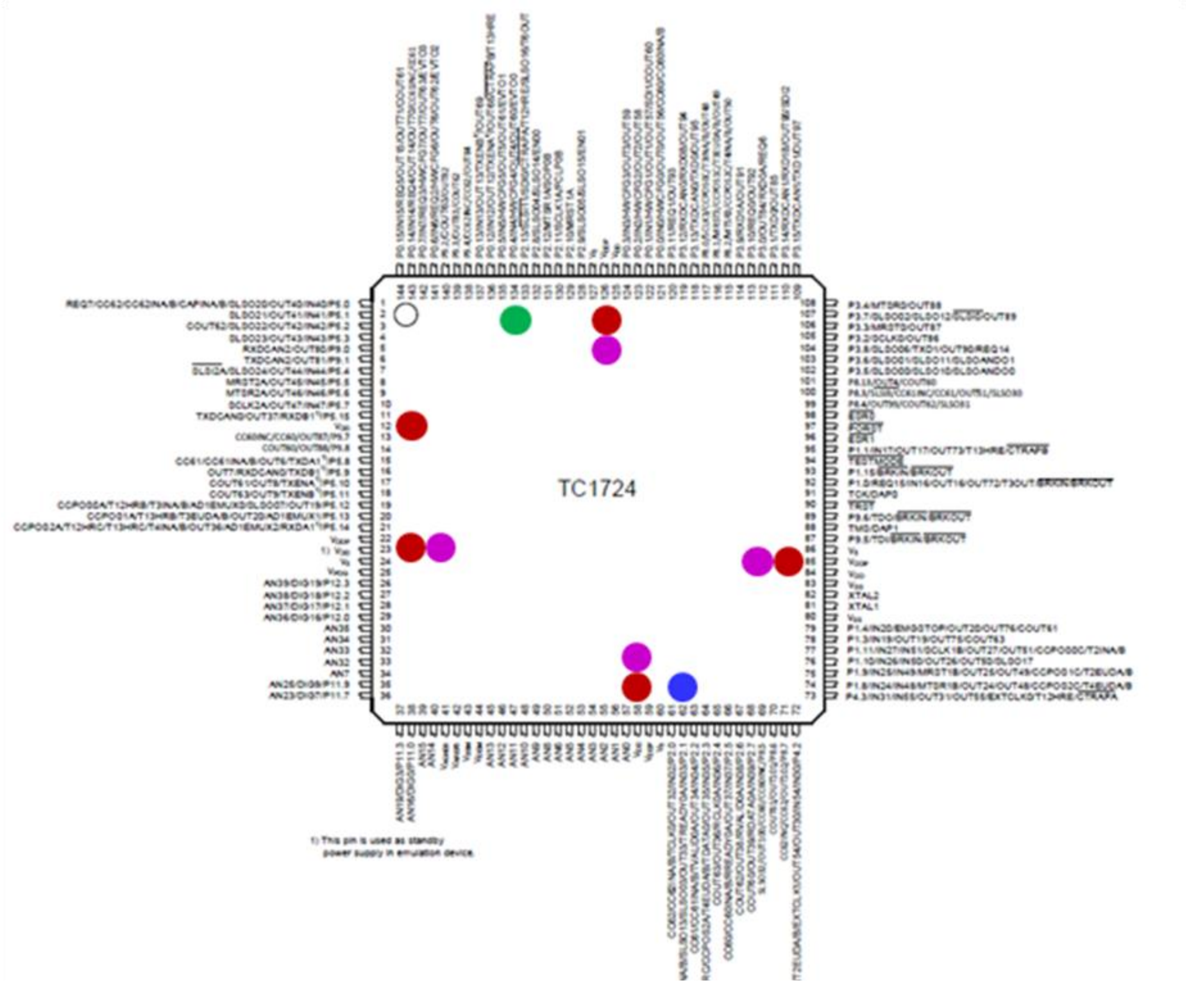

Figure 5 TC1724 probed nets for electromagnetic emission

6.1.2 TC1724: Result summary

The TC1724 fulfills the BISS emission limits on all nets except VDD (4th harmonic: +4 dBµV).

Because of the EVR, VDD is an internal node without external connection to system voltage regulator, ECU connector or cable. Therefore, the VDD net can be layouted locally, isolating its noise. Take care for short current return paths through decoupling capacitors.

6.1.3 TC1724: Conducted emission results

Fig. 6-9 show the emission measurement results at the four probed nets.

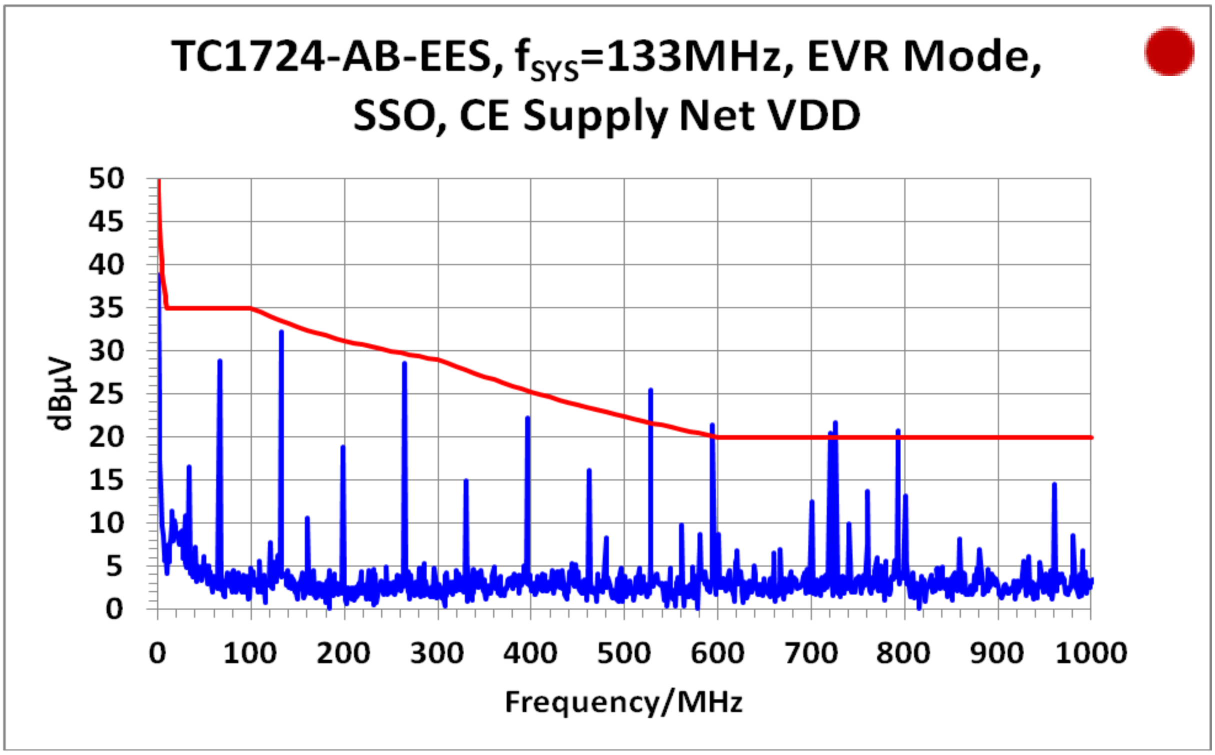

Figure 6 TC1724; Application pattern; 133 MHz; VDD conducted

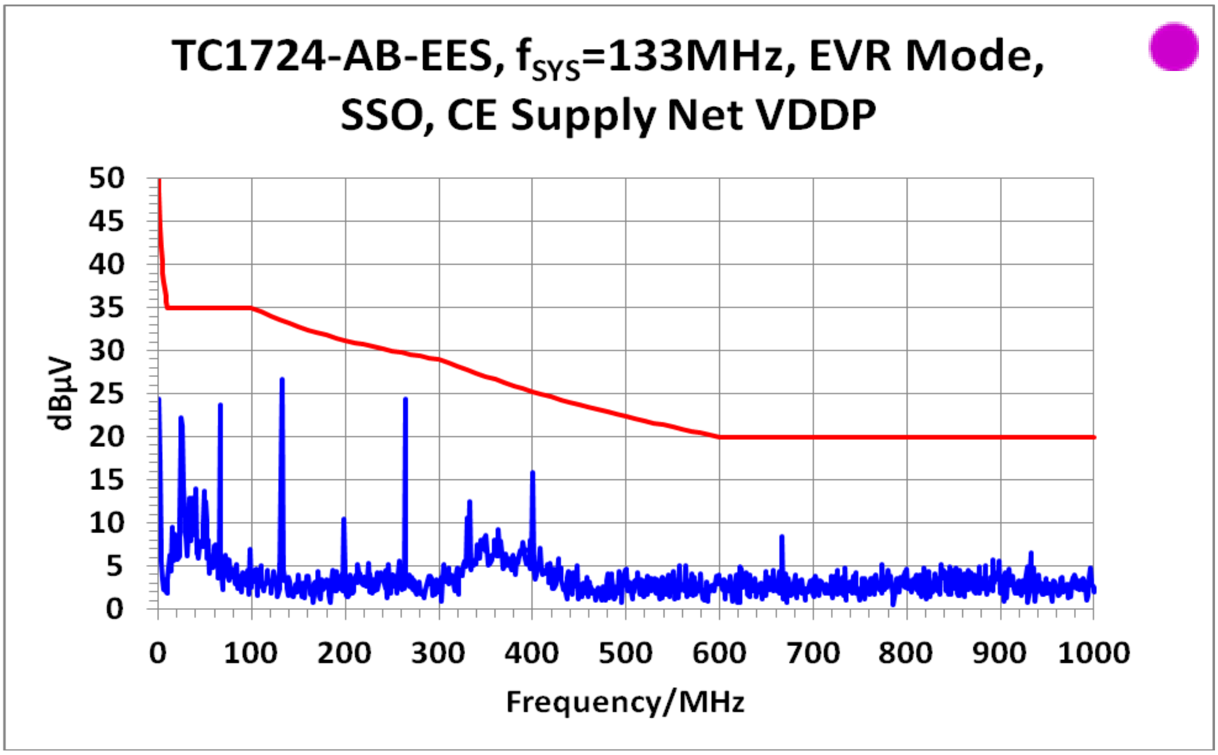

Figure 7 TC1724; Application pattern; 133 MHz; VDDP conducted

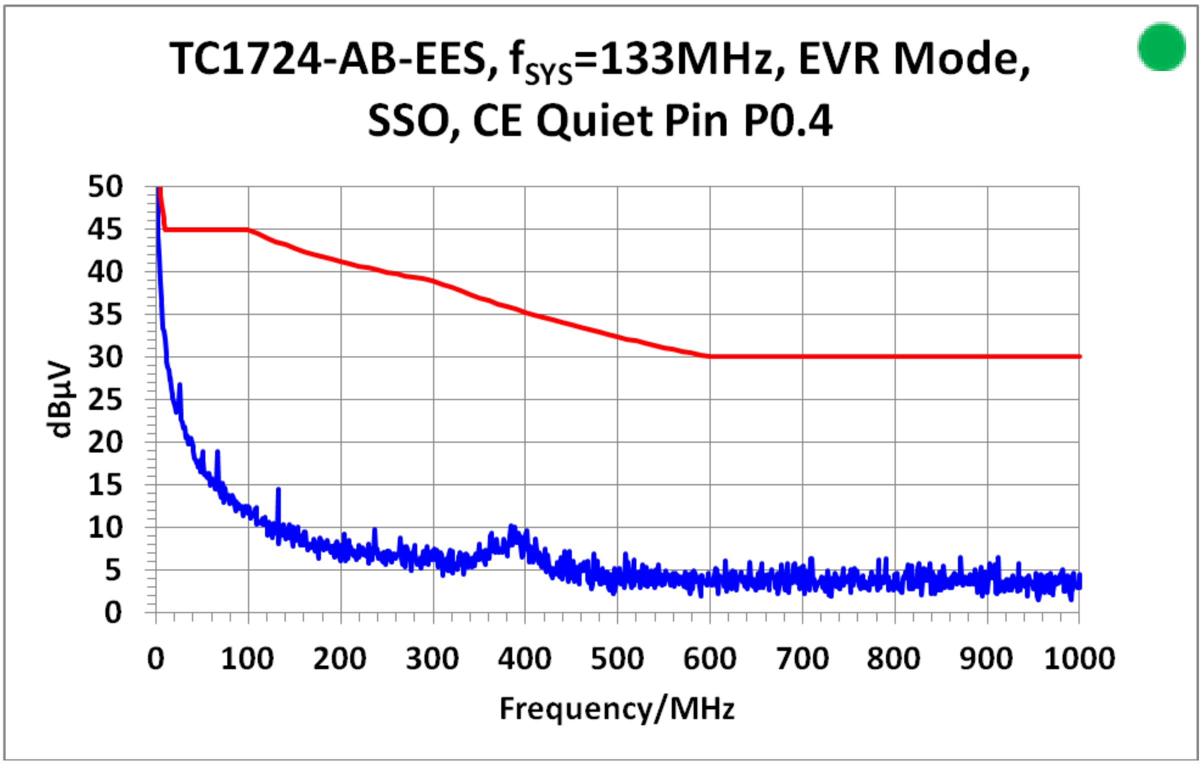

Figure 8 TC1724; Application pattern; 133 MHz; best-case I/O conducted

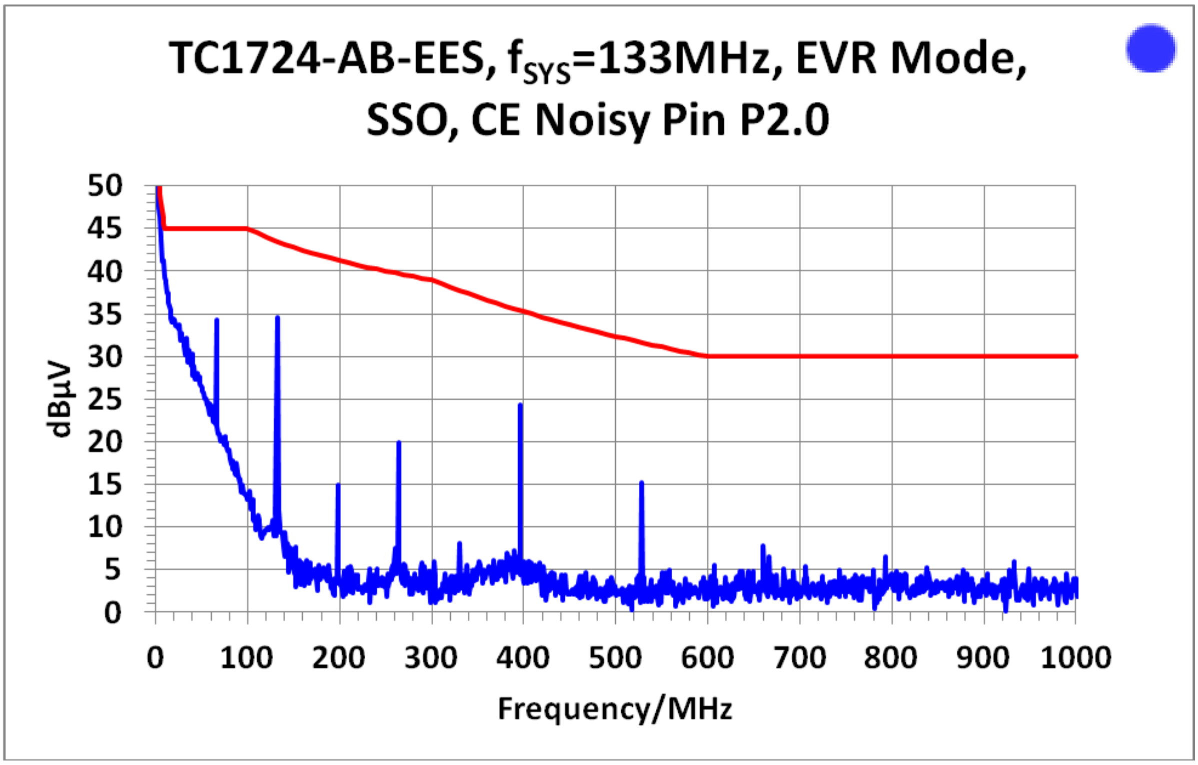

Figure 9 TC1724; Application pattern; 133 MHz; worst-case I/O conducted

6.2 Microcontroller TC1728

6.2.1 TC1728: Probed nets

Fig. 10 shows the location of the four nets selected for emission measurement:

- VDD 1.3V (embedded voltage regulator output)
- VDDP 3.3V (embedded voltage regulator output)
- P0.9 (min. noise level)
- P2.0 (max. noise level)

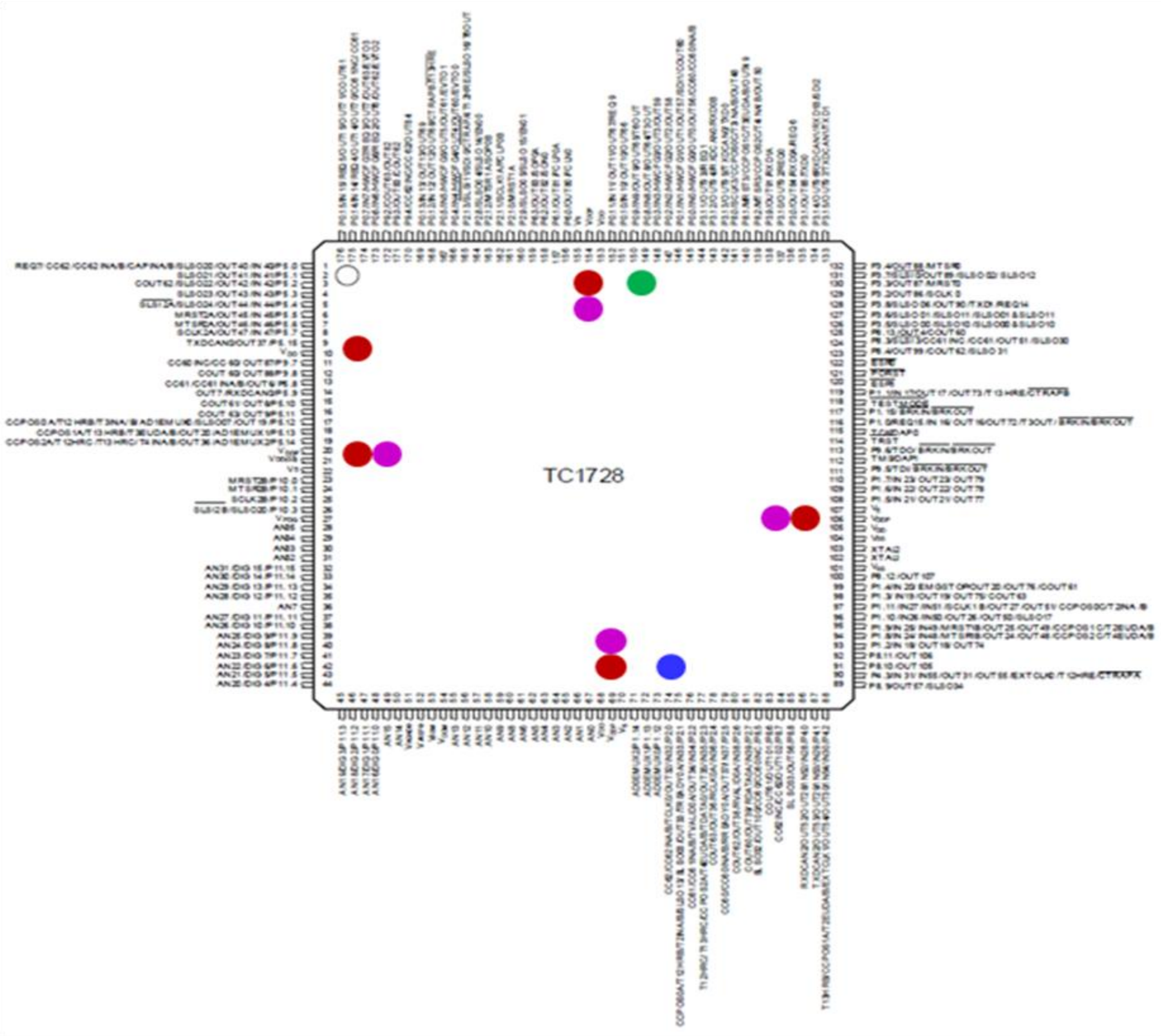

Figure 10 TC1728 probed nets for electromagnetic emission

6.2.2 TC1728: Result summary

The TC1728 fulfills the BISS emission limits on all nets except VDD (5^{th} harmonic: +6 dBµV).

Because of the EVR, VDD is an internal node without external connection to system voltage regulator, ECU connector or cable. Therefore, the VDD net can be layouted locally, isolating its noise. Take care for short current return paths through decoupling capacitors.

6.2.3 TC1728: Conducted emission results

Fig. 11-14 show the emission measurement results at the four probed nets.

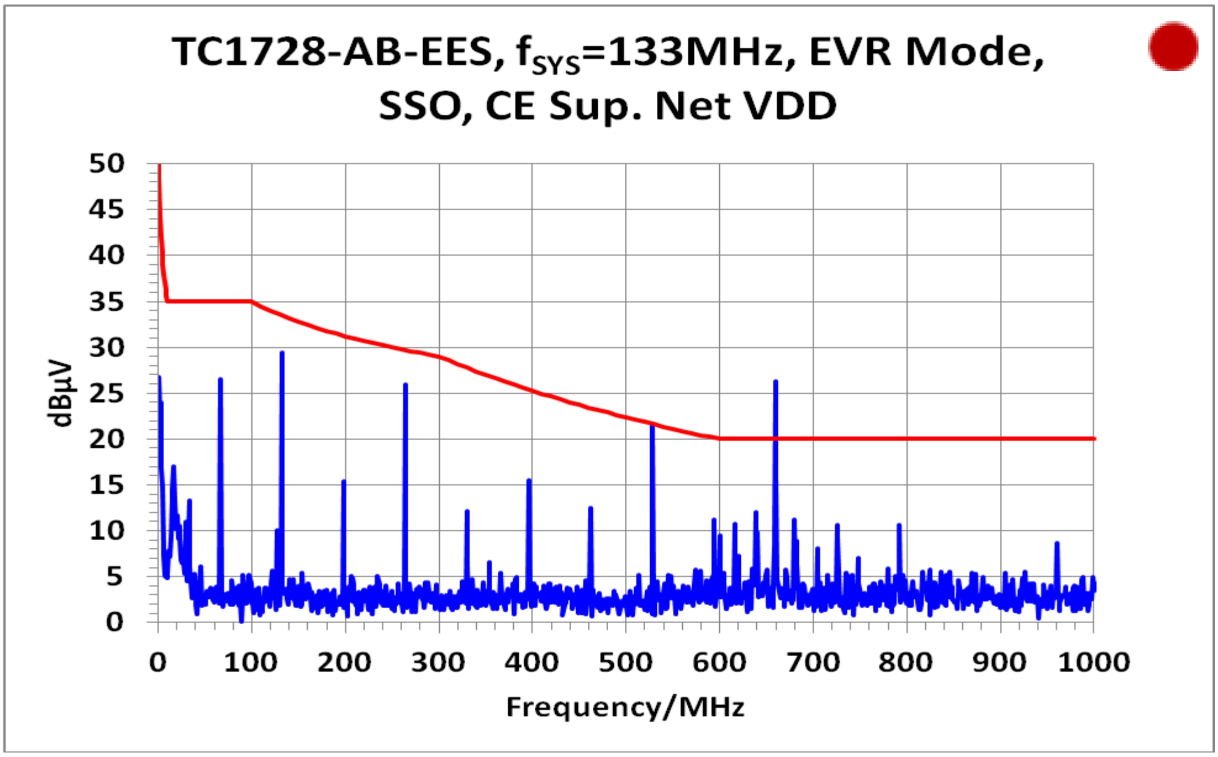

Figure 11 TC1728; Application pattern; 133 MHz; VDD conducted

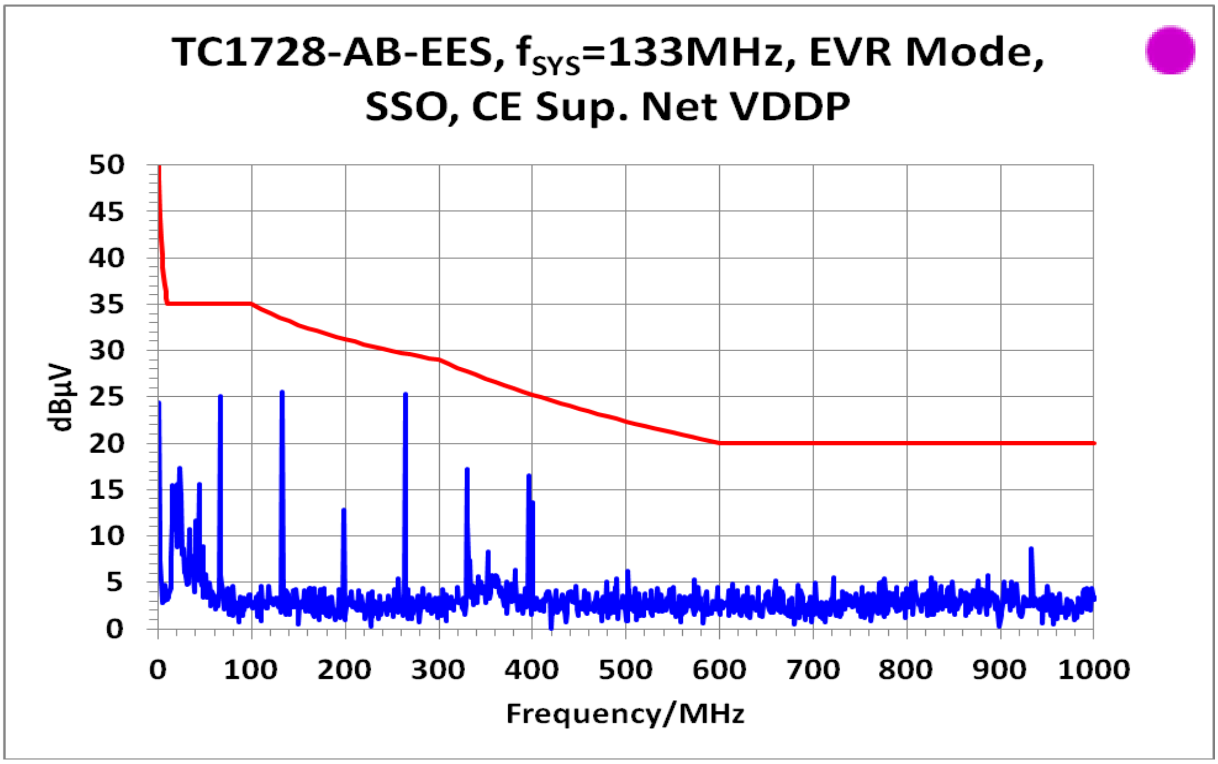

Figure 12 TC1728; Application pattern; 133 MHz; VDDP conducted

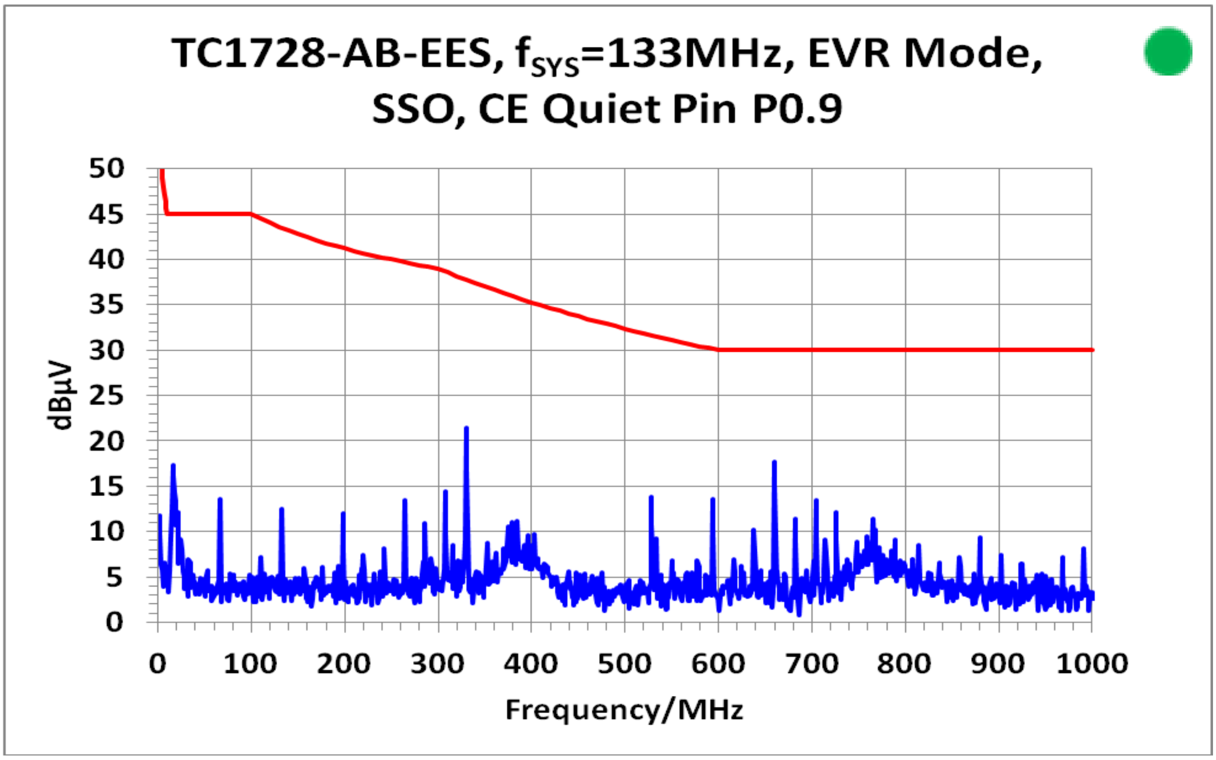

Figure 13 TC1728; Application pattern; 133 MHz; best-case I/O conducted

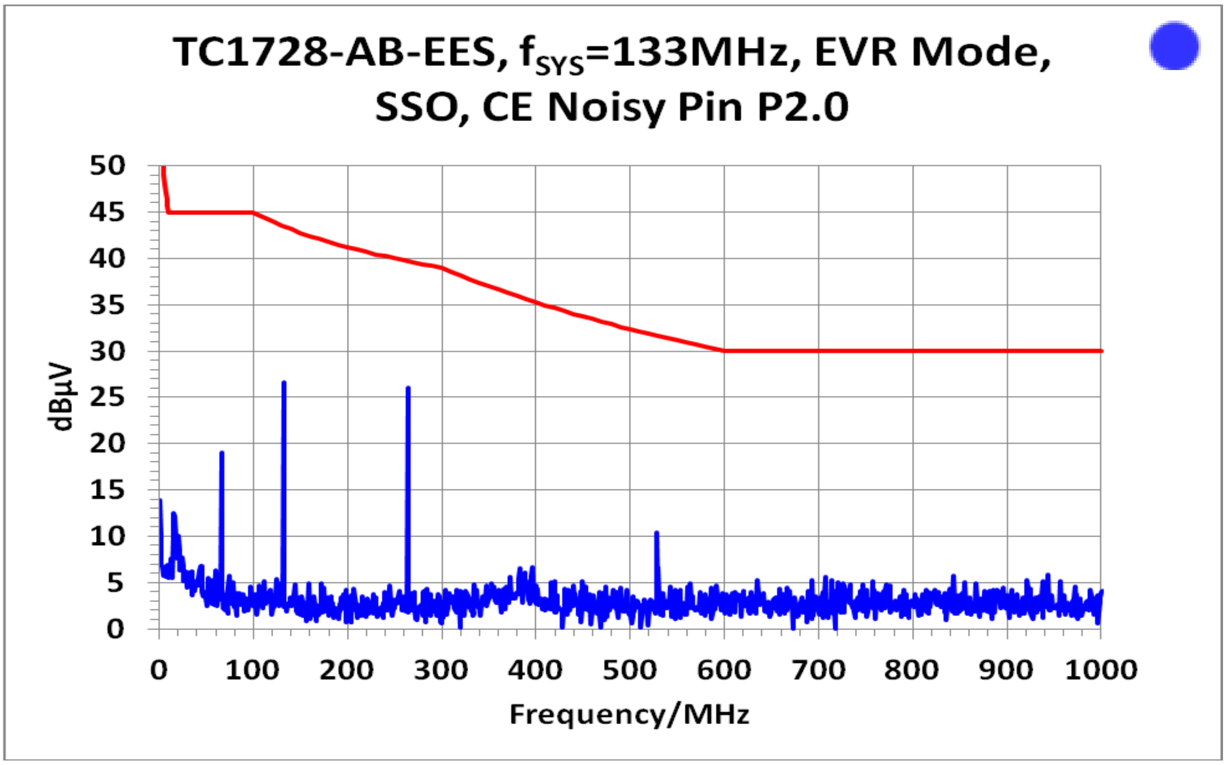

Figure 14 TC1728; Application pattern; 133 MHz; worst-case I/O conducted

6.3 Microcontroller TC1782

6.3.1 TC1782: Probed nets

Fig. 15 shows the location of the four nets selected for emission measurement:

- VDD 1.3V
- VDDP 3.3V
- P1.7 (min. noise level)
- P2.0 (max. noise level)

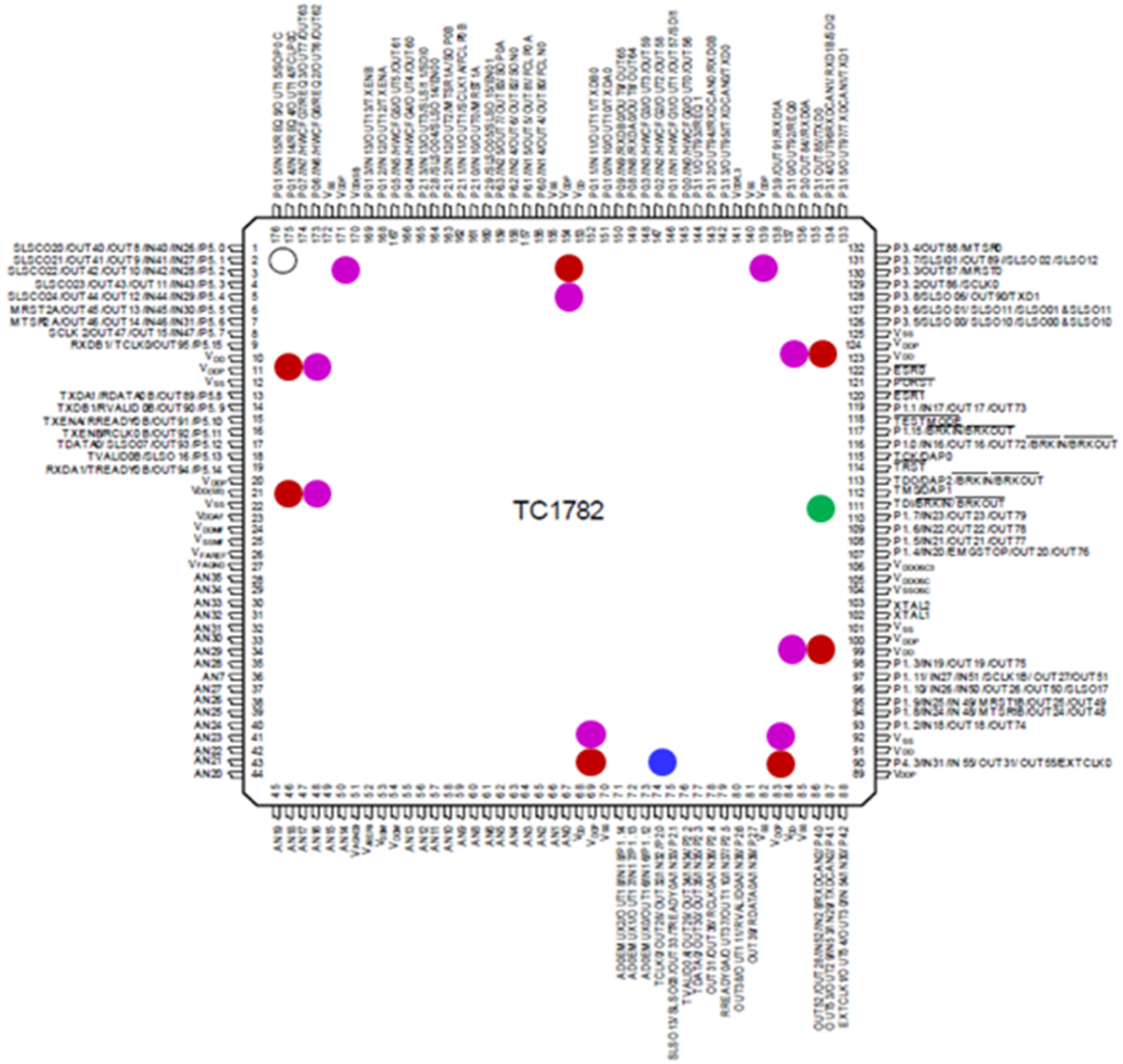

Figure 15 TC1782 probed nets for electromagnetic emission

6.3.2 TC1782: Result summary

The TC1728 fulfills the BISS emission limits on all nets except P2.0 (crosstalk on base frequency and 2nd harmonic: +2 dBµV).

External filters should be considered for port pins close to the CPU which leave the application board.

6.3.3 TC1782: Conducted emission results

Fig. 16-19 show the emission measurement results at the four probed nets.

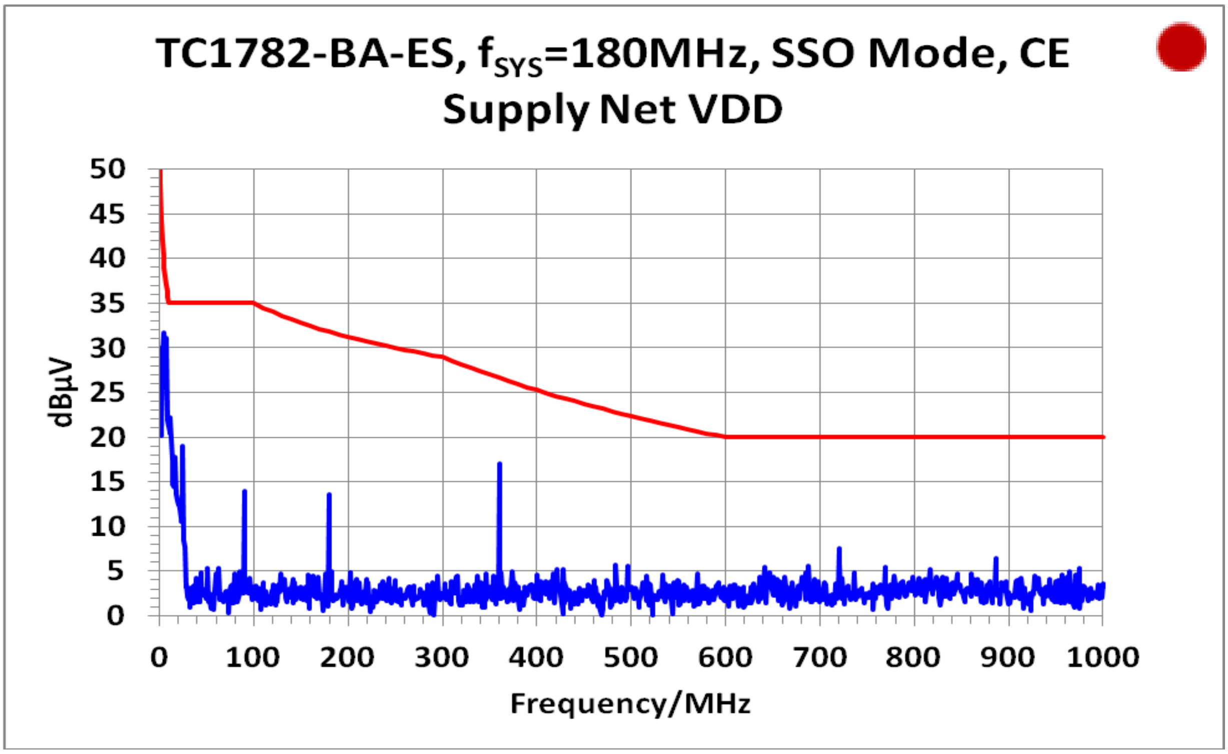

Figure 16 TC1782; Application pattern; 180 MHz; VDD conducted

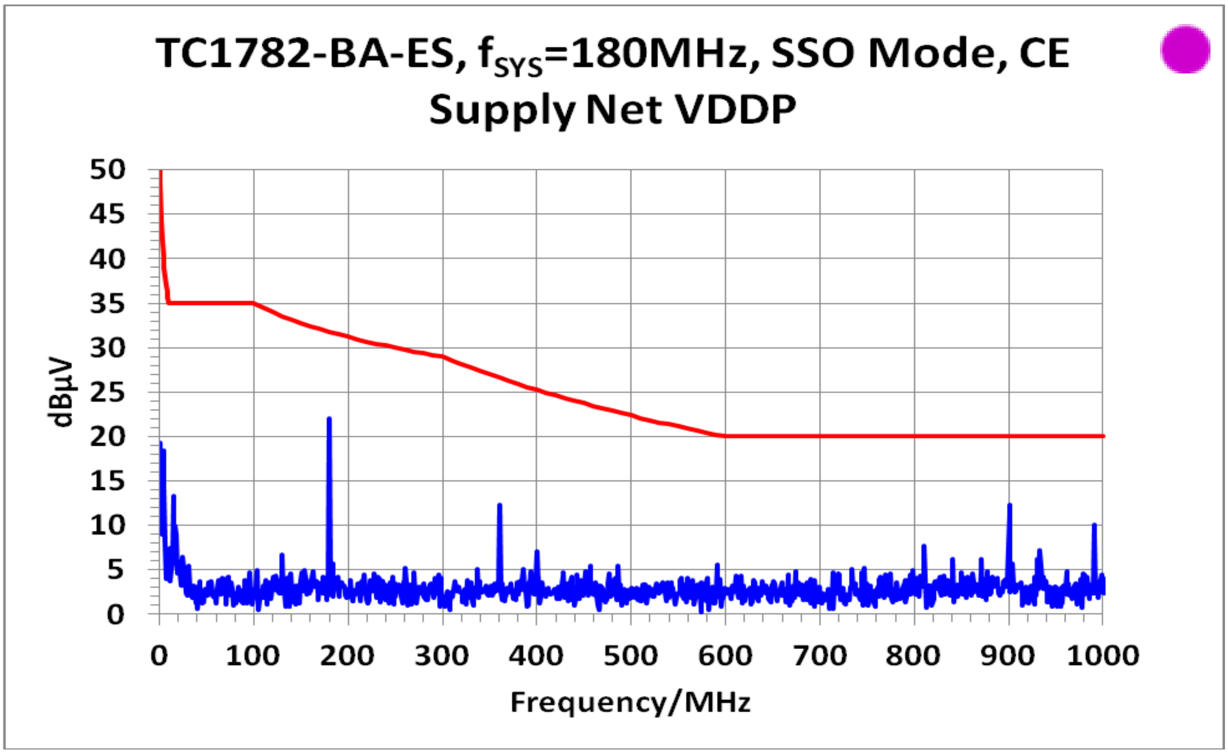

Figure 17 TC1782; Application pattern; 180 MHz; VDDP conducted

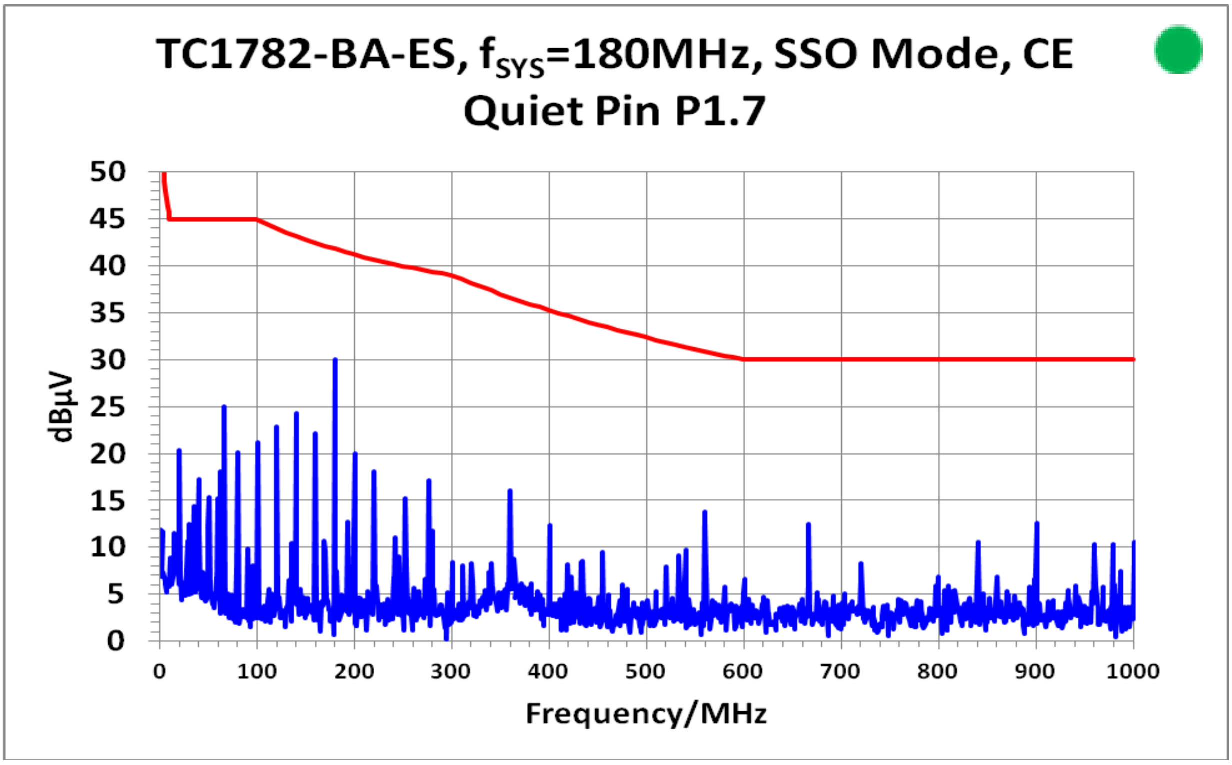

Figure 18 TC1782; Application pattern; 180 MHz; best-case I/O conducted

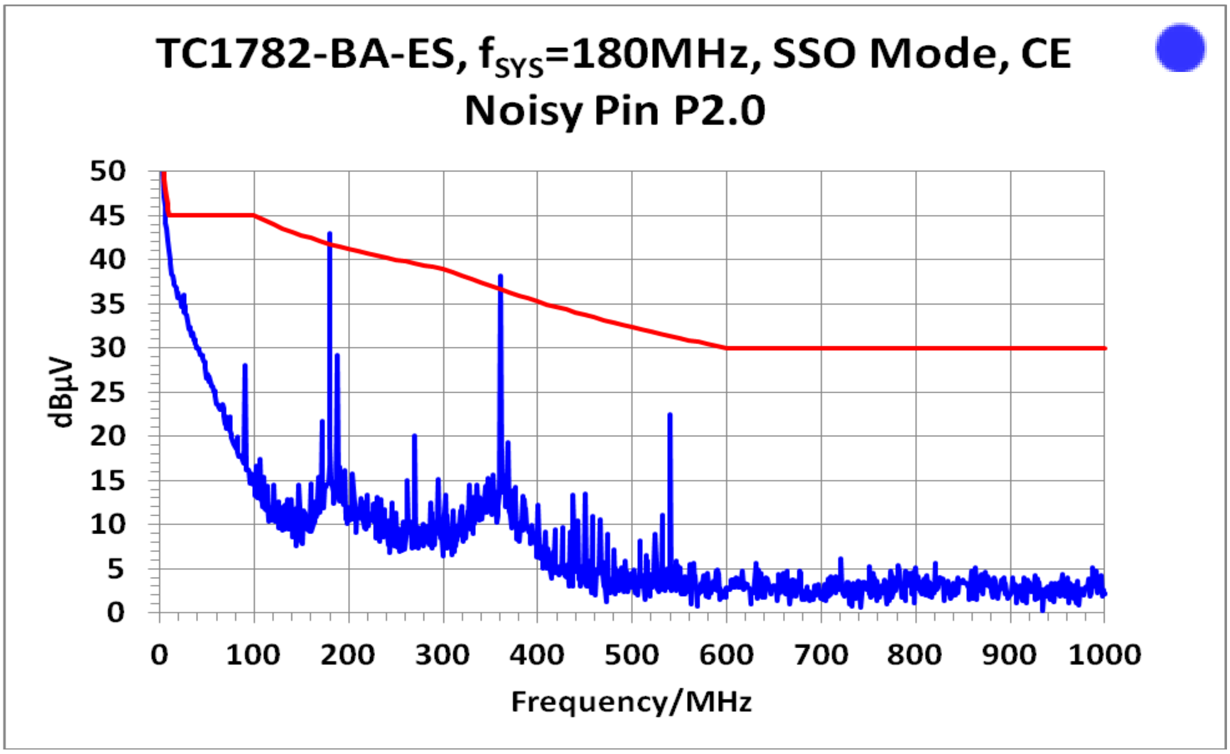

Figure 19 TC1782; Application pattern; 180 MHz; worst-case I/O conducted

6.4 Microcontroller TC1784

6.4.1 TC1784: Probed nets

Fig. 20 shows the location of the four nets selected for emission measurement:

- VDD 1.3V
- VDDP 3.3V
- P10.12 (min. noise level)
- P1.5 (max. noise level)

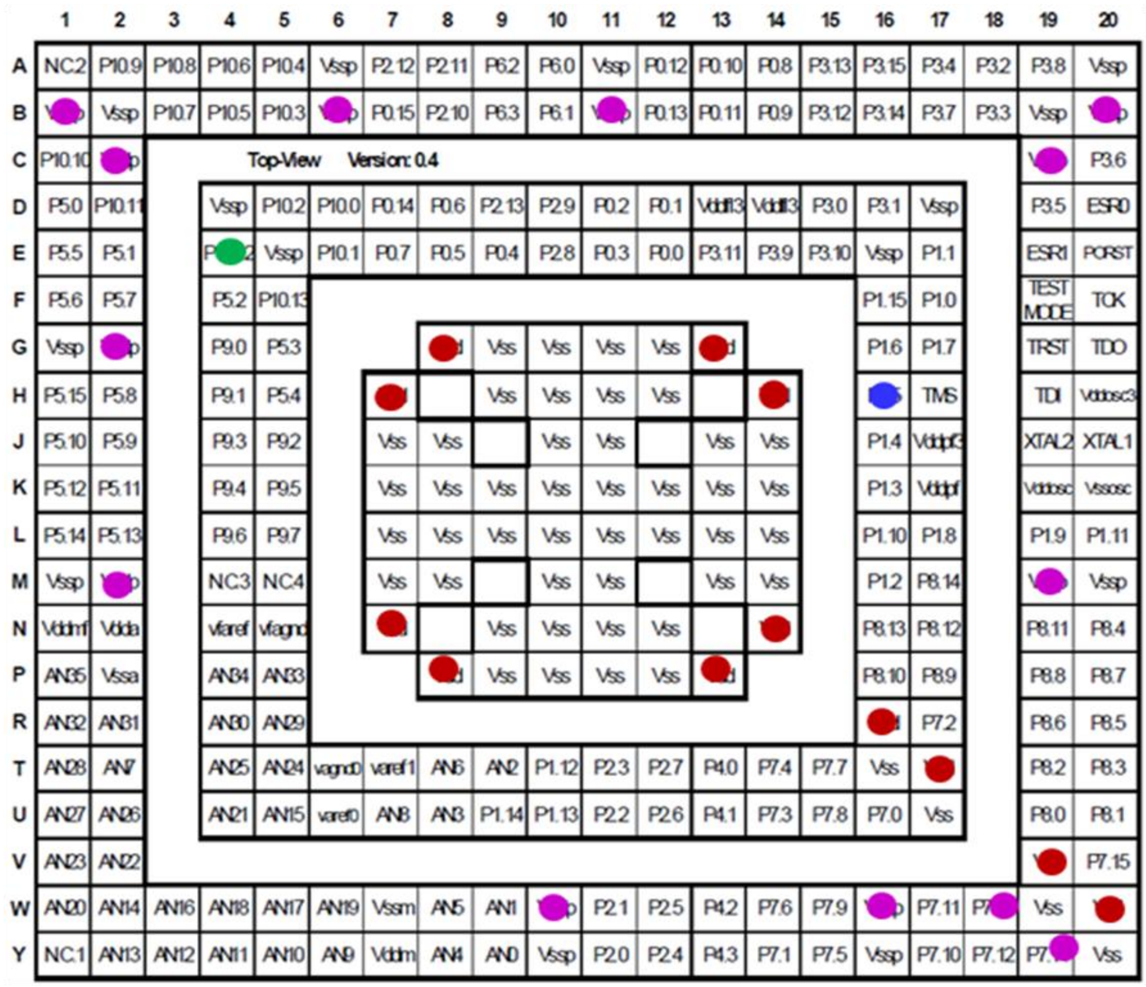

Figure 20 TC1784 probed nets for electromagnetic emission

6.4.2 TC1784: Result summary

The TC1784 violates the BISS emission limits on VDD (2nd, 3rd, 4th harmonic: +5..10 dBµV).

The TC1784 reaches the BISS emission limits on port pins close to oscillator (e.g. P1.5) due to strong oscillator clock crosstalk; critical frequency is the oscillator base frequency.

The oscillator should be operated with series resistor (e.g. 1 kΩ) between XTAL2 pin and crystal. Furthermore, the oscillator gain may be reduced to level 2 (second-strongest value).

The power supply should be routed carefully; at least four PCB layers are recommended.

6.4.3 TC1784: Conducted emission results

Fig. 21-24 show the emission measurement results at the four probed nets.

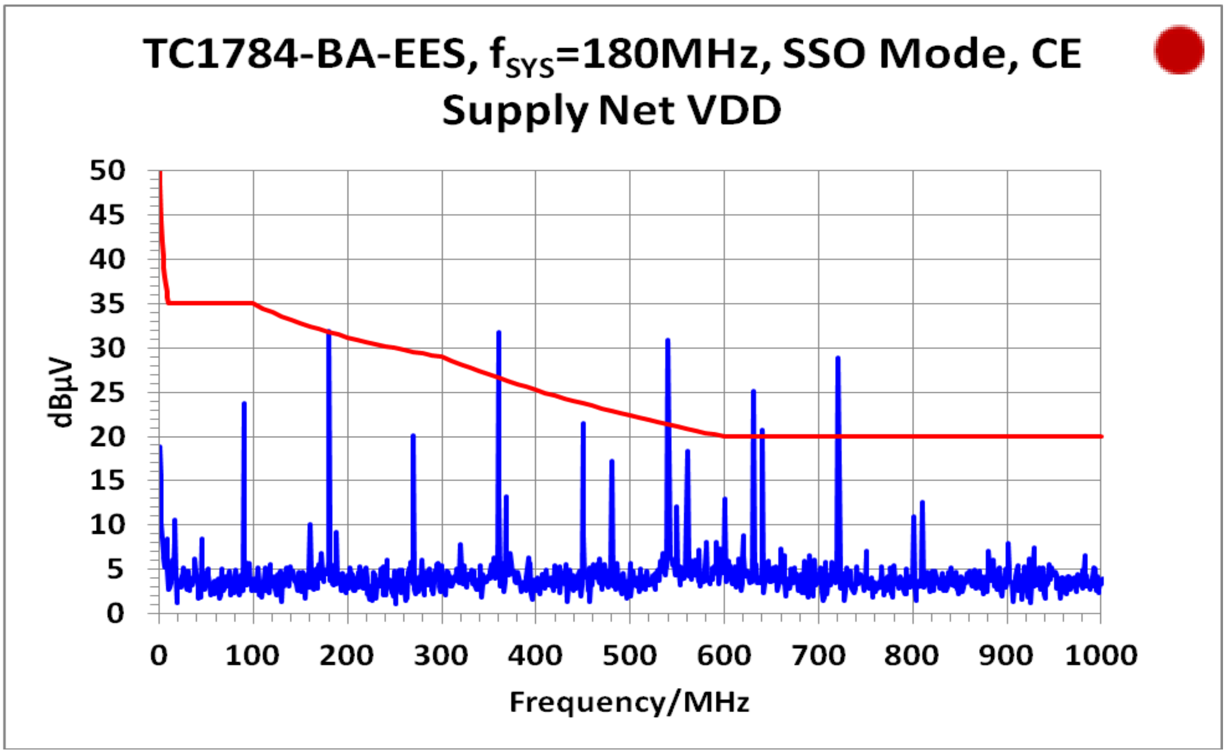

Figure 21 TC1784; Application pattern; 180 MHz; VDD conducted

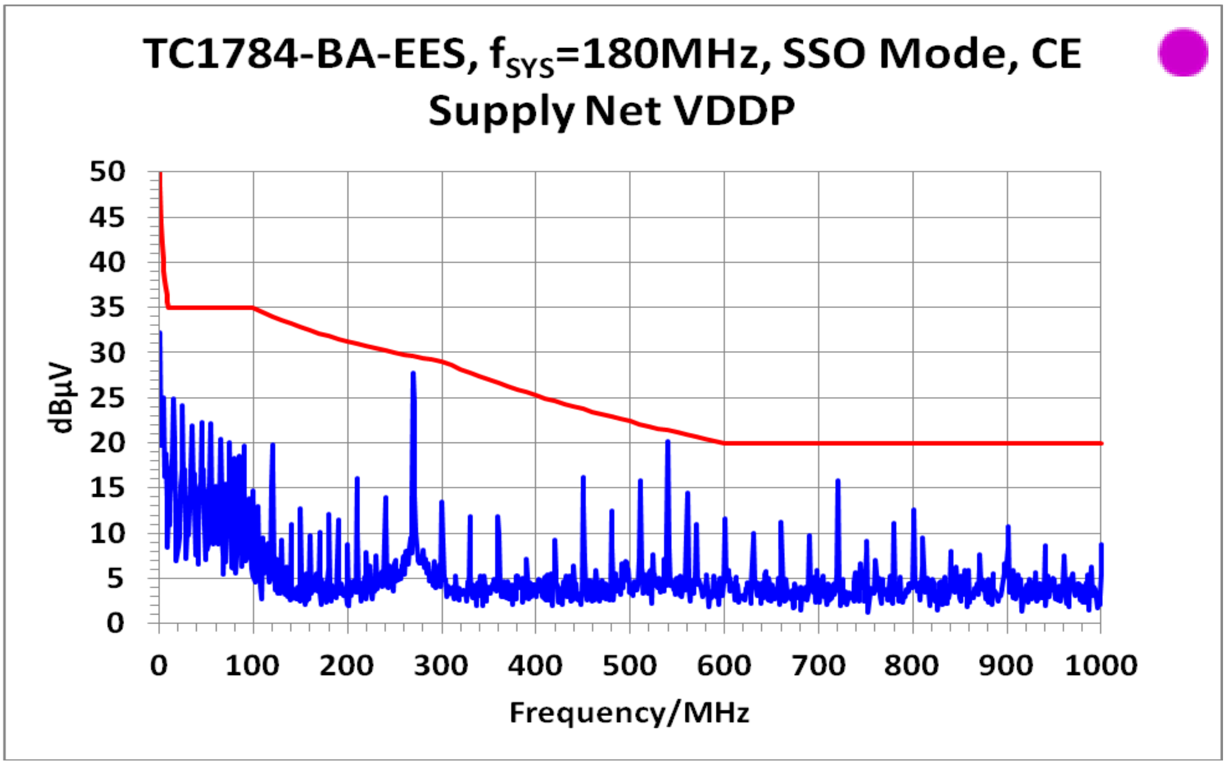

Figure 22 TC1784; Application pattern; 180 MHz; VDDP conducted

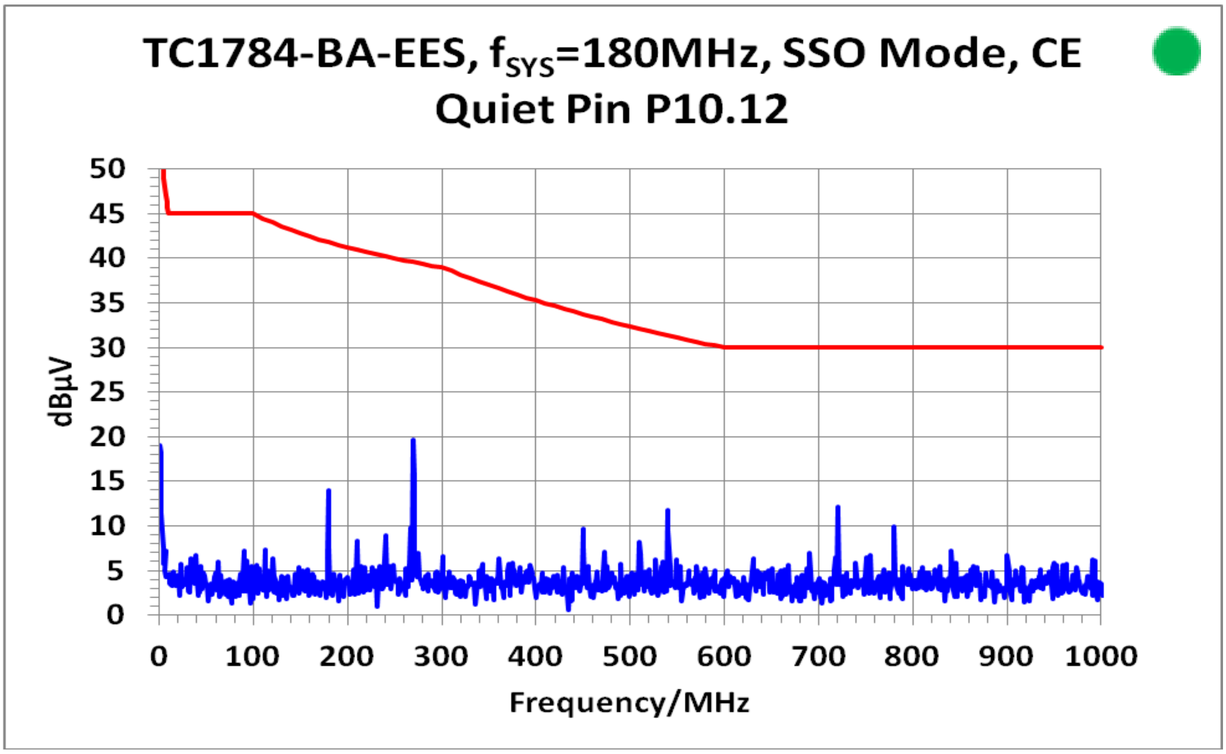

Figure 23 TC1784; Application pattern; 180 MHz; best-case I/O conducted

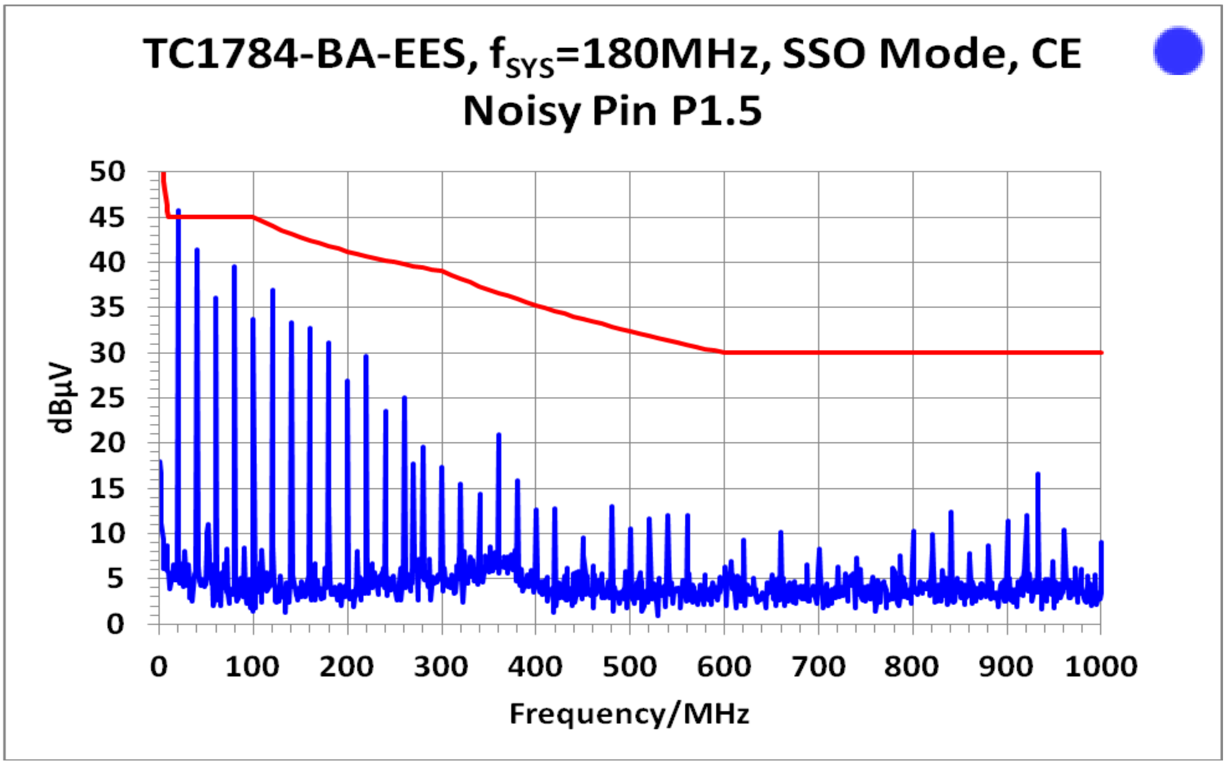

Figure 24 TC1784; Application pattern; 180 MHz; worst-case I/O conducted

6.5 Microcontroller TC1791

6.5.1 TC1791: Probed nets

Fig. 25 shows the location of the four nets selected for emission measurement:

- VDD 1.3V
- VDDP 3.3V
- P8.2 (min. noise level)
- P9.14 (max. noise level)

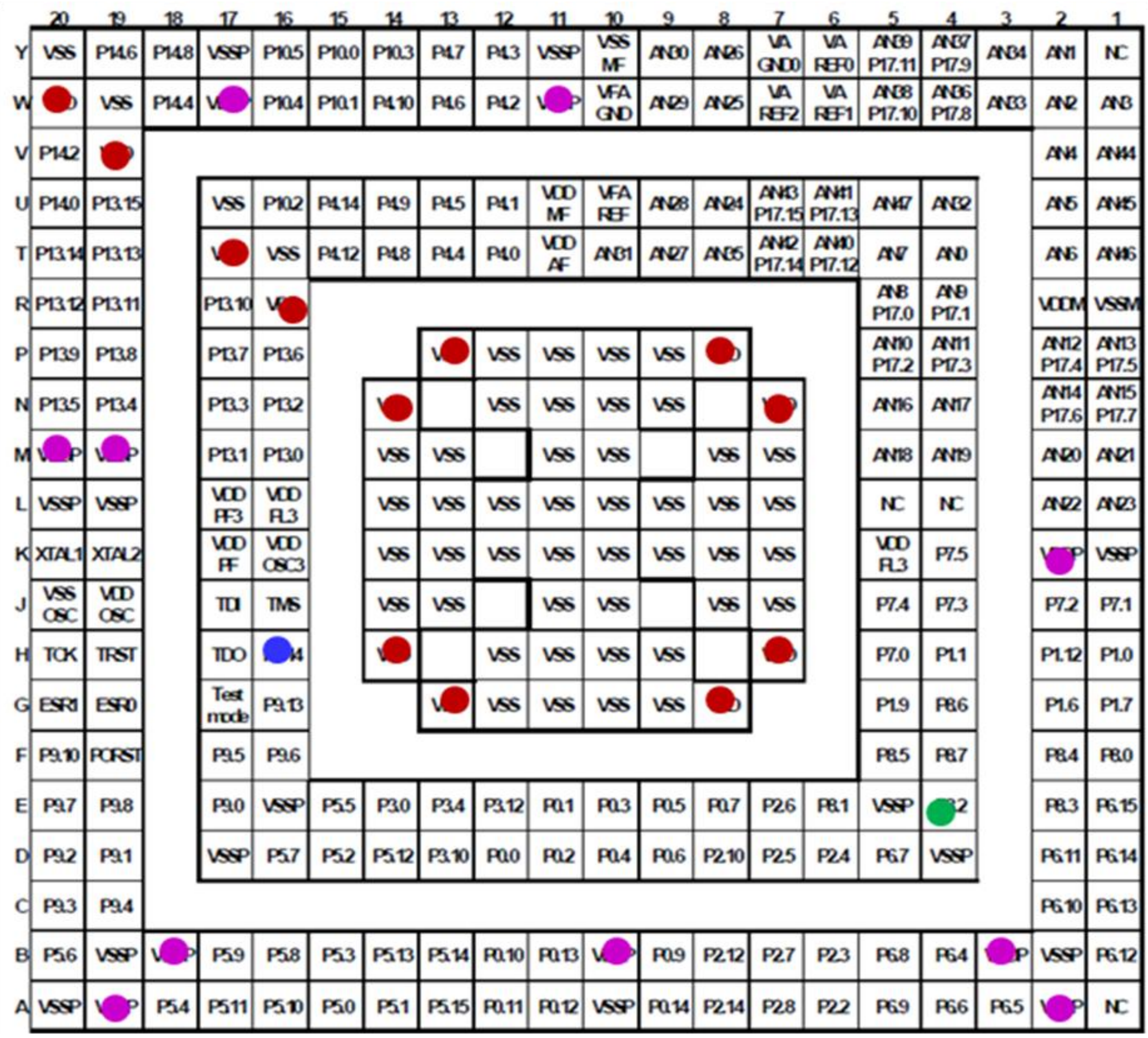

Figure 25 TC1791 probed nets for electromagnetic emission

6.5.2 TC1791: Result summary

The TC1791 violates BISS emission limits on the power supply net VDD (system clock divided by 3: +3 dBµV). The system frequency itself touches the BISS limit.

The TC1791 exceeds the BISS emission limits by 9 dBµV on port pins close to oscillator (e.g. P9.14) due to strong oscillator clock crosstalk; critical frequency is the oscillator base frequency.

The oscillator should be operated with series resistor (e.g. 1 kΩ) between XTAL2 pin and crystal. Furthermore, the oscillator gain may be reduced to level 2 (second-strongest value).

6.5.3 TC1791: Conducted emission results

Fig. 26-29 show the emission measurement results at the four probed nets.

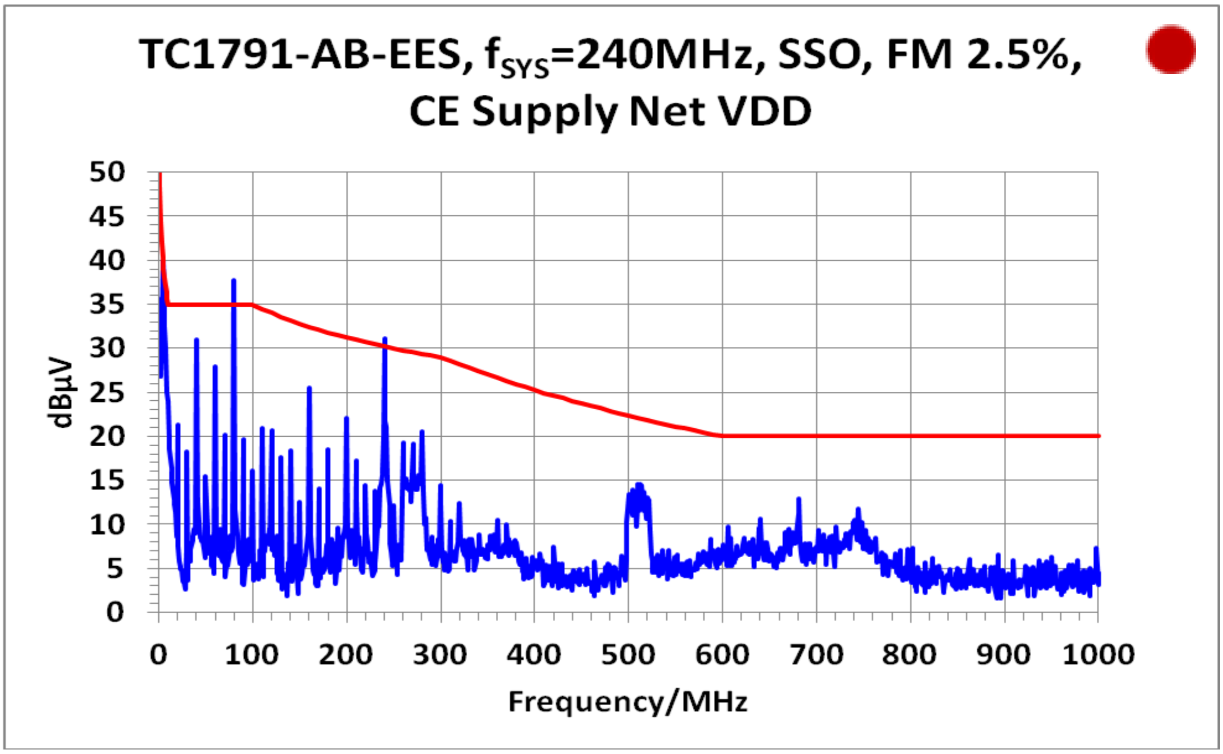

Figure 26 TC1791; Application pattern; 240 MHz; VDD conducted

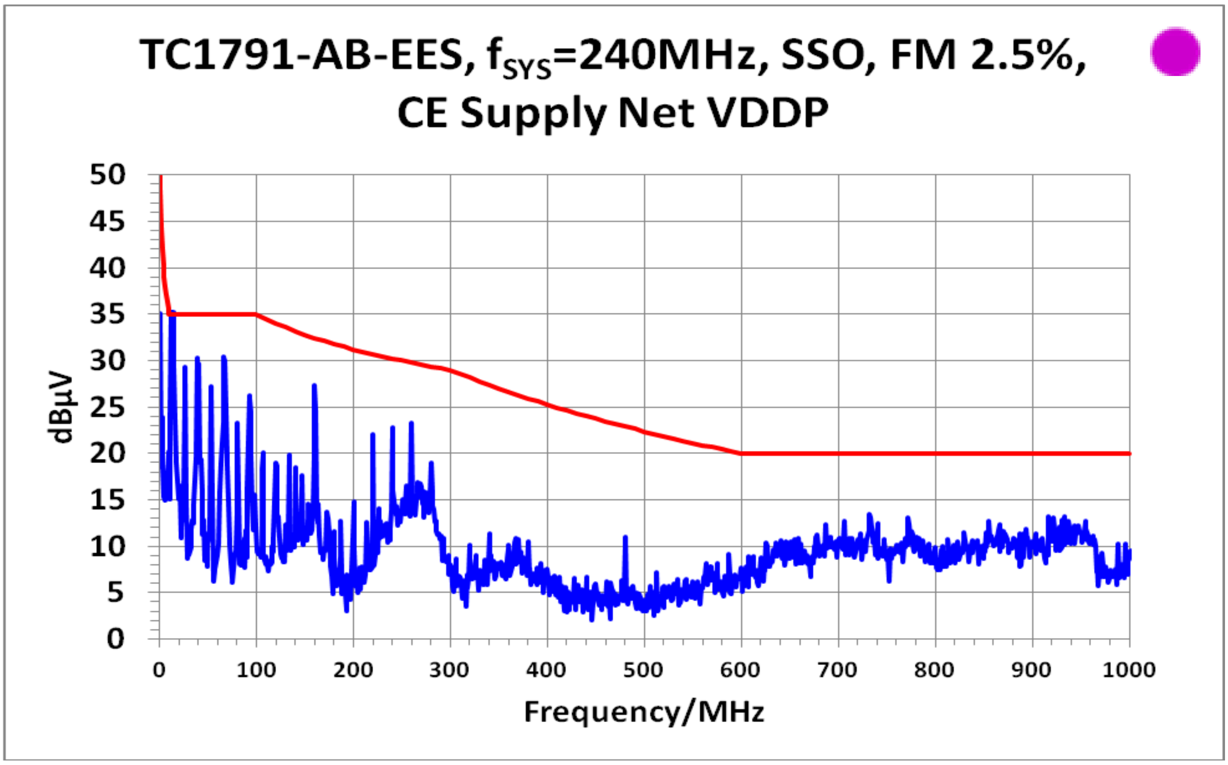

Figure 27 TC1791; Application pattern; 240 MHz; VDDP conducted

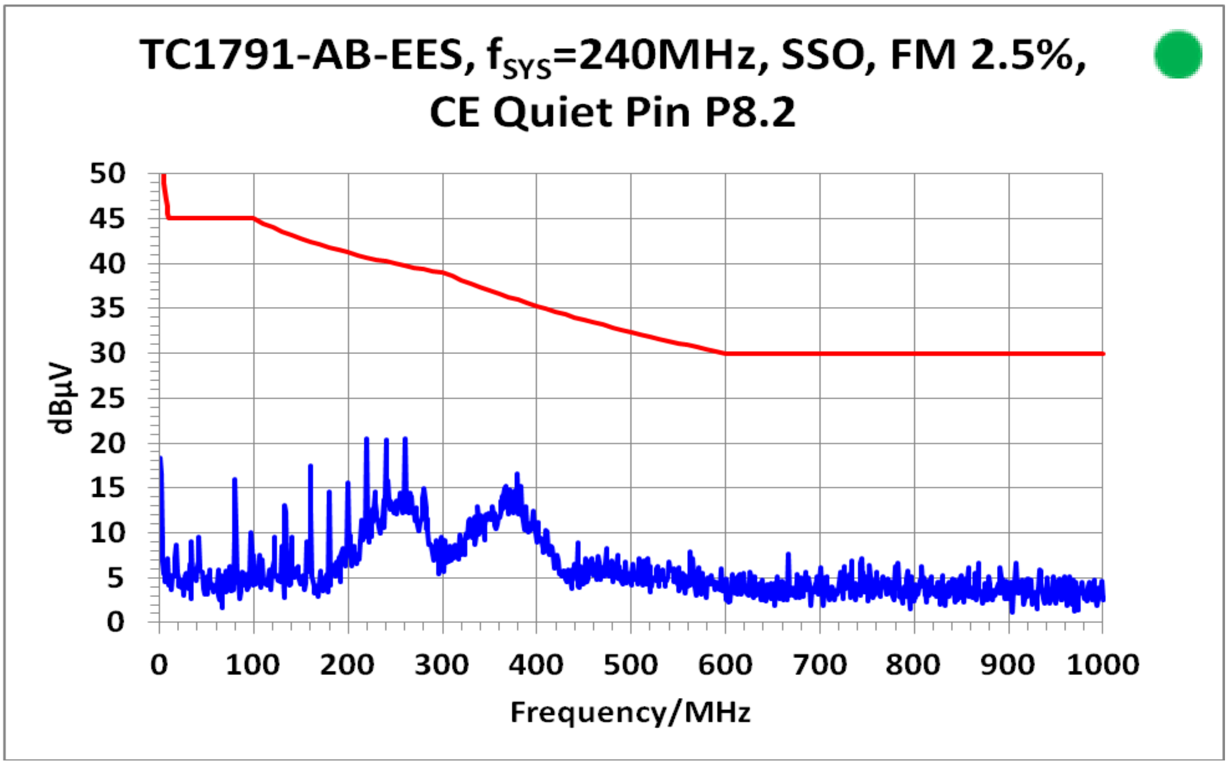

Figure 28 TC1791; Application pattern; 240 MHz; best-case I/O conducted

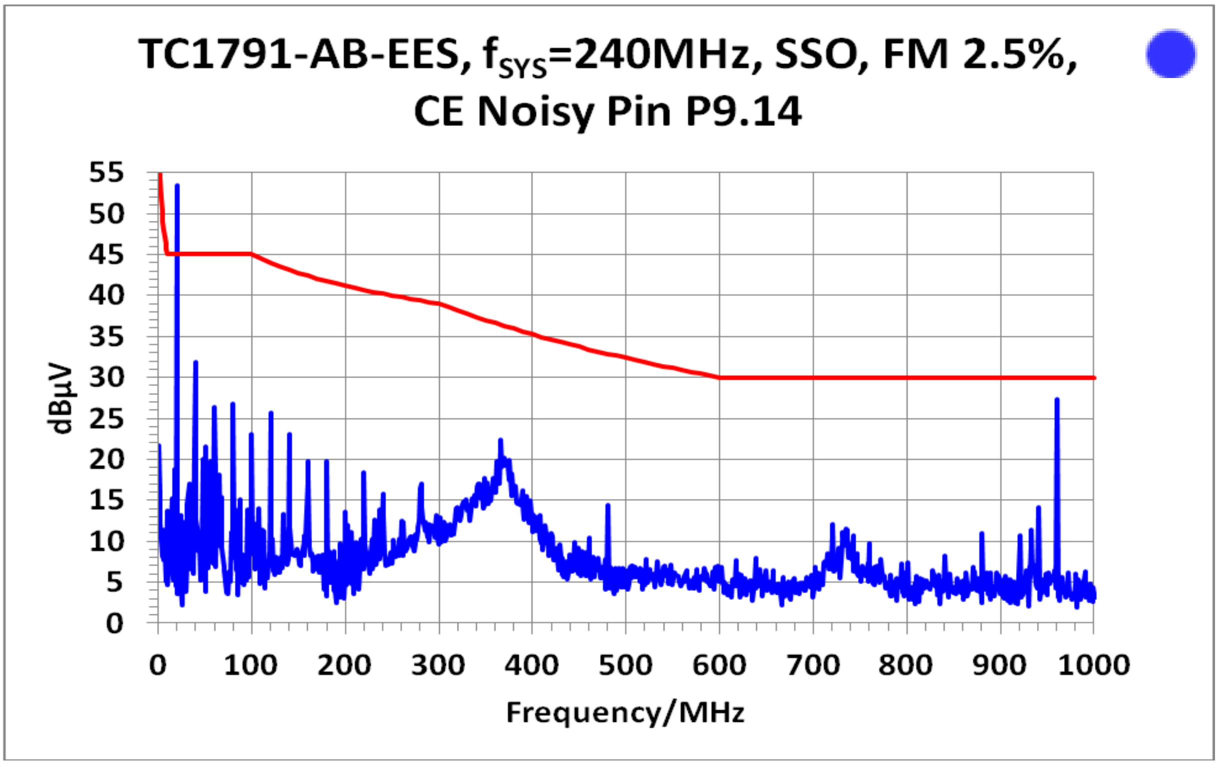

Figure 29 TC1791; Application pattern; 240 MHz; worst-case I/O conducted

6.6 Microcontroller TC1793

6.6.1 TC1793: Probed nets

Fig. 30 shows the location of the four nets selected for emission measurement:

- VDD 1.3V
- VDDP 3.3V
- P3.1 (min. noise level)
- P1.3 (max. noise level)

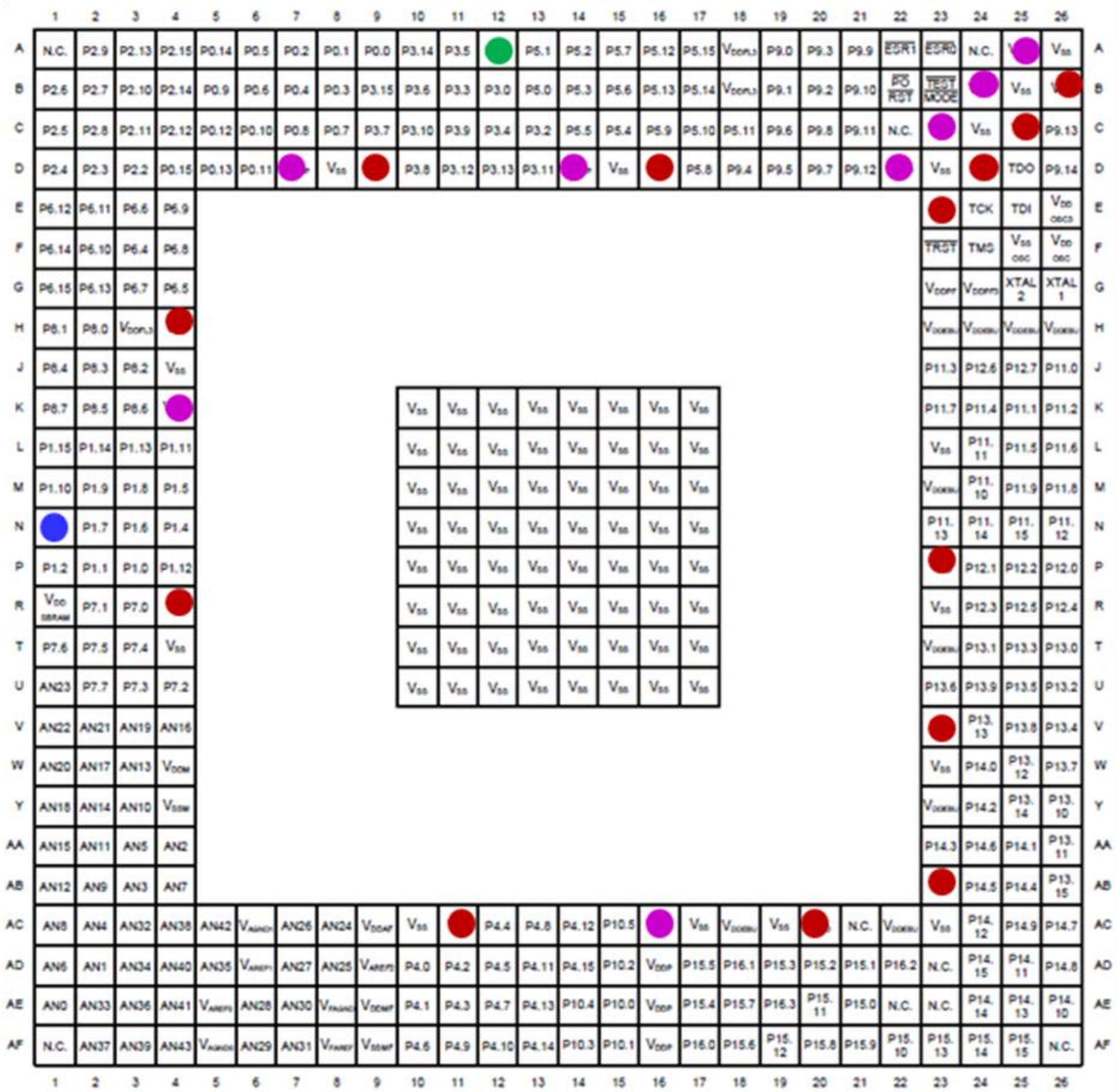

Figure 30 TC1793 probed nets for electromagnetic emission

6.6.2 TC1793: Result summary

The TC1782 generally fulfills the BISS emission limits on all nets.

Worst-case I/O emission might exceed the BISS limit at very low frequencies. External filters may be considered for port pins which leave the application board.

6.6.3 TC1793: Conducted emission results

Fig. 31-34 show the emission measurement results at the four probed nets.

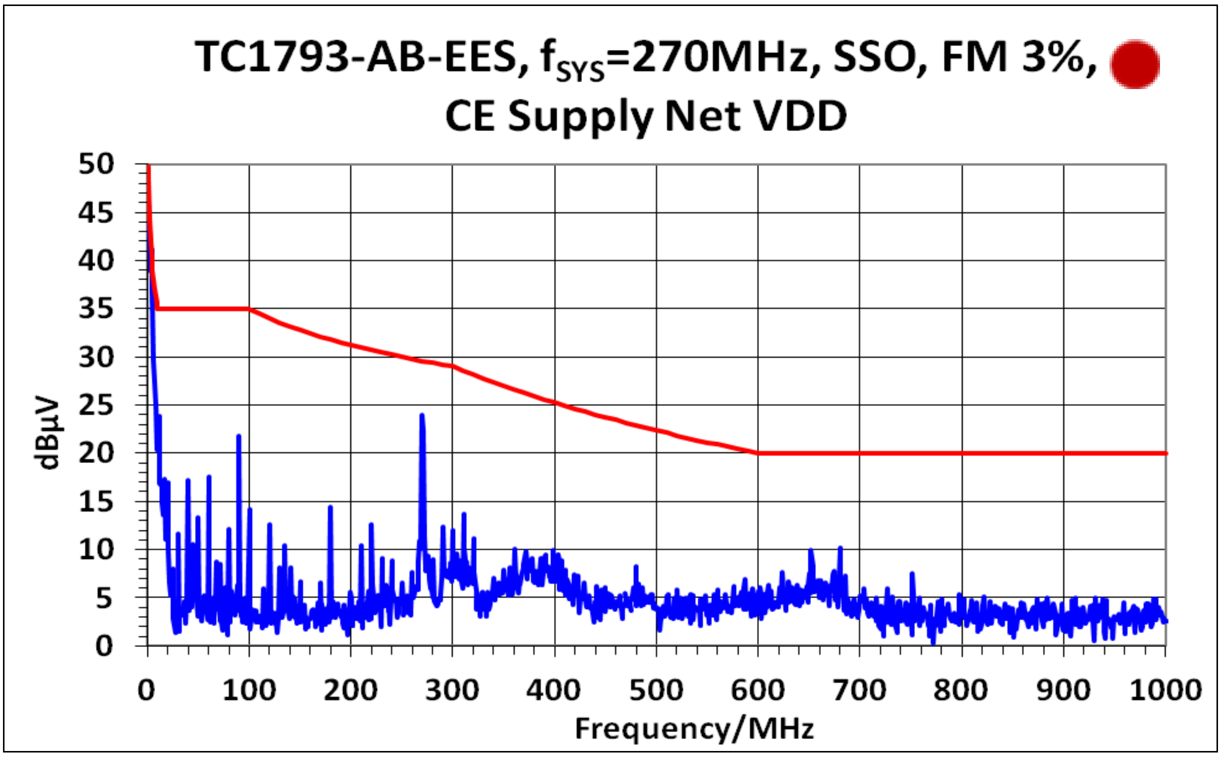

Figure 31 TC1793; Application pattern; 270 MHz; VDD conducted

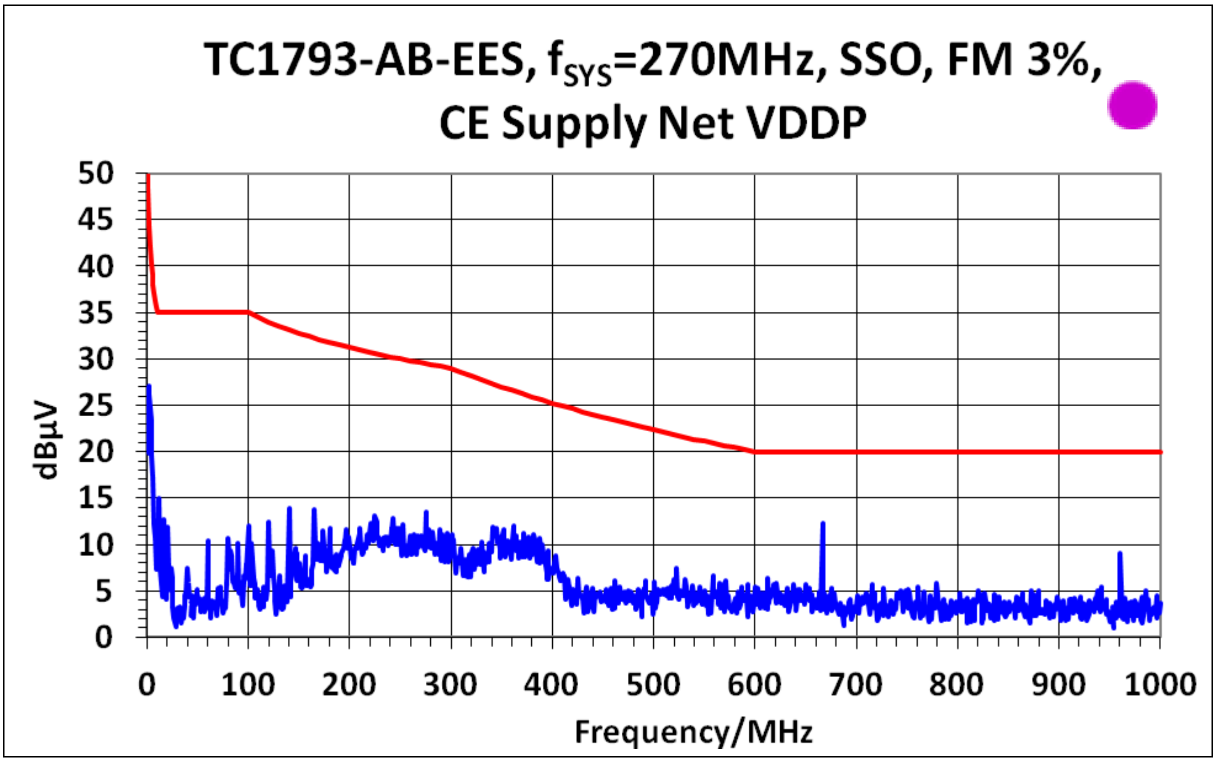

Figure 32 TC1793; Application pattern; 270 MHz; VDDP conducted

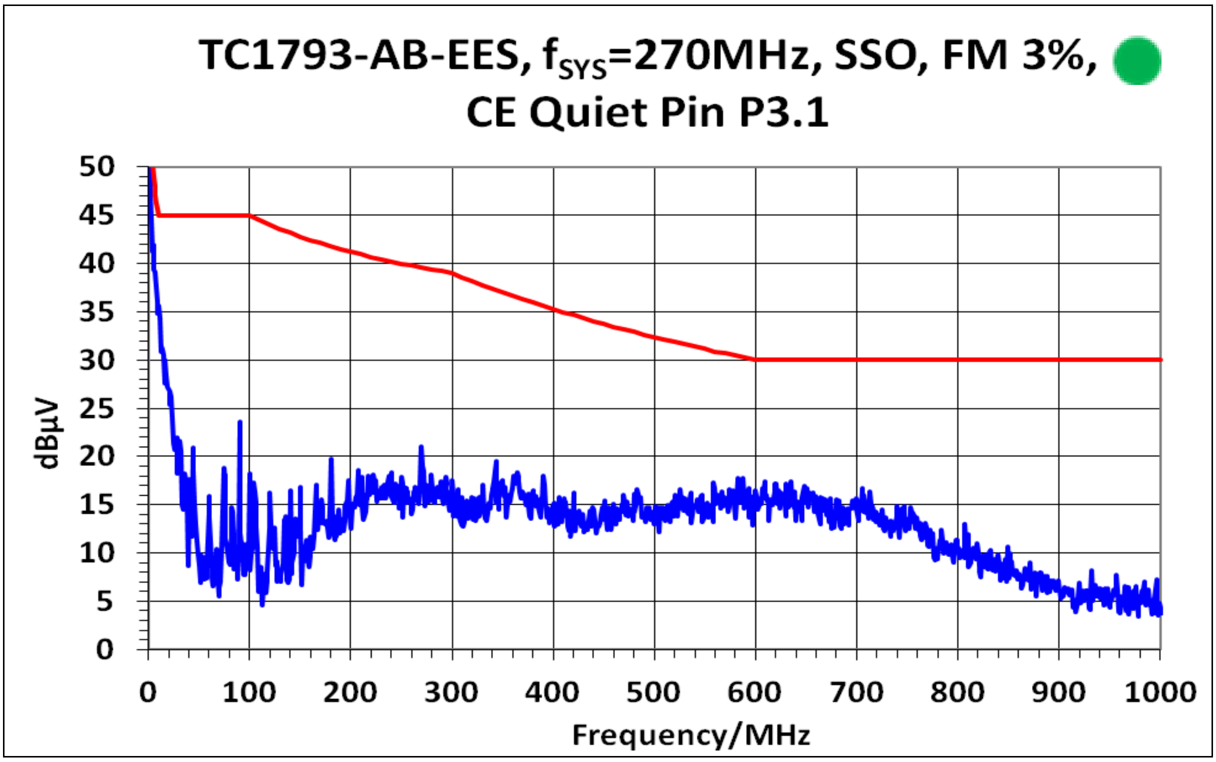

Figure 33 TC1793; Application pattern; 270 MHz; best-case I/O conducted

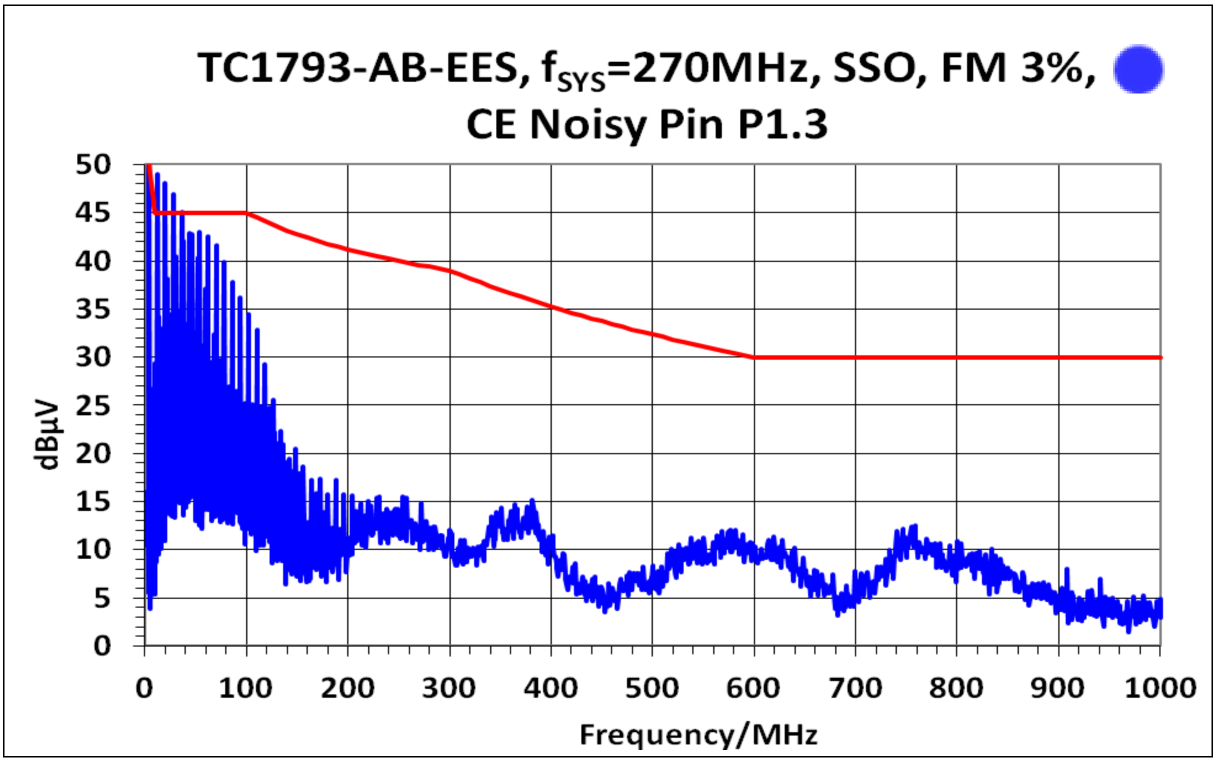

Figure 34 TC1793; Application pattern; 270 MHz; worst-case I/O conducted

6.7 Microcontroller TC1798

6.7.1 TC1798: Probed nets

Fig. 35 shows the location of the four nets selected for emission measurement:

- VDD 1.3V
- VDDP 3.3V
- P2.6 (min. noise level)
- P9.14 (max. noise level)

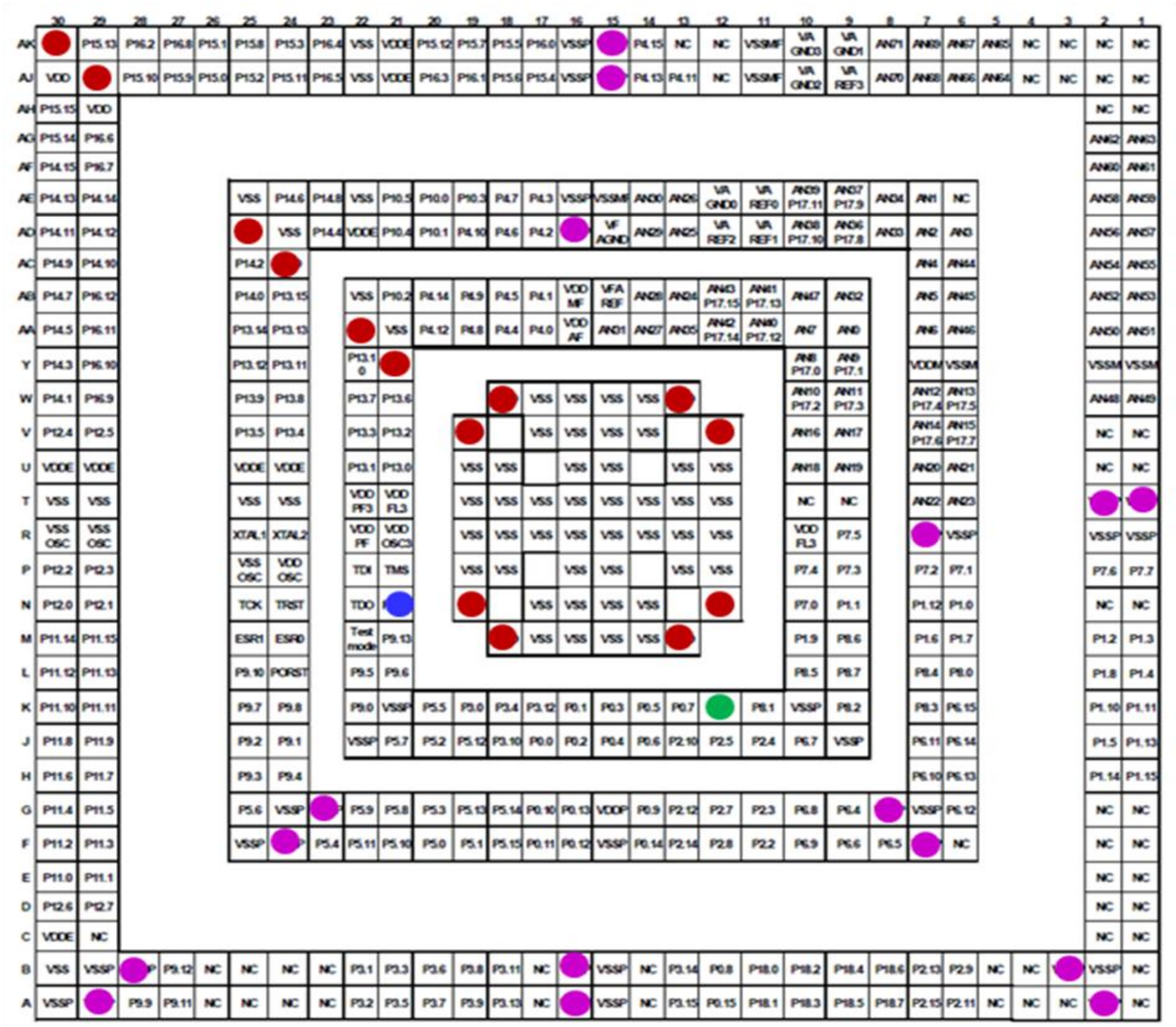

Figure 35 TC1798 probed nets for electromagnetic emission

6.7.2 TC1798: Result summary

The TC1798 violates BISS emission limits on the power supply net VDD (system clock divided by 3: +3 dBµV). The system frequency itself touches the BISS limit.

The TC1798 exceeds the BISS emission limits by 6 dBµV on port pins close to oscillator (e.g. P9.14) due to strong oscillator clock crosstalk; critical frequency is the oscillator base frequency.

The oscillator should be operated with series resistor (e.g. 1 kΩ) between XTAL2 pin and crystal. Furthermore, the oscillator gain may be reduced to level 2 (second-strongest value).

6.7.3 TC1798: Conducted emission results

Fig. 36-39 show the emission measurement results at the four probed nets.

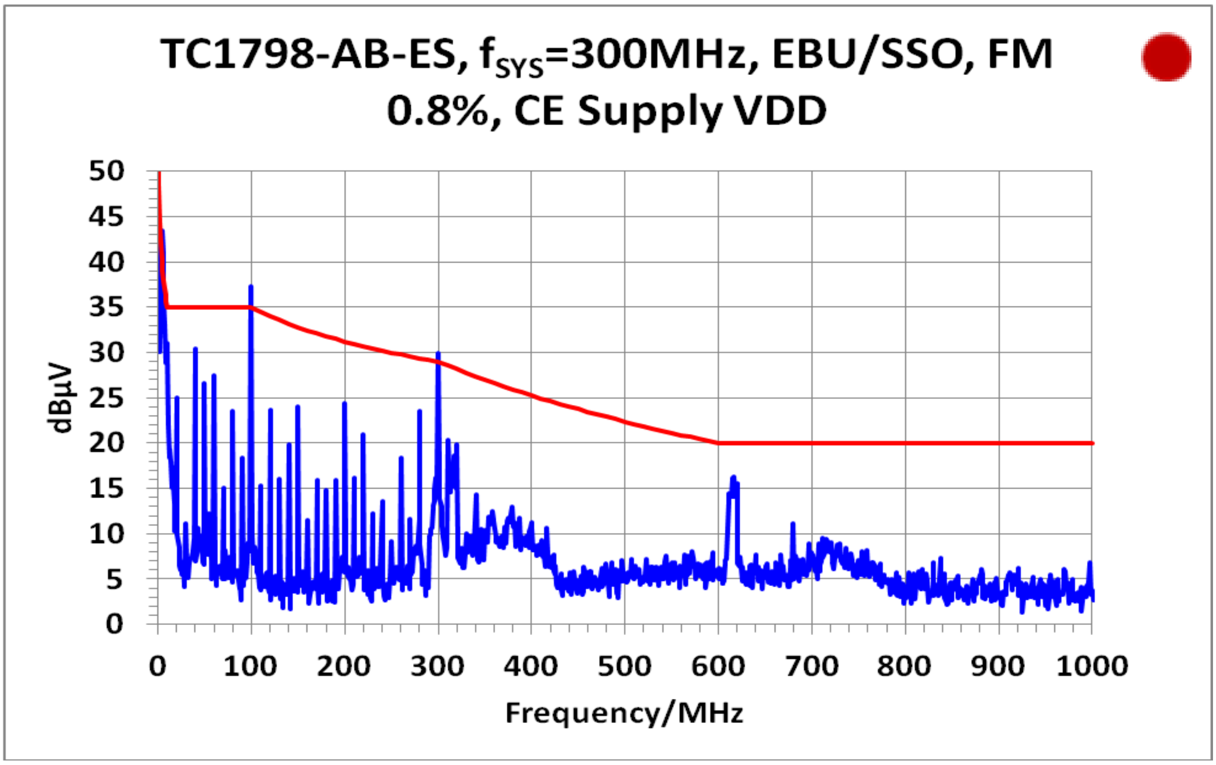

Figure 36 TC1798; Application pattern; 300 MHz; VDD conducted

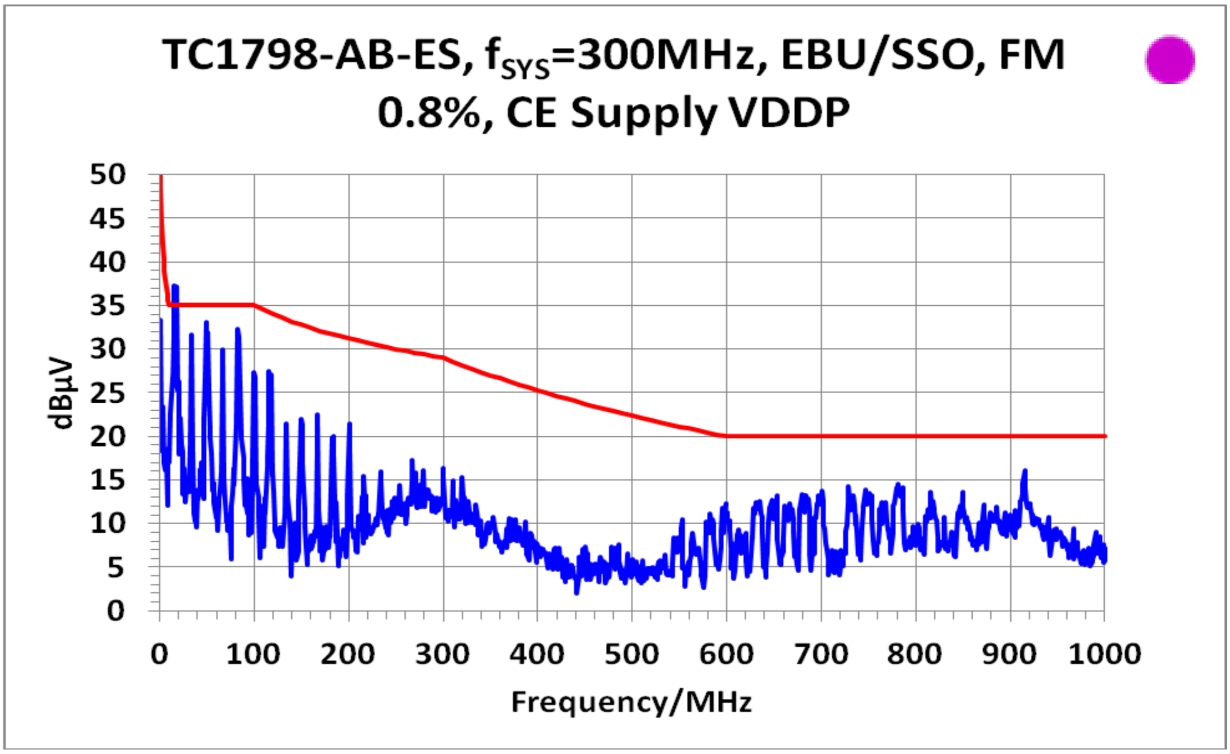

Figure 37 TC1798; Application pattern; 300 MHz; VDDP conducted

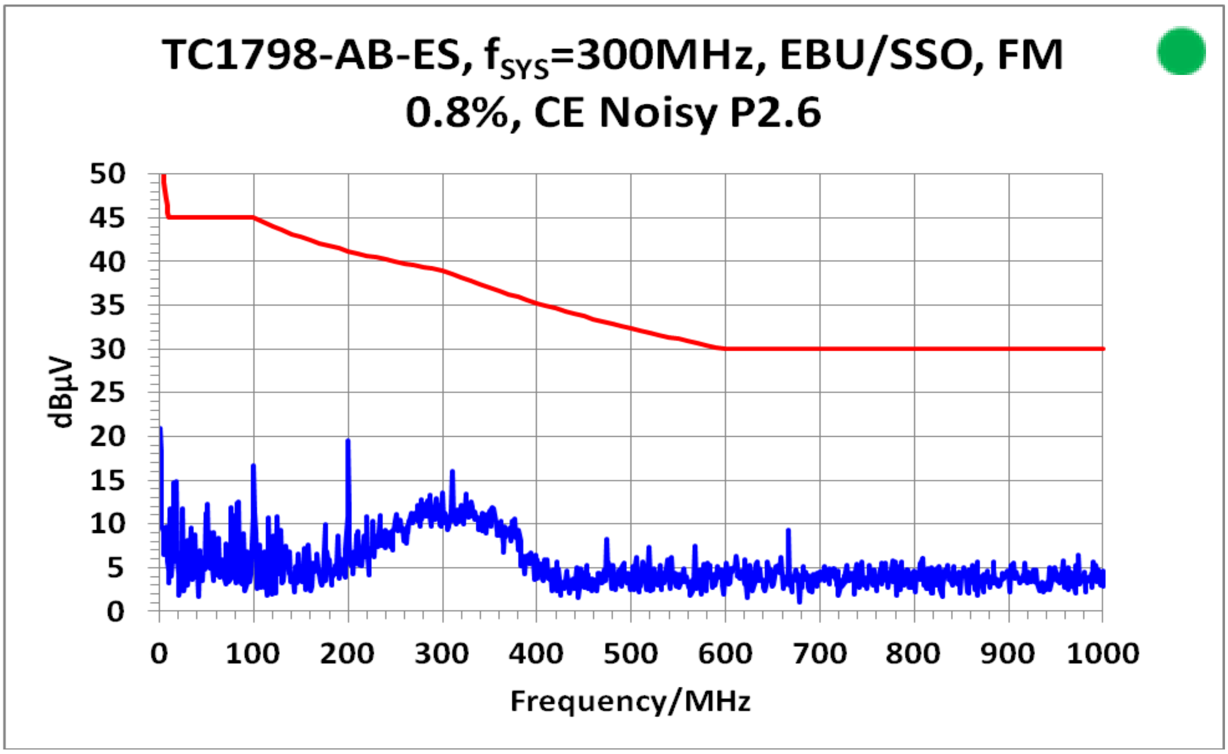

Figure 38 TC1798; Application pattern; 300 MHz; best-case I/O conducted

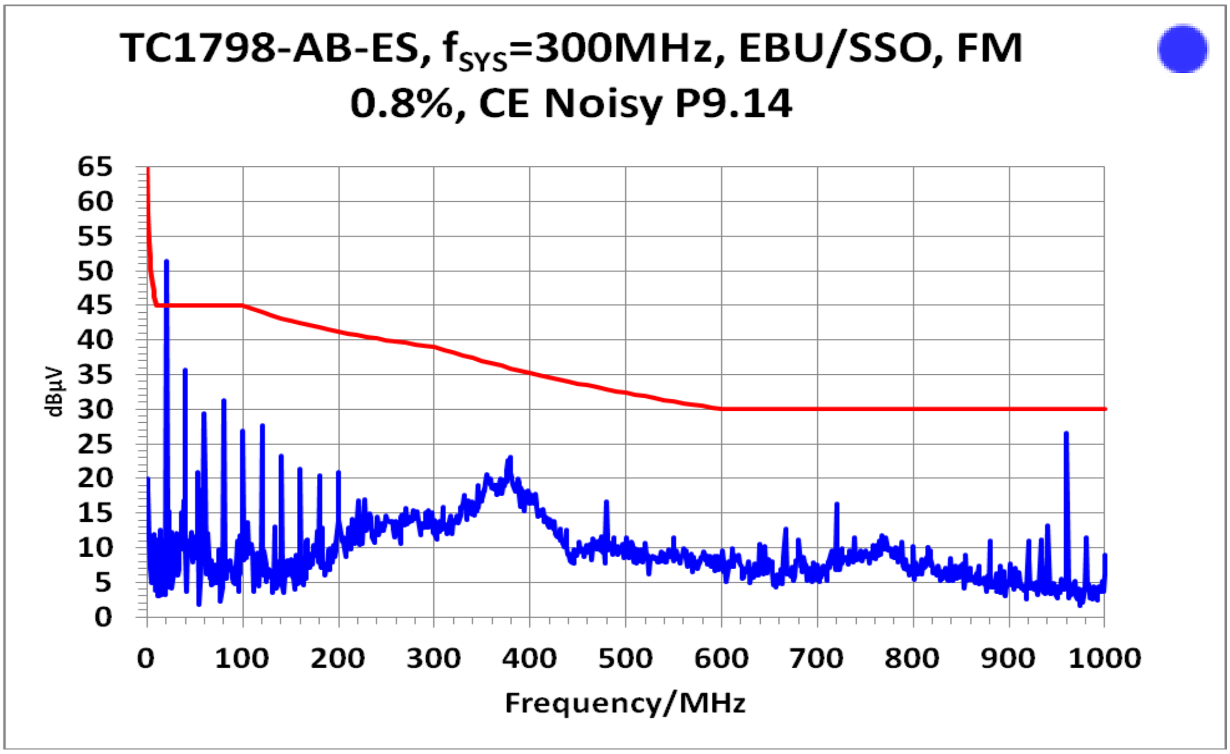

Figure 39 TC1798; Application pattern; 300 MHz; worst-case I/O conducted

7 Radiated emission measurement results

7.1 Microcontroller TC1724

7.1.1 TC1724: Radiated emission result summary

The TC1724 fulfills the BISS emission limits except 7th system clock harmonic: +9 dBµV.

7.1.2 TC1724: Radiated emission result

Fig. 40 shows the radiated emission measurement result.

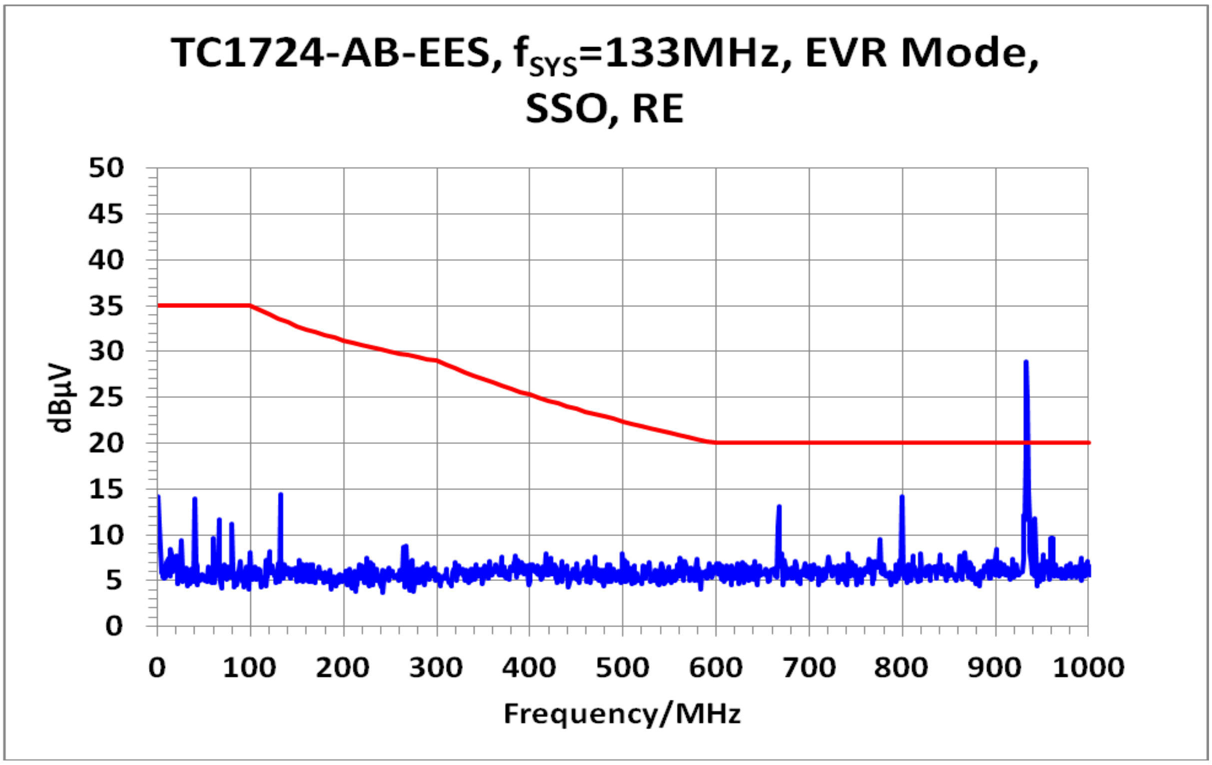

Figure 40 TC1724; Application pattern; 133 MHz; radiated

Note: The emission peak at 933 MHz is amplified by unintended GSM interference. Mere microcontroller emission is less and should stay below the BISS limit.

7.2 Microcontroller TC1728

7.2.1 TC1728: Radiated emission result summary

The TC1728 fulfills the BISS emission limits except 7th system clock harmonic: +3 dBµV.

7.2.2 TC1728: Radiated emission result

Fig. 41 shows the radiated emission measurement result.

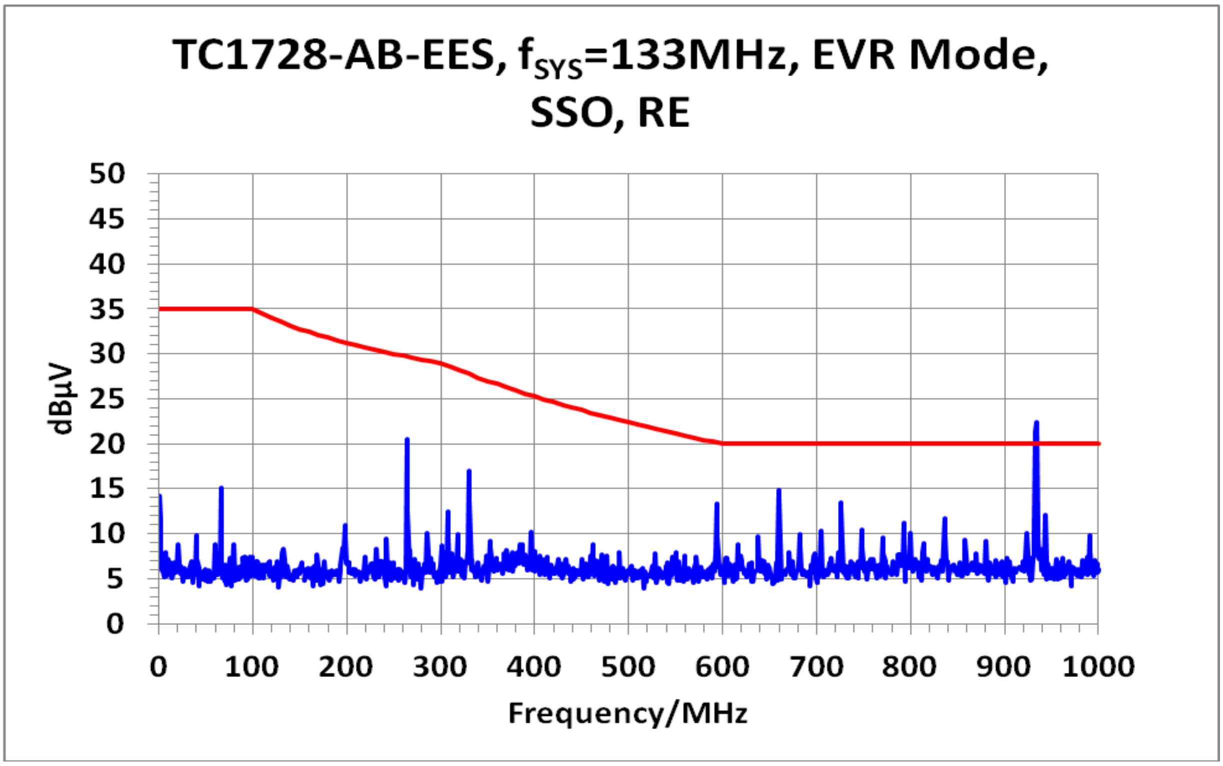

Figure 41 TC1728; Application pattern; 133 MHz; radiated

Note: The emission peak at 933 MHz is amplified by unintended GSM interference. Mere microcontroller emission is less and should stay below the BISS limit.

7.3 Microcontroller TC1782

7.3.1 TC1782: Radiated emission result summary

The TC1782 fulfills the BISS emission limits except in the range between 500 and 650 MHz: +2 dBµV.

7.3.2 TC1782: Radiated emission result

Fig. 42 shows the radiated emission measurement result.

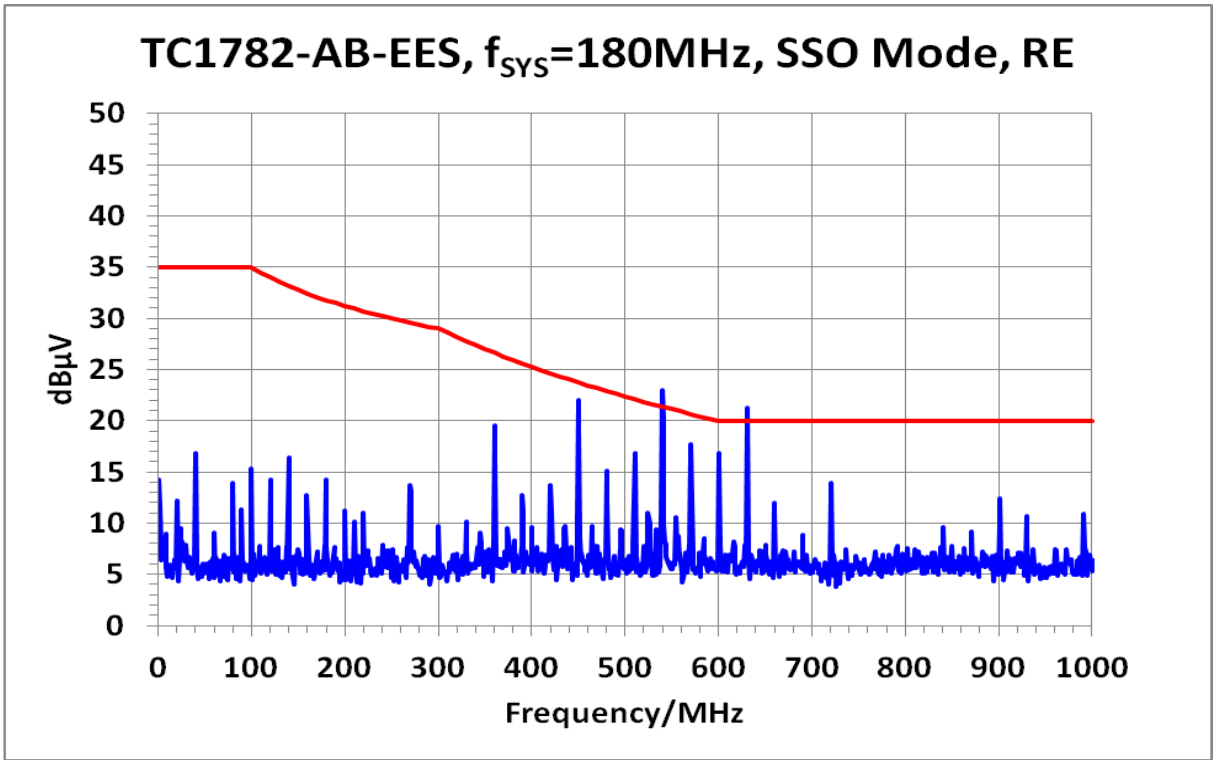

Figure 42 TC1782; Application pattern; 180 MHz; radiated

7.4 Microcontroller TC1784

7.4.1 TC1784: Radiated emission result summary

The TC1784 fulfills the BISS emission limits.

7.4.2 TC1784: Radiated emission result

Fig. 43 shows the radiated emission measurement result.

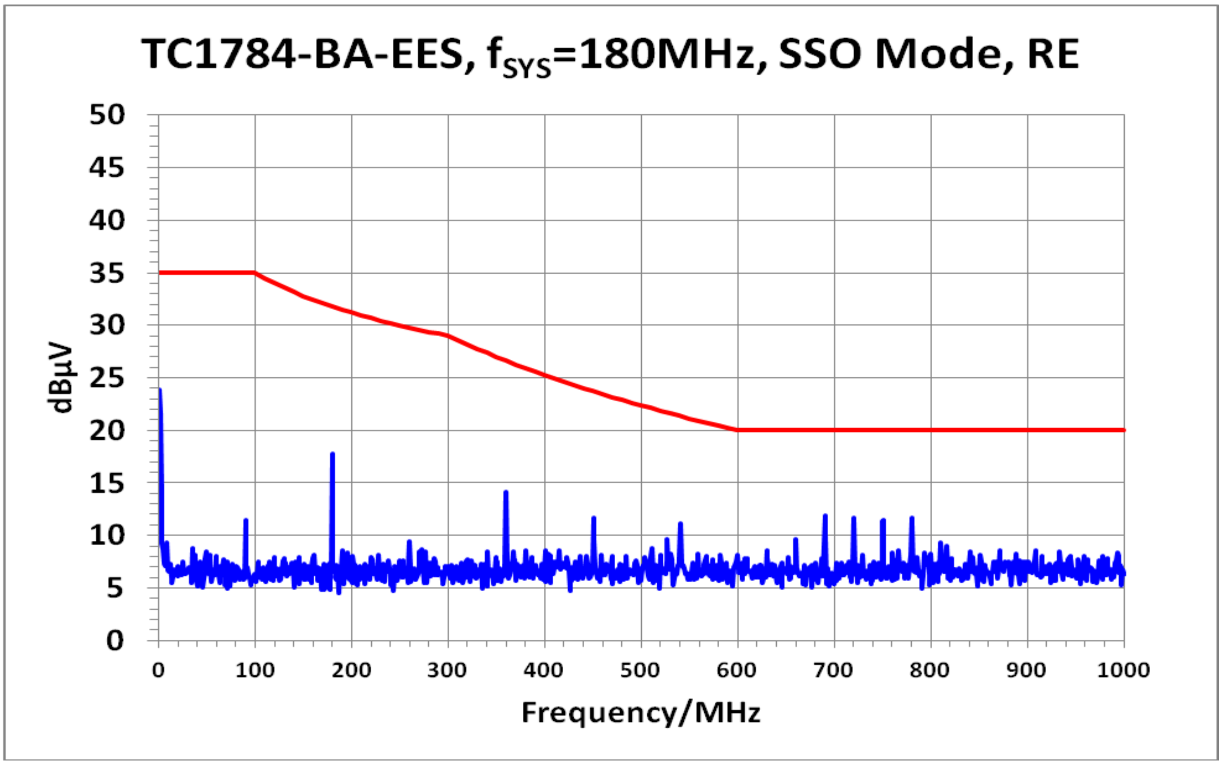

Figure 43 TC1784; Application pattern; 180 MHz; radiated

7.5 Microcontroller TC1791

7.5.1 TC1791: Radiated emission result summary

The TC1791 fulfills the BISS emission limits.

7.5.2 TC1791: Radiated emission result

Fig. 44 shows the radiated emission measurement result.

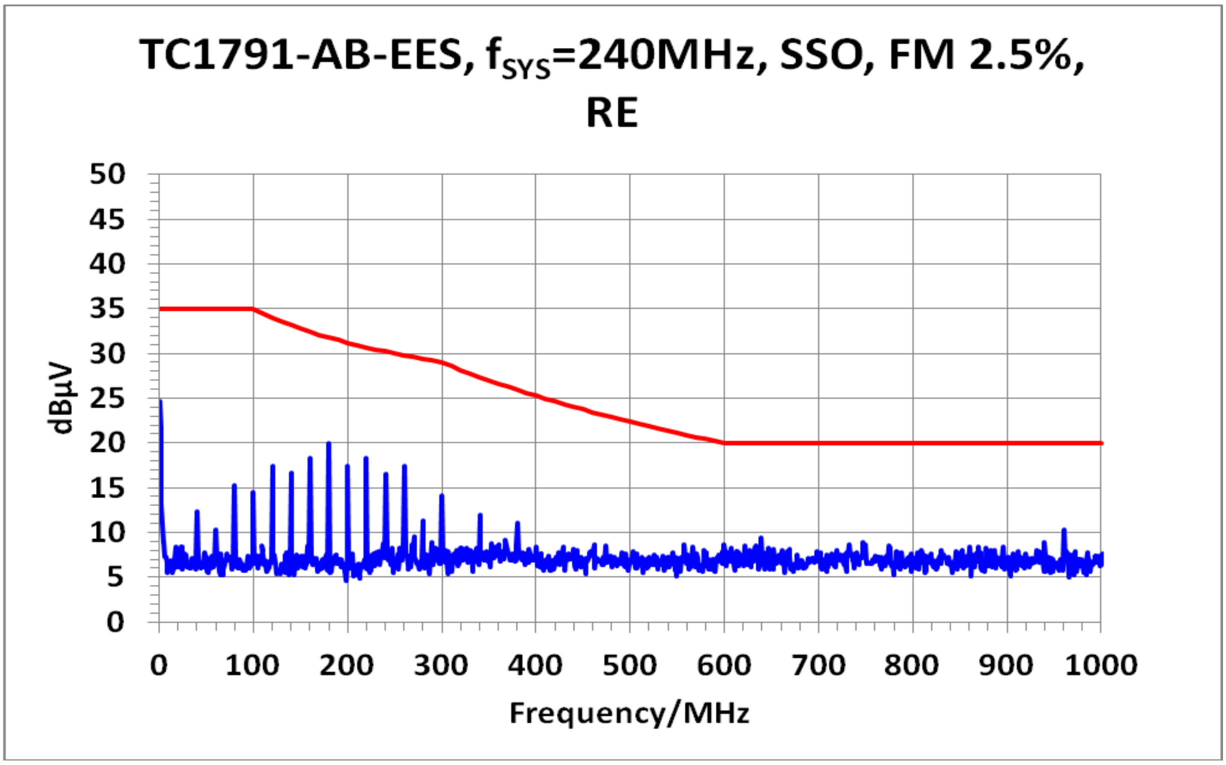

Figure 44 TC1791; Application pattern; 240 MHz; radiated

7.6 Microcontroller TC1793

7.6.1 TC1793: Radiated emission result summary

The TC1793 fulfills the BISS emission limits.

7.6.2 TC1793: Radiated emission result

Fig. 45 shows the radiated emission measurement result.

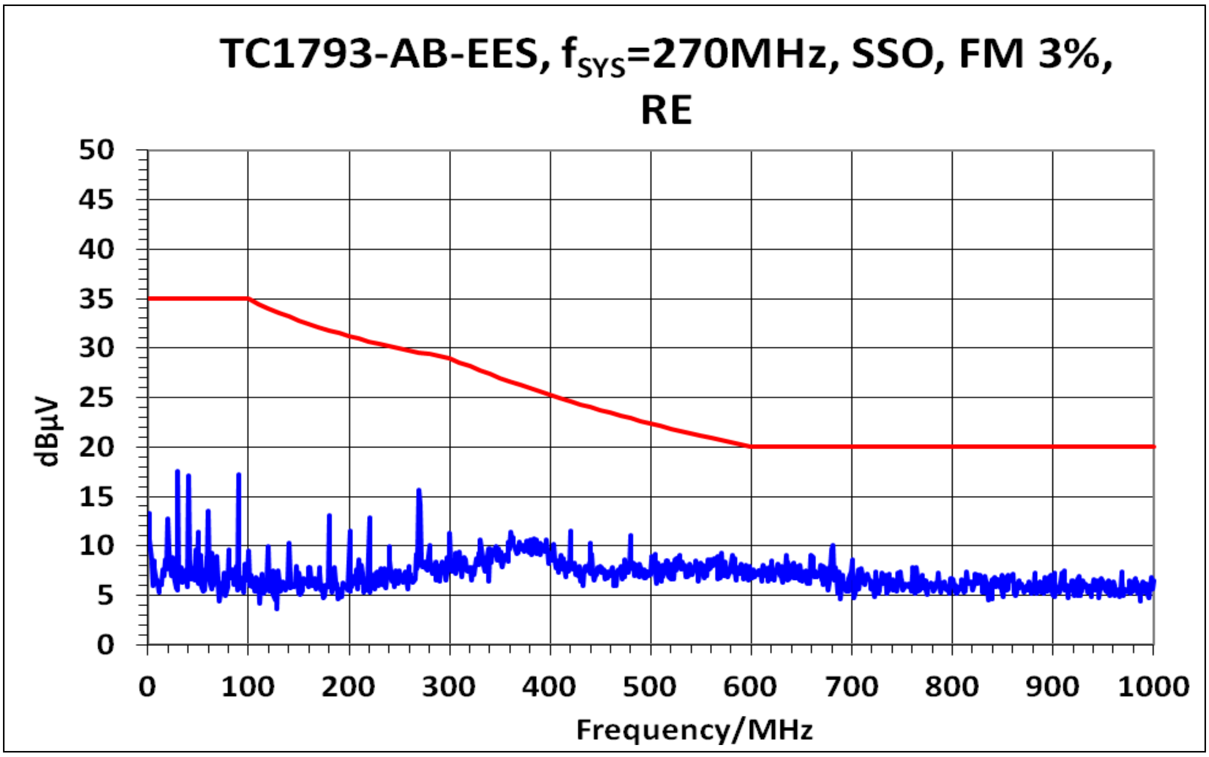

Figure 45 TC1793; Application pattern; 270 MHz; radiated

7.7 Microcontroller TC1798

7.7.1 TC1798: Radiated emission result summary

The TC1798 fulfills the BISS emission limits.

7.7.2 TC1798: Radiated emission result

Fig. 46 shows the radiated emission measurement result.

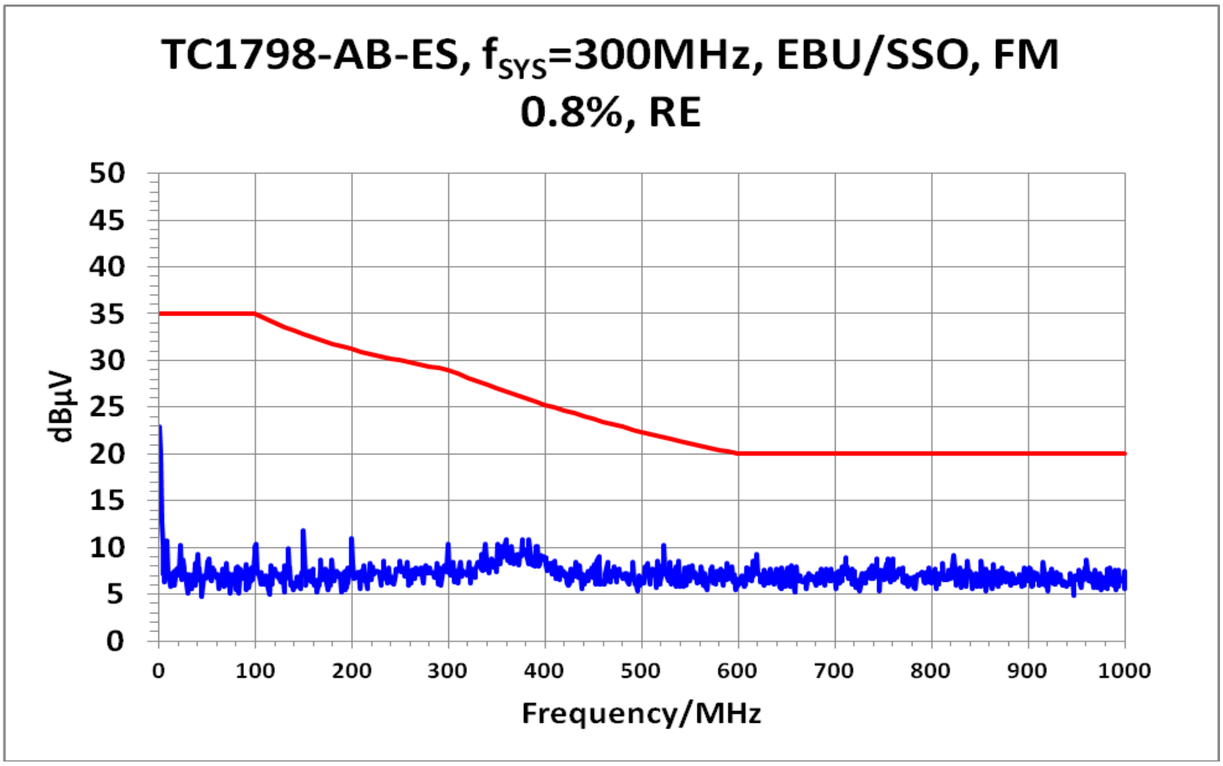

Figure 46 TC1798; Application pattern; 300 MHz; radiated

8 Microcontroller configuration impact on emission

8.1 Emission influence from exposed die pad

Exposed die pads (e-pads) are used in leadframe packages to dissipate the static and dynamic IC power from the die to the PCB without need for expensive heat sinks. Typical PCB layouts use “thermal vias” to transfer the heat from the die through the PCB to the GND plane. TC1724, TC1728 and TC1782 offer an e-pad which is electrically connected to the VSS (ground) net of the microcontroller. Since the standard assembly forms a conducting connection between the PCB trace or plane and the e-pad, the e-pad must be soldered to the PCB GND plane. The e-pads of all referenced microcontrollers in this document had been soldered to PCB-GND.

The e-pad provides a lower impedance connection and a shorter current return paths of all VSS supply pads on the die, because all VSS pads are bonded onto the e-pad surface. By connecting the e-pad to the PCB GND plane, a very low-ohmic connection between chip-GND and PCB-GND is established. For some electrical nets, this conducting e-pad connection leads to slightly higher electromagnetic emission, due to easier noise propagation from the die to the PCB. On the other hand, a disconnected e-pad leads to higher dynamic voltage drop on the die during operation, thus reducing the margin for reliable operation. The electrical device specification is nevertheless fulfilled.

The emission results in Fig. 47-50 are obtained from a TC1782 which was assembled in two ways: (1) e-pad soldered to PCB-GND, and (2) mounted in a socket without conducting e-pad connection. The emission of a soldered TC1782 without conducting e-pad connection will stay between any two measurement results provided within one row of the result table.

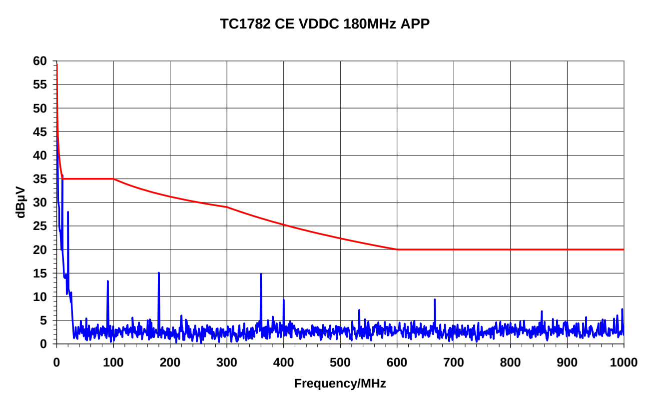

Figure 47 TC1782; soldered; e-Pad; Application; VDD conducted; 180 MHz

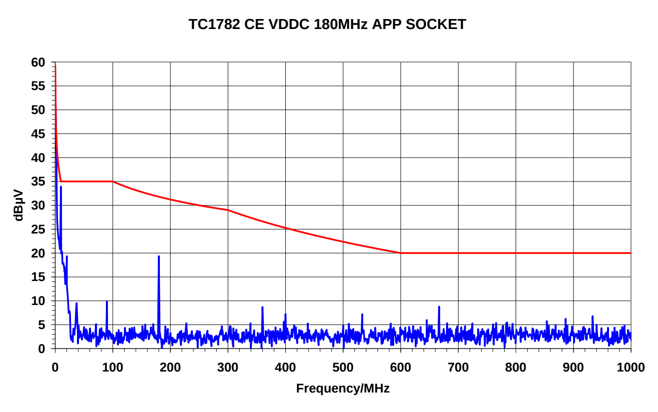

Figure 48 TC1782; Socket; no e-Pad; Application; VDD conducted; 180 MHz

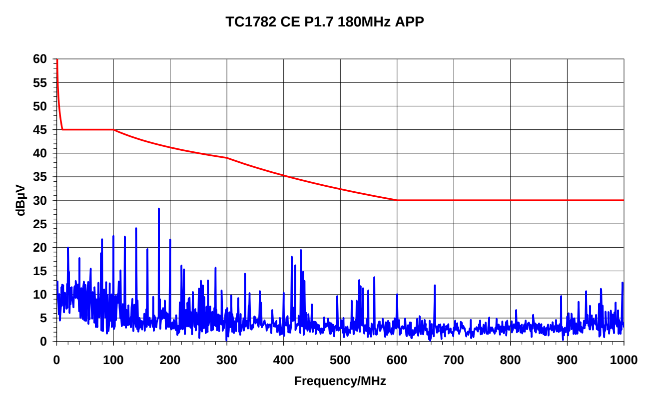

Figure 49 TC1782; soldered; e-Pad; Application; P1.7 conducted; 180 MHz

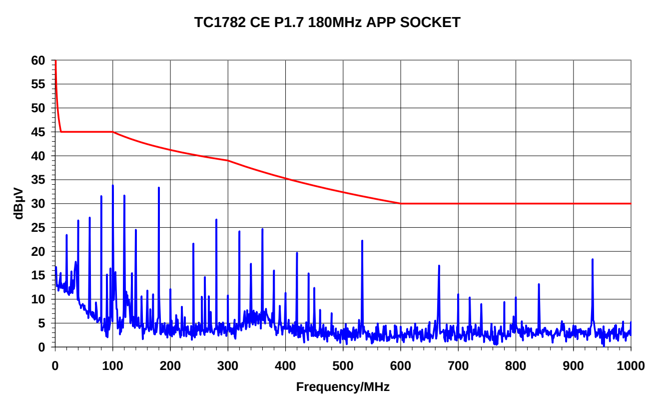

Figure 50 TC1782; Socket; no e-Pad; Application; P1.7 conducted; 180 MHz

8.2 Emission influence from scaled pad drivers

For emission measurements, so called "application-typical" microcontroller configurations as described in chapter 5 are used. All function units are active, but the port pin drivers do not use their their strongest default settings after reset. Instead, weaker driver settings are configured. The actual driver scaling per pin depends on the data rate this pin must provide with good signal integrity. According Table 3 in chapter 5, none of the pads are using driver strengths stronger than "strong-soft". The used "weak", "medium" and "strong-soft" settings keep the pad switching emission low and should be preferred in any application. Fast data rates recommend for strong driver settings, but even here, the microcontrollers provide several sub-settings, depending on the microcontroller family. Fig. 47 provides a generic overview of emission reduction potential when weaker pad driver settings are used. The strongest driver ("strong-sharp", default after reset) serves as the 0dB reference line. Any pad driver scaling other than "strong-sharp" leads to significant emission reduction up to 30dB ("weak"). Please note that driver settings "strong-sharp-minus", "strong-medium-minus" and "strong-slow" are only available in the TC1782. In addition, the emission reduction numbers in dB should be treated as rough reference. The real numbers may differ. For details, please refer to the Infineon Application Notes [1] [2].

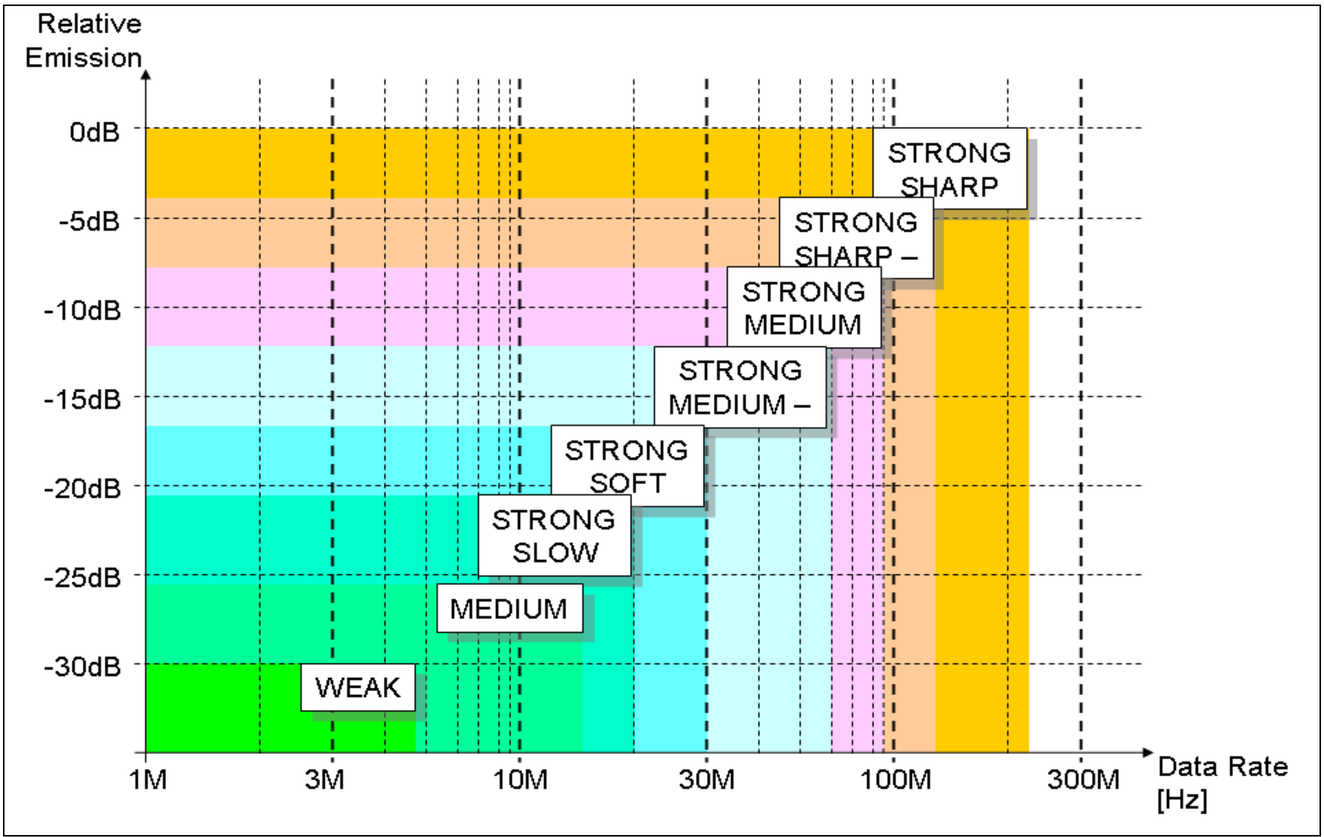

Figure 51 Emission reduction by pad driver settings for VDDP = 3.3 V and Cload = 22 pF at 25°C

Infineon strongly recommends to use the pad driver scaling feature in order to reduce electromagnetic emission. The lists of pin-wise driver settings for the microcontrollers under test are given in the microcontroller-specific full electromagnetic emission reports which are available upon request.

If many port pins are operated using strong pad driver settings, the electromagnetic emission behavior may be worse than shown in the measurement diagrams within this document.

The following conducted emission results have been obtained from TC1782. Emission reduction depends on the pin and the signal integrity constraints. Nevertheless, the following Fig. 40 and 41 indicate up to 10 dB emission reduction on VDDP and up to 20 dB emission reduction on P0.9.

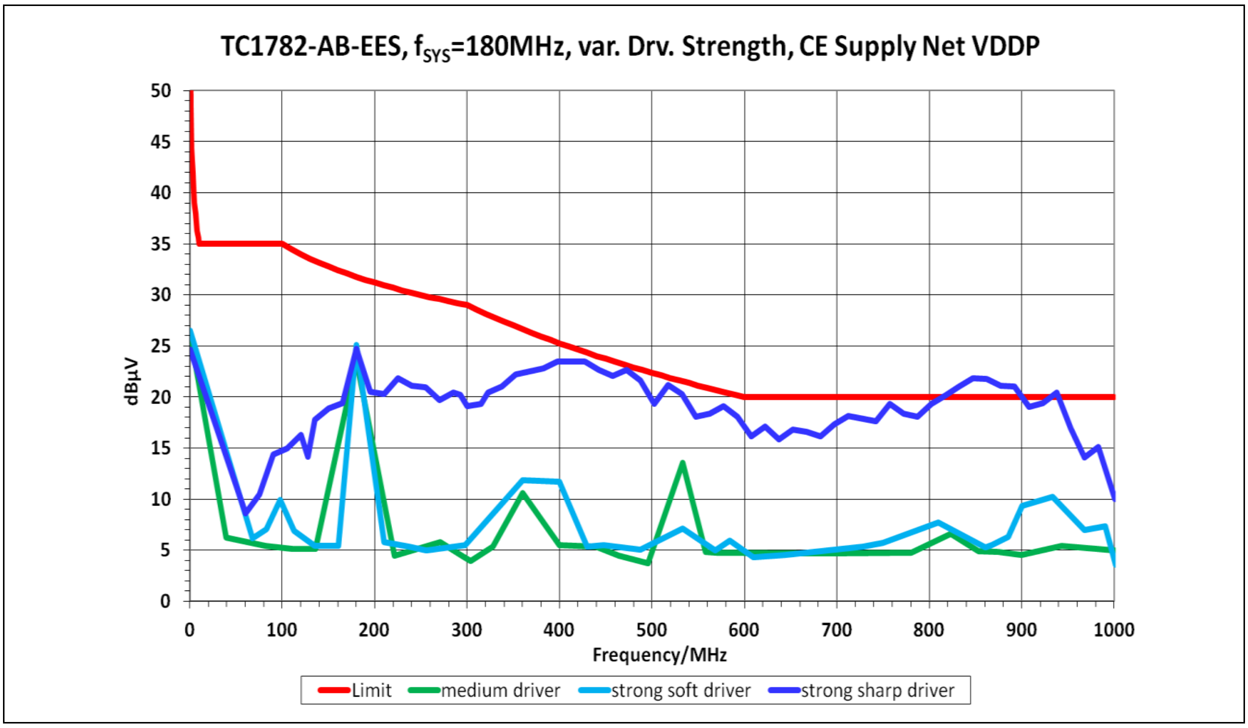

Figure 52 TC1793; Application pattern; 270 MHz; best-case I/O conducted

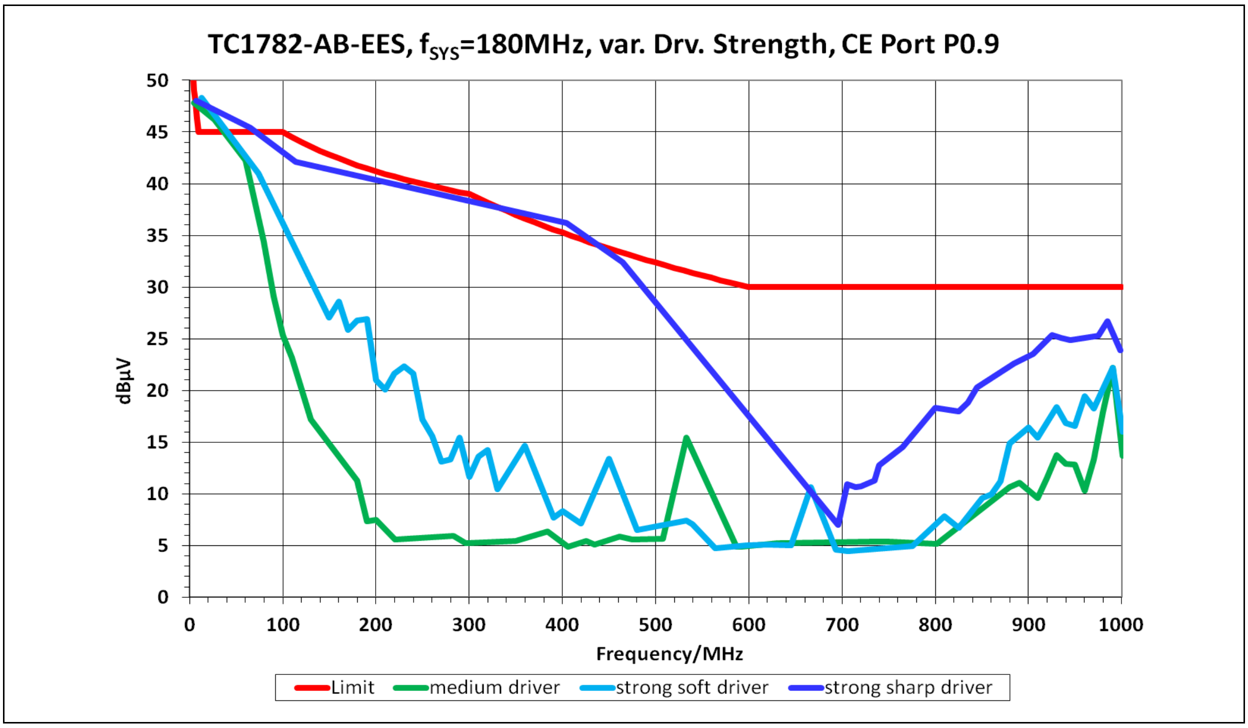

Figure 53 TC1793; Application pattern; 270 MHz; best-case I/O conducted

8.3 Emission influence from clock frequency modulation

Unmodulated clocks keep their energy in the narrow-band peaks along the clock harmonic frequencies. Clock frequency modulation leads to a distribution of the same energy into lower and upper side-bands of those harmonics. Thus the peak energy of the clock harmonics decreases according to the modulation amplitude. Unfortunately, standard triangular frequency modulation causes significant time shifts of the clock edges towards an unmodulated clock with same frequency. For that reason, this clocking technology cannot be applied to asynchronous data interfaces. Infineon developed an advanced clock modulation technique which offers similar emission reduction together with a strict limitation of clock edge shift, i.e. the resulting time interval error TIE stays very low. Details can be found in [1]. Therefore, the FMPLL feature of the AudoMax microcontrollers TC1791, TC1793 and TC1798 allows proper operation of asynchronous data communication like CAN while benefitting from up to 20 dB emission reduction, see Fig. 54-59.

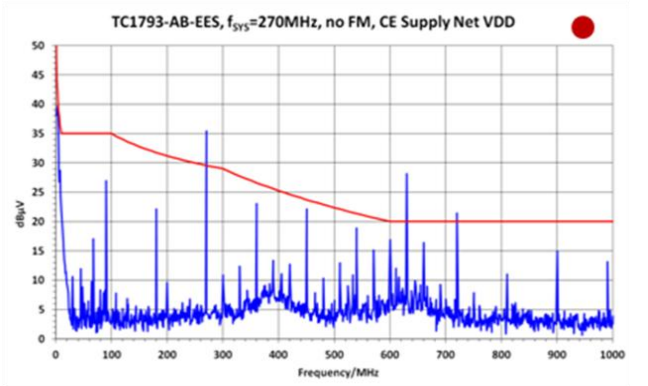

Figure 54 TC1793; VDD conducted; FMPLL off

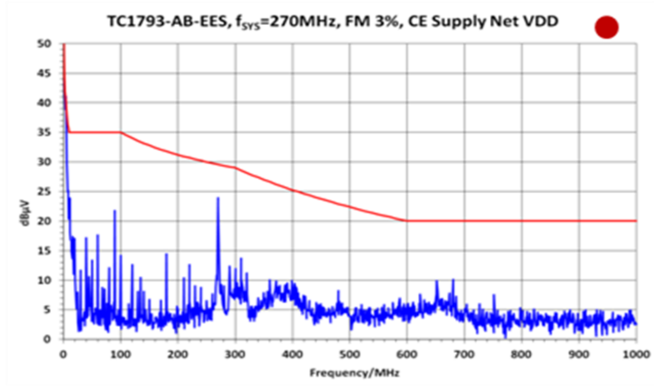

Figure 55 TC1793; VDD conducted; FMPLL on

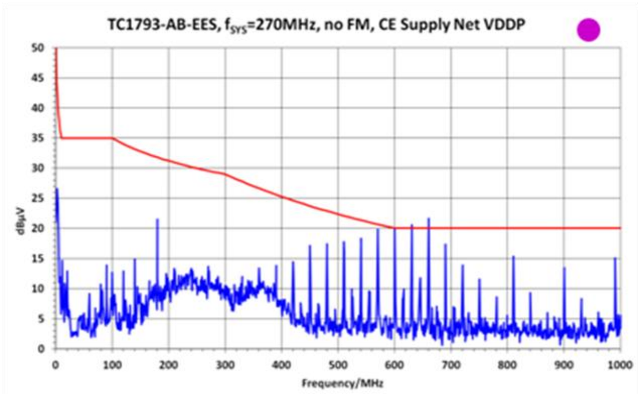

Figure 56 TC1793; VDDP conducted; FMPLL off

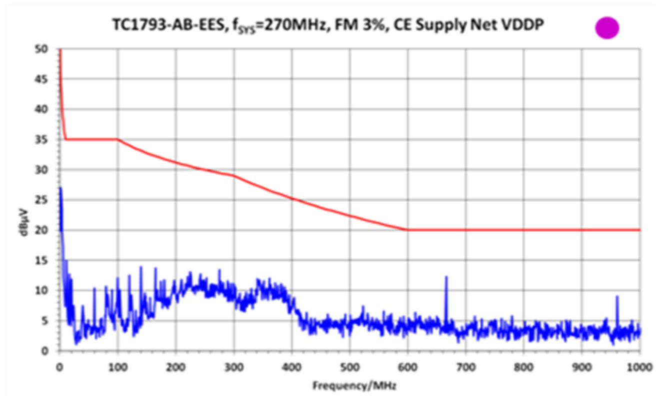

Figure 57 TC1793; VDDP conducted; FMPLL on

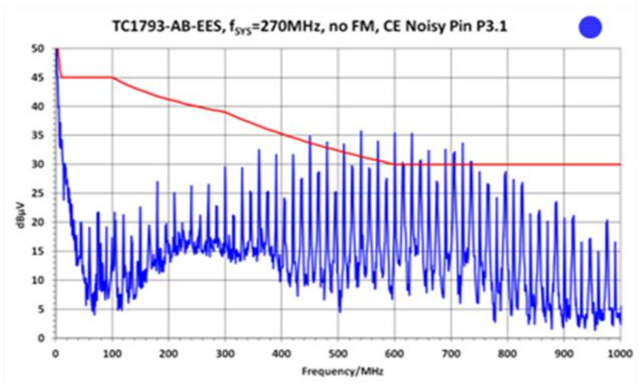

Figure 58 TC1793; P3.1 conducted; FMPLL off

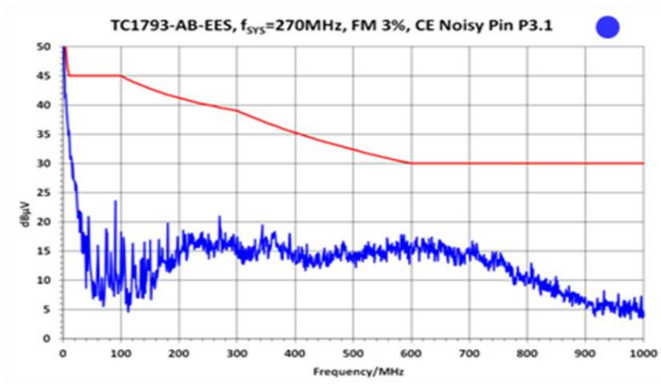

Figure 59 TC1793; P3.1 conducted; FMPLL on

9 References

These documents can be downloaded from the Infineon microcontroller internet pages www.infineon.com

[1] Application Note AP32185 "Frequency-modulated PLL"; Parameters, effects, programming

[2] Application Note AP32146 "Scalable pads in 90nm microcontrollers"; Timing and emission

[3] Application Note AP24026 "General EMC guidelines for PCB design"

[4] Application Note AP32181 "EMC guidelines for PCB design – TC172x"

[5] Application Note AP32145 "EMC guidelines for PCB design – TC1782"

[6] Application Note AP32161 "EMC guidelines for PCB design – TC1784"

[7] Application Note AP32162 "EMC guidelines for PCB design – TC1791"

[8] Application Note AP32163 "EMC guidelines for PCB design – TC1793"

[9] Application Note AP32164 "EMC guidelines for PCB design – TC1798"

The BISS test specification can be downloaded from http://www.zvei.org/IC_EMC_Test_Specification

[10] Generic IC EMC Test Specification ("BISS paper"),
open copyright by Robert Bosch GmbH, Infineon Technologies AG, Continental AG;

Detailed electromagnetic emission and immunity test reports for all AudoMax microcontrollers are available on request.

10 Abbreviations

BGA	Ball-grid array IC package
BISS	Bosch/Continental/Infineon IC EMC Test Specification
CPU	Central processing unit
EBU	External bus unit (e.g. external flash or SRAM communication)
EMC	Electromagnetic compatibility
EME	Electromagnetic emission
e-Pad	Exposed die pad
EVR	Embedded voltage regulator
FMPLL	Frequency-modulated phase-locked loop
LDO	Linear voltage regulator output
PCB	Printed circuit board
PLL	Phase-locked loop (e.g. system clock generation)
QFP	Quad flat-pack lead-frame IC package
TIE	Time interval error

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