TriCore™ Family

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Migration guide for TriCore™ based Microcontrollers

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Device1

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Previous Version: none

Page	Subjects (major changes since last revision)

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1 Preface

The AUDO Family with TriCore™ is a unified, superscalar, 32-bit microcontroller architecture optimized for embedded real-time applications. Compatibility, scalability, and maximum re-use within the family result in a broad portfolio of TriCore™-based products and features, addressing advanced performance in automotive power train, safety and industrial applications.

Based on the industry leading TriCore™ high performance microcontroller core running at up to 300MHz, the AUDO Family offers the best of three worlds: Reduced Instruction Set Computer (RISC), Complex Instruction Set Computer (CISC) and Digital Signal Processing (DSP) functionality.

While Infineon strives to continuously improve the TriCore™ based microcontrollers we respect the efforts our customers put into the product development both in terms of software and hardware. Infineon therefore provides a broad product portfolio of devices within one family, allowing engineers to choose the right combination of features meeting their requirements. In addition Infineon provides a migration path to allow an easy transition to the next device generation.

Software that has been developed on existing controllers can generally be reused on a new core. All members of the AUDO family are binary compatible and share the same development tools. Since in most cases the software requires changes to accomplish for newly introduced or improved peripherals, it is recommended to rebuild the code in order to take full advantage from improvements in the core revision.

Infineon offers microcontrollers for both the automotive as well as the industrial environment. The naming convention was slightly changed with the AUDO MAX family in order to reflect the availability of FlexRay.

- TC11xx, TC17xx**N** Industrial and Multimarket devices
- TC17xx, TC17xx**F** Automotive devices

While several devices are electrically compatible, they are specified and tested differently, e.g. regarding the temperature range. In addition the automotive devices are qualified according to AEC-Q100.

Based on the technology node the TriCore™ microcontrollers are grouped into families where the individual devices share a common basic structure including the core revision, the bus structure as well as the peripheral feature set. The following table shows the devices per family for industrial and automotive applications.

The tables in the following paragraphs only give the base variants in each family. Please note that there might be several variants offered that differ in terms of frequency, memory sizes and/or temperature range.

Table 1 TriCore™ based microcontrollers

AUDO NG	TC1164 TC1166	TC1762 TC1766 TC1796
AUDO FUTURE	TC1736 TC1167 TC1197	 TC1767 TC1797
AUDO MAX	TC1724N (no FlexRay) TC1728N TC1782N TC1784N TC1793N TC1798N	TC1724F (with FlexRay) TC1728N TC1782F TC1784F TC1793F TC1798F

Typically devices from a newer family implement a lot of improvements both in terms of the core as well as in the peripherals. This document can only list the major items that changed between families.

Attention: For further details please refer to the Data Sheets and User Manuals, respectively. In case of any inconsistency Data Sheet and User Manual take precedence.

2 AUDO NG to AUDO FUTURE

2.1 Migration Paths

The following migration possibilities exist:

AUDO NG	AUDO FUTURE	
TC1166 / TC1766	TC1167 / TC1767	QFP-176, performance upgrade
TC1796	TC1197 / TC1797	BGA-416, performance upgrade

2.2 TC1166 / TC1766 vs. TC1167 / TC1767

2.2.1 Feature Comparison

		TC1166 & TC1766	TC1167 & TC1767
Core	TC Version	1.3	1.3.1
	Frequency (max.)	80 MHz	133 MHz
Flash	Program Flash	1.5 MB	1.0 MB (TC1767: 2.0 MB)
	Data Flash	32 KB	64 KB
SRAM	Σ (w/o PCP, Cache)	88 KB	96 KB
	PMI	24 KB	24 KB
	DMI	56 KB	72 KB
	Overlay	8 KB	8 KB
PCP	Frequency (max.)	80 MHz	133 MHz
	Code Memory	12 KB	16 KB
	Parameter Memory	8 KB	8 KB
DMA	Channels	8	8
ADC	Σ Analog Inputs	32	32
	ADC Modules x Channels	1 x 32	2 x 16
	FADC Channels	2	4
Timer	Σ Timed IO (max.)	80	80
	GPTA	1	1
	LTC	-	1
Interfaces	CAN nodes / objects	2 / 64	2 / 64
	SSC / ASC	2 / 2	2 / 2
	MLI / MSC	2 / 1	1 / 1
Package		LQFP 176	LQFP 176
Temperature (ambient)		-40 °C ... +85 °C	-40 °C ... +85 (125) °C

2.2.2 Design Compatibility

Since the basic electrical parameters as well as the positions of most pins remained unchanged, a combined layout for the AUDO NG and AUDO FUTURE devices is feasible.

Care must be given to changes due to added or changed functionality in the newer devices.

The power supply requirements are almost identical; in general a PSU designed for the TC1166 can be used without changes. Due to improvements in the core design, the maximum required supply current is identical, even with the TC1167 running at a significantly higher clock rate.

The TC1167 implements a 5V ADC which can also be used with 3.3V. Still the electrical parameters of the external ADC circuitry should be checked.

The following tables list the changes and additions starting with pin1.

Table 2 Changed/Removed Functionality

Pin	TC1166 & TC1766	TC1167 & TC1767
1...8	OCDS2	OCDS2 removed
13...19	OCDS2	OCDS2 removed
20	IO (P5.15)	V_{DDP}
21	NC	V_{DD}
22	V_{SSAF}	V_{SS}
54	V_{DDM} 3.3V max.	V_{DDM} 5.0V max.
86..88, 90	IO & HWCFG[3:0]	HWCFG[3:0] removed
89	NC	V_{DD}
91	IO (P1.0)	V_{DDP}
92	IO (P1.1)	V_{SS}
145...148	IO (P0.0...0.3)	IO (P0.0...0.3) & HWCFG0...3
166, 167, 173, 174	IO (P0.4...0.7)	IO (P0.4...0.7) & HWCFG4...7
145...152, 166...169, 173...176	IO & SWCFG[15:0]	SWCFG[15:0] removed

Table 3 Added Functionality

Pin	TC1166 & TC1766	TC1167 & TC1767
9	TRCLK for OCDS2	additional IO (P5.15, pin 20 of TC1x66)
111...115	JTAG only	additional DAP
116...119	JTAG only	additional IO
128...138	SSC/ASC only	additional timed IO (GPTA0)
142...144	ASC/CAN only	additional timed IO (GPTA0)
156...159	MSC0 only	additional IO & timed IO (GPTA0)
71...73, 76...80, 93, 107..110, 116, 119, 156...159, 161...163, 165		additional timed IO (LTCA2)

2.2.3 Features, Peripherals & Software Compatibility

For the TC1167 the same tool chains can be used as for the AUDO NG devices.

The core revision was updated from 1.3 to 1.3.1. Aside of the increase in maximum speed the access to data and code including branch prediction has been improved. In combination with the increased clock rate the performance increase can be in the range of 60-70 %.

The clock rate of the PCP has been increased from 80MHz to 133MHz and the code memory increased. For PCP frequencies exceeding 80 MHz, 2:1 mode vs. the FPI bus has to be enabled.

The TC1167 provides an improved memory system providing faster access times as well as more flexibility. The SRAM in the DMI can be used as data RAM as well as data cache. For both PMI and DMI the split between RAM and CACHE can be software configured. The TC1167 and TC1767 provide more data flash and the TC1767 a bigger amount of program flash.

OCDS2 (Program Trace) is no more supported - please use the Emulation device.

Below is a description of the more important changes in the peripherals.

The TC1167 implements two independent 5V ADC modules. These can also be used with 3.3V and additionally use an alternative reference voltage applied at channel 0.

The General Purpose Timer Array (GPTA v5) in the TC1167 provides an additional block of 32 Local Timer Cells. The output multiplexer allows a much more flexible routing to I/O lines, output lines, clock inputs, other on-chip peripherals and other GPTA cells. The local and global bypass features of the LTC have been improved allowing a group of Local Timer Cells (LTCs) to drive a specific output pin or to perform coherent cell update.

The PLL has been changed to allow easier reprogramming.

The reset system now offers an additional system reset. For several reset sources (e.g. WDT, ESRx, and SW) the type of reset generated can be configured.

The CAN register mapping has been changed in order to become common for all existing and future of AUDO Future derivatives.

The serial interfaces ASC/SSC implement some bug fixes and improvements in configuration flexibility.

For the SSC interfaces the flexibility of the IO routing has been significantly enhanced.

2.3 TC1796 vs. TC1197 / TC1797

2.3.1 Feature Comparison

		TC1796	TC1197 & TC1797
Core	TC Version	1.3	1.3.1
	Frequency (max.)	150 MHz	180 MHz
Flash	Program Flash	2.0 MB	2.0 MB / 4.0 MB
	Data Flash	128 KB	64 KB
SRAM	Σ (w/o PCP, Cache)	208 KB	176 KB
	PMI	64 KB	40 KB
	DMI	64 KB	128 KB
	DMU	80 KB	-
	Overlay	-	8 KB
PCP	Frequency (max.)	75 MHz	180 MHz
	Code Memory	32 KB	32 KB
	Parameter Memory	16KB	16KB
DMA	Channels	16	16
ADC	Σ Analog Inputs	44	44
	ADC Modules / Channels	2 x 16	3 x 16
	FADC Channels	4	4
Timer	Σ Timed IO (max.)	112	112
	GPTA	2	2
	LTC	1 (64 cells)	1 (32 cells)
Interfaces	FlexRay	-	1 (TC1797 only)
	CAN nodes / objects	4 / 128	4 / 128
	SSC / ASC	2 / 2	2 / 2
	MLI / MSC	2 / 2	2 / 2
	EBU	1	1
Package		BGA-416	BGA-416
Temperature (ambient)		-40 °C ... +125 °C	-40 °C ... +125 °C

2.3.2 Design Compatibility

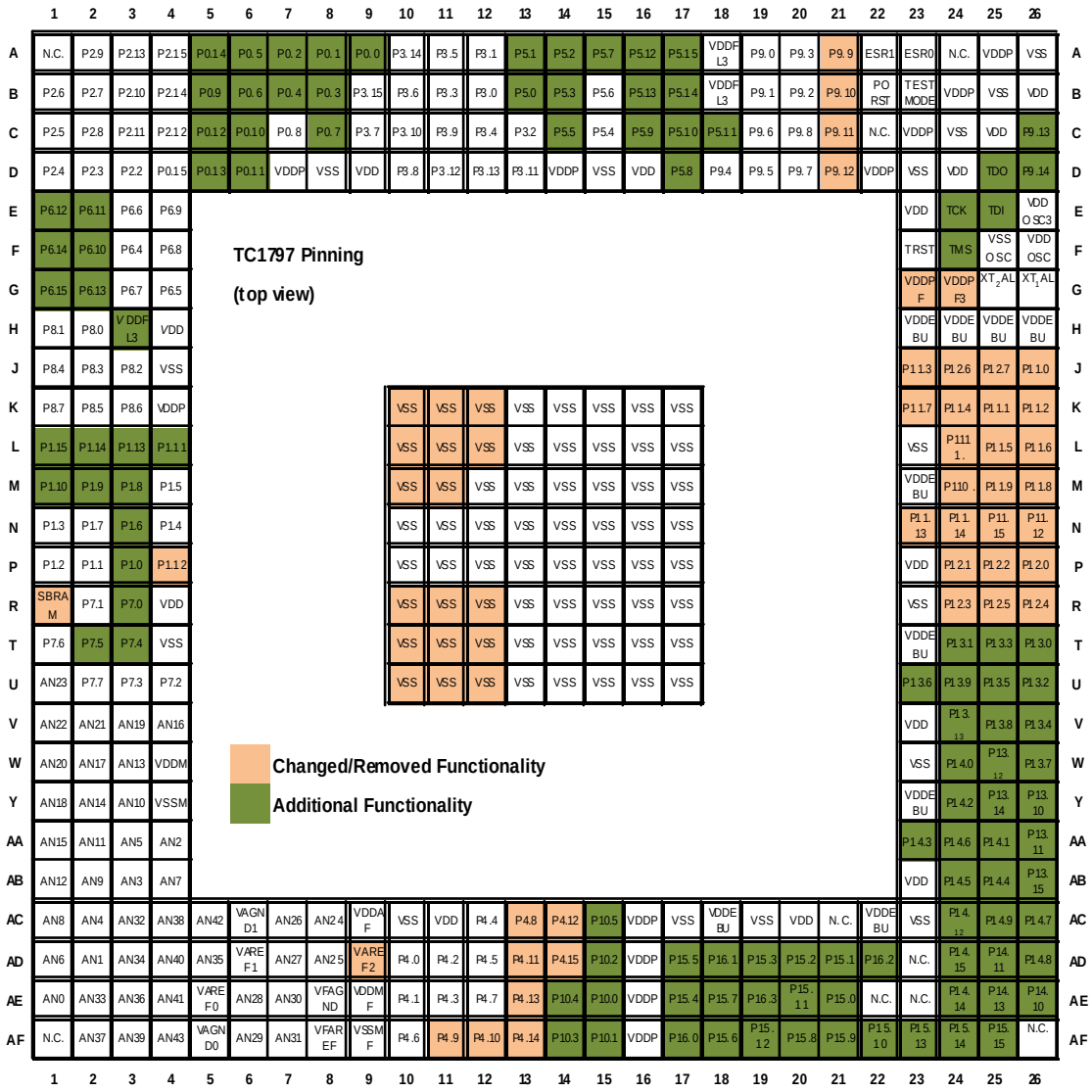
Since the basic electrical parameters as well as the positions of most balls remained unchanged, a combined layout for the AUDO NG and AUDO FUTURE devices is feasible.

Care must be given to changes due to added or changed functionality in the newer devices.

The power supply requirements are almost identical; in general a PSU designed for the TC1796 can be used without changes. Due to improvements in the core design, the maximum required supply current for the TC1197 is actually lower, even with the TC1197 running at a significantly higher clock rate.

The TC1197 implements three 5V ADCs which can also be used with 3.3V. Still the electrical parameters of the external ADC circuitry should be checked.

Figure 1 Ball out changes on TC1797 compared to TC1796



The following tables list the changes and additions clockwise starting with the top left corner.

Table 4 Changed/Removed Functionality

Ball	TC1796	TC1197 & TC1797
A21	P10.0	P9.9
B21	P10.1	P9.10
C21	P10.2	P9.11
D21	P10.3	P9.12
G23	NC	V_{DDPF}
G24	TSTRES	V_{DDPF3}
J24...R26, J23, K23, N23 (24 balls)	A[23:0] (aligned or non-aligned address mode)	address pins are shifted by two LSBs (aligned address mode only) additional IO (P11.x / P12.x)
AC13, AC14, AD13, AD14, AE13, AF11...13	LTCA2 IN/OUT 32..39	LTCA2 IN/OUT 0...7 (LTCA2 has only 32 cells)
AD9	V_{SSAF}	V_{AREF2}
R1	$V_{DDSBRAM}$	NC
P4	SYSCLK	EXTCLK0
K10...U12 (17 balls)	TR[15:0], TRCLK	V_{SS} (OCDS2 removed)

Table 5 Additional Functionality

Ball	TC1796	TC1197 & TC1797
A5, B5, C5, C6, D5, D6	IO	additional FlexRay (TC1797 only)
A6...9, B6...8, C8	IO	additional timed IO (GPTA0/1)
A13...17, B13, B14, B16, B17, C14, C16...18, D17	IO	additional timed IO (GPTA0/1)
C26	BRKIN	additional IO (P9.13)
D26	BRKOUT	additional IO (P9.14)
D25, E24, E25, F24	JTAG only	additional DAP
T24...AE26, U23, AA23 (32 balls)	D[31:0]	additional IO (P13.x / P14.x) additional timed IO (GPTA0/1)
AD17...22, AE17...21, AF17...25	EBU control	additional IO (P15.x / P16.x)
AC15, AD15, AE14, AE15, AF14, AF15	SSC0	additional IO (P10.x)
T2, T3, R3	IO	additional AD2EMUX0/1
P3	IO	additional EXTCLK1
N3	IO/MLI	additional SLSO10
M1...3, L1...4	IO/MLI	additional timed IO (GPTA0/1)
H3	NC	V_{DDFL3}
E1, E2, F1, F2, G1, G2	IO/ASC/CAN	additional FlexRay (TC1797 only)

2.3.3 Features, Peripherals & Software Compatibility

For the TC1197 the same tool chains can be used as for the AUDO NG devices.

The core revision was updated from 1.3 to 1.3.1. Aside of the increase in maximum speed the access to data and code including branch prediction has been improved. In conjunction with the increased clock rate the performance increase can be in the range of 30-50 %.

The clock rate of the PCP has been increased from 75MHz to 180MHz and the code memory increased. For PCP frequencies exceeding 90 MHz, 2:1 mode vs. the FPI bus has to be enabled.

The TC1197 provides an improved memory system providing faster access times as well as more flexibility. The SRAM in the DMI can be used as data RAM as well as data cache. For both PMI and DMI the split between RAM and CACHE can be software configured. The TC1197 and TC1797 provide 64KB of data flash (TC1796: 128KB) and there are devices available with up to 4MB of program flash.

OCDS2 (Program Trace) is no more supported please use the Emulation device.

Below is a description of the more important changes in the peripherals.

The TC1197 implements three independent 5V ADC modules. These can also be used with 3.3V and additionally use an alternative reference voltage applied at channel 0.

The number of cells in the LTCA block of the General Purpose Timer Arrays (GPTA v5) has been downsized to 32 Local Timer Cells. The output multiplexer allows a much more flexible routing to I/O lines, output lines, clock inputs, other on-chip peripherals and other GPTA cells. The local and global bypass features of the LTC have been improved allowing a group of Local Timer Cells (LTCs) to drive a specific output pin or to perform coherent cell update.

The PLL has been changed to allow easier reprogramming.

The reset system now offers an additional system reset. For several reset sources (e.g. WDT, ESRx, and SW) the type of reset generated can be configured.

While the TC1197 provides the same number of CAN nodes and message objects, the CAN register mapping has been changed in order to become common for all existing and future of AUDO FUTURE derivatives.

The serial interfaces ASC/SSC implement some bug fixes and improvements in configuration flexibility.

For the SSC interfaces the flexibility of the IO routing has been significantly enhanced.

3 AUDO FUTURE to AUDO MAX

Attention: The AUDO MAX family of devices is not yet fully released. Therefore all information given in the following paragraphs should be considered preliminary!

3.1 Migration Paths

The following migration possibilities exist:

AUDO FUTURE	AUDO MAX	
TC1736	*TC1724N / TC1724F*	*QFP-144, cost improvement [1])*
TC1167 / TC1767	TC1728N	QFP-176, cost improvement
	TC1782N / TC1782F	QFP-176, performance upgrade
TC1197 / TC1797	TC1793N / TC1793F	BGA-416, performance upgrade

[1])...limited feature compatibility, not pin compatible

3.2 TC1736 vs. TC1724N / TC1724F

3.2.1 Feature Comparison

		TC1736	TC1724N & TC1724F
Core	TC Version	1.3.1	1.3.1
	Frequency (max.)	80 MHz	133 MHz
Flash	Program Flash	1.0 MB	1.5 MB
	Data Flash	32 KB	64 KB
SRAM	Σ (w/o PCP, Cache)	48 KB	152 KB
	PMI	8 KB	24 KB
	DMI	36 KB	120 KB
	Overlay	4 KB	8 KB
PCP	Frequency (max.)	-	133 MHz
	Code Memory	-	24 KB
	Parameter Memory	-	8 KB
DMA	Channels	8	16
ADC	Σ Analog Inputs	24	28
	ADC Modules x Channels	2 / 32	2 / 40
	FADC Channels	2	2
Timer	Σ Timed IO (max.)	53	77
	GPTA	1	1
	GPT12	-	2
	CCU6	-	1
Interfaces	FlexRay	-	1 (TC1724**F** only)
	CAN nodes / objects	2 / 64	3 / 64
	SSC / ASC	2 / 2	4 / 2
	MLI / MSC	1 / 1	1 / 1
Package		LQFP 144	LQFP 144 (ePAD)
Temperature (ambient)		-40 °C ... +125 °C	-40 °C ... +125 °C

3.2.2 Design Compatibility

While the TC1724 is the predecessor of the TC1736 in terms of the applications targeted it has not been designed to be a pin compatible replacement. So the following description is given to assist customers that are already familiar with the TC1736 to create or change a design for the TC1724.

The new AUDO MAX family of devices requires a core supply of 1.3V vs. 1.5V for the AUDO FUTURE devices.

The new TC1724 has an integrated voltage regulator (EVR), which can be used to create a single supply design. The device features an internal supply watchdog end there is no need for external power sequencing.

For the single supply scheme special care must be given to the power dissipation of the total device. If the EVR is supplied with 5V the system frequency is limited to 80MHz. In order to reach the full 133MHZ, an additional external pass device for the 3.3V rail has to be added.

If the 5V is not required the EVR can be fed with 3.3V and there is no need for an external pass device.

The power supply currents at a clock of 80MHz are very similar to the TC1736. If the TC1724 is run at 133MHz the currents for the core supply are higher. Since the ADC and the FADC at the TC1724 use a common supply, the current required is the sum of the individual currents at the TC1736.

A PSU originally designed for the TC1736 has to be checked accordingly.

The TC1724 uses an LQFP package with exposed pad to reduce the thermal resistance. Utilizing the exposed pad is important namely if the internal voltage regulator is used.

The number of power supply pins has been significantly reduced, allowing now for 95 digital IO pins vs. 70 at the TC1736. If the TC1724 is used in a layout originally designed for the TC1736 care must be given to not pull these IO pins low which would shorten the respective power supply.

3.2.3 Features, Peripherals & Software Compatibility

For the TC1724 the same tool chains can be used as for the AUDO FUTURE devices, namely since the core revision and the memory configuration remains the same.

The TC1724 provides significantly more SRAM for data – 152KB vs. 48KB.

In addition both the SRAM in DMI and PMI can be ECC protected.

The TC1724 has an additional PCP (Peripheral Co Processor) which can run at the full 133MHz and has 24KB of local code memory and 8KB parameter memory.

The number of DMA channels has been increased to 16 in two DMA blocks.

The TC1728 provides several measures targeted at safety and security applications. Amongst others these measures include error detection on the local bus, a bus monitor unit (BMU) a memory checker module and a Flexible CRC Engine (FCE).

The Flexible CRC Engine (FCE) provides a parallel implementation of one or more Cyclic Redundancy Code (CRC) algorithms. The standard CRC polynomial implemented in the FCE module is the IEEE 802.3 Ethernet CRC32. The FCE is meant to be used as a hardware acceleration engine for software applications or operating systems services using CRC signatures.

Below is a description of the more important differences regarding the peripheral modules.

The TC1724 can use a peripheral clock of 110MHz instead of 80MHz, allowing several peripherals like CAN, ASC, SSC, MSC, MLI and the timers to achieve higher data rates and timer resolution. Please note that the core and bus clock have to have a ratio of 1:1 or 1:2, so if the peripheral clock of 110MHz is used the core clock is also limited to 110MHz.

The TC1724 includes four high-speed synchronous serial interfaces (SSC) instead of two.

The TC1724**F** incorporates an E-Ray IP-module with two channels performing communication according to the FlexRay™ 1) protocol specification v2.1.

The MultiCAN module implemented provides three independent CAN nodes instead of two. The number of available message objects is 64.

In addition to the GPTA the TC1724 incorporates several additional timer units: one Capture Compare Units CCU6 and two general purpose timer units (GPT12).

The CCU6 provide two independent timers (T12, T13), which can be used for PWM generation, especially for AC-motor control or power conversion stages. Additionally special control modes for block commutation and multi-phase machines are supported.

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. Its functionality includes enhanced incremental interface modes and clock prescaler support.

The two ADC modules now provide 40 input channels whereof max. 28 are available on input pins. All ADC input channels now include broken wire detection. The maximum ADC clock has been increased from 10MHz to 18MHz.

The FADC provides a significantly shorter conversion time namely if the increased peripheral clock of 110MHz is used.

3.3 TC1167 / TC1767 vs. TC1728N

3.3.1 Feature Comparison

		TC1167 & TC1767	TC1728N
Core	TC Version	1.3.1	1.3.1
	Frequency (max.)	133 MHz	133 MHz
Flash	Program Flash	1.0 MB (TC1767: 2.0 MB)	1.5 MB
	Data Flash	64 KB	64 KB
SRAM	Σ (w/o PCP, Cache)	96 KB	152 KB
	PMI	24 KB	24 KB
	DMI	72 KB	120 KB
	Overlay	8 KB	8 KB
PCP	Frequency (max.)	133 MHz	133 MHz
	Code Memory	16 KB	24 KB
	Parameter Memory	8 KB	8 KB
DMA	Channels	8	16
ADC	Σ Analog Inputs	32	36
	ADC Modules / Channels	2 / 32	2 / 40
	FADC Channels	4	2
Timer	Σ Timed IO (max.)	80	93
	GPTA	1	1
	LTCA / cells	1 / 32	-
	GPT12	-	2
	CCU6	-	1
Interfaces	FlexRay	-	-
	CAN nodes / objects	2 / 64	3 / 64
	SSC / ASC	2 / 2	4 / 2
	MLI / MSC	1 / 1	1 / 1
Power Supply		3 supplies	single supply EVR
Package		LQFP 176	LQFP 176 (ePAD)
Temperature (ambient)		-40 °C ... +85 (125) °C	-40 °C ... +125 °C

3.3.2 Design Compatibility

The biggest changes affecting the hardware design are the supply concept and the use of an LQFP-176 with exposed pad.

The new AUDO MAX family of devices requires a core supply of 1.3V vs. 1.5V for the AUDO FUTURE devices.

The new TC1728 has an integrated voltage regulator (EVR), which can be used to create a single supply design. The device features an internal supply watchdog end there is no need for external power sequencing.

For the single supply scheme special care must be given to the power dissipation of the total device. If the EVR is supplied with 5V the system frequency is limited to 80MHz. In order to reach the full 133MHZ, an additional external pass device for the 3.3V rail has to be added.

If the 5V is not required the EVR can be fed with 3.3V and there is no need for an external pass device.

Overall the power supply currents are very similar to the TC1167. Since the ADC and the FADC at the TC1728 use a common supply, the current required is the sum of the individual currents at the TC1167.

Together with the changed core voltage this has to be taken into account if a PSU designed for the TC1167 should be re-used.

The TC1728 uses an LQFP package with exposed pad to reduce the thermal resistance. Utilizing the exposed pad is important namely if the internal voltage regulator is used.

The number of supply pins has been reduced to gain on IO capability. If the TC1728 is used in a layout designed for the TC1167 care must be given to not pull these IO pins low which would shorten the respective power supply.

Due to a number of peripheral modules being added it is impractical to list all pins with changed functionality. Therefore the table below only lists pins which changed from being power supply to IO.

Table 6 Changed Functionality from power supply to IO

Pin	TC1167 & TC1767	TC1728N
11	V_{DDP}	IO (P9.7) &, GPTA, CCU6
12	V_{SS}	IO (P9.8) & GPTA, CCU6
23...26	V_{DDAF} V_{DDMF} V_{SSMF} V_{FAREF}	IO (P10.0...P10.3) & SSC
82...85	V_{SS} V_{DDMF} V_{SSMF} V_{FAREF}	IO (P8.5...P8.8) & GPTA, CCU6
89	V_{DD}	IO (P8.9) & GPTA, SSC
99	V_{DD}	IO (P1.4) & GPTA, CCU6
100	V_{DDP}	IO (P8.12) & GPTA
123...125	V_{DD} V_{DDP} V_{SS}	IO (P8.x) & GPTA, CCU6, SSC
139...141	V_{DDP} V_{SS} V_{DDFL3}	IO (P8.x) & GPTA, CCU6, GPT, SSC
170...172	V_{DD} V_{DDP} V_{SS}	IO (P9.4...P9.2) & GPTA, CCU6

3.3.3 Features, Peripherals & Software Compatibility

For the TC1728 the same tool chains can be used as for the AUDO FUTURE devices, namely since the core revision and the memory configuration remains the same.

The TC1728 provides significantly more SRAM for data – 120KB vs. 72KB.

In addition both the SRAM in DMI and PMI can be ECC protected.

The PCP has access to 24KB of code memory instead of 16KB.

The number of DMA channels has been increased to 16 in two DMA blocks.

The TC1728 provides several measures targeted at safety and security applications. These measures e.g. include error detection on the local bus, a bus monitor unit (BMU) a memory checker module and a Flexible CRC Engine (FCE).

The FCE is meant to be used as a hardware acceleration engine for software applications or operating systems services using CRC signatures.

Below is a description of the more important changes in the peripherals.

The TC1728 can use a peripheral clock of 110MHz instead of 80MHz, allowing several peripherals like CAN, ASC, SSC, MSC, MLI and the timers to achieve higher data rates and timer resolution. Please note that the core and bus clock have to have a ration of 1:1 or 1:2, so if the peripheral clock of 110MHz is used the core clock is also limited to 110MHz.

The TC1728 includes four high-speed synchronous serial interfaces (SSC) instead of two.

The MultiCAN module implemented provides three independent CAN nodes instead of two. The number of available message objects is 64.

The separate block of 32 local timer cells (LTCA) has been removed from the GPTA.

The TC1728 incorporate several additional timer units: one Capture Compare Units CCU6 and two general purpose timer units (GPT12).

The CCU6 provide two independent timers (T12, T13), which can be used for PWM generation, especially for AC-motor control or power conversion stages. Additionally special control modes for block commutation and multi-phase machines are supported.

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. Its functionality includes enhanced incremental interface modes and clock prescaler support.

The two ADC modules now provide 40 input channels whereof max. 36 are available on input pins. All ADC input channels now include broken wire detection. The maximum ADC clock has been increased from 10MHz to 18MHz.

The FADC has two differential inputs instead of four and provides a significantly shorter conversion time namely if the increased peripheral clock of 110MHz is used.

3.4 TC1167 / TC1767 vs. TC1782N / TC1782F

3.4.1 Feature Comparison

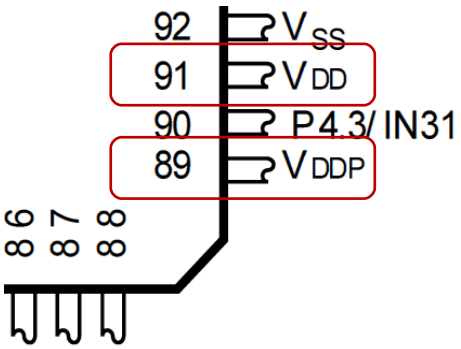
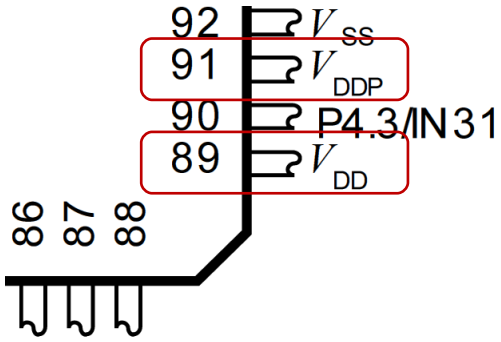
		TC1167 & TC1767	TC1782N & TC1782F
Core	TC Version	1.3.1	1.3.1
	Frequency (max.)	133 MHz	180 MHz
Flash	Program Flash	1.0 MB (TC1767: 2.0 MB)	2.5 MB
	Data Flash	64 KB	128 KB
SRAM	Σ (w/o PCP, Cache)	96 KB	176 KB
	PMI	24 KB	40 KB
	DMI	72 KB	128 KB
	Overlay	8 KB	8 KB
PCP	Frequency (max.)	133 MHz	180 MHz
	Code Memory	16 KB	32 KB
	Parameter Memory	8 KB	16 KB
DMA	Channels	8	16
ADC	Σ Analog Inputs	36	36
	ADC Modules / Channels	2 x 16	2 x 16
	FADC Channels	4	4
Timer	Σ Timed IO (max.)	80	80
	GPTA	1	1
	LTCA / cells	1 / 32	1 / 32
Interfaces	FlexRay	-	1 (TC1782**F** only)
	CAN nodes / objects	2 / 64	3 / 128
	SSC / ASC	2 / 2	3 / 2
	MLI / MSC	1 / 1	1 / 1
Package		LQFP 176	LQFP 176 (ePAD)
Temperature (ambient)		-40 °C ... +85 (125) °C	-40 °C ... +125 °C

3.4.2 Design Compatibility

The TC1782 provides very good pin compatibility to the TC1167 with two major differences:

- core supply voltage of 1.3V instead of 1.5V
- two swapped supply pins (V_{DD} <=> V_{DDP})

Table 7 Swapped supply pins

TC1167 & TC1767	TC1782N & TC1782F
	

Due to the increased operating frequency the power supply current for the core (1.3V) is significantly higher. The other power supply currents are similar to the TC1167.

The TC1782 uses an LQFP package with exposed pad to reduce the thermal resistance. Utilizing the exposed pad is strongly recommended.

Table 8 Changed/Removed Functionality

Pin	TC1167 & TC1767	TC1782N & TC1782F
89	V_{DDP}	V_{DD}
91	V_{DD}	V_{DDP}
146	LTCA2 Input 1	MSC0 Serial Data Input 1
151	GPTA0 Output 66	FlexRay (TC1782**F** only)
152	GPTA0 Output 67	FlexRay (TC1782**F** only)
175	GPTA0 Output 70	MSC0 Clock Output Positive C
176	GPTA0 Output 71	MSC0 Serial Data Output Positive C

Table 9 Added Functionality

Pin	TC1167 & TC1767	TC1782N & TC1782F
1...8	timed IO	additional SSC2
9, 13...16, 19	timed IO	additional FlexRay (TC1782**F** only)
86, 87	timed IO	additional CAN
149, 150	timed IO	additional FlexRay (TC1782**F** only)

3.4.3 Features, Peripherals & Software Compatibility

For the TC1782 the same tool chains can be used as for the TC1167, namely since the core revision and the memory configuration remains the same.

The maximum clock rate of the PCP has been increased from 133MHz to 180MHz. For PCP frequencies exceeding 90MHz, 2:1 mode vs. the FPI bus has to be enabled.

The TC1782 provides 40KB scratch pad RAM instead of 24KB and significantly more SRAM for data – 128KB vs. 72KB.

In addition both the SRAM in DMI and PMI can be ECC protected.

The PCP has access to 32KB of code memory and 16KB of parameter memory.

Following is a description of the more important changes in the peripherals.

The TC1782 can use a peripheral clock of 90MHz instead of 80MHz, allowing several peripherals like CAN, ASC, SSC, MSC, MLI to achieve higher data rates.

The TC1782 includes four high-speed synchronous serial interfaces (SSC) instead of two.

The TC1782**F** incorporates an E-Ray IP-module with two channels performing communication according to the FlexRay™ 1) protocol specification v2.1.

The MultiCAN module implemented provides three independent CAN nodes instead of two with a maximum of 128 message objects.

The maximum ADC clock has been increased from 10MHz to 18MHz.

The FADC can make use of the increase peripheral clock of 90MHz instead of 80MHz in order to achieve shorter conversion cycles.

3.5 TC1197 / TC1797 vs. TC1793N / TC1793F

3.5.1 Feature Comparison

		TC1197 & TC1797	TC1793N & TC1793F
Core	TC Version	1.3.1	1.6
	Frequency (max.)	180 MHz	270 MHz
Flash	Program Flash	2.0 MB / 4.0 MB	4.0 MB
	Data Flash	64 KB	192 KB
SRAM	Σ (w/o PCP, Cache)	176 KB	288 KB
	PMI	40 KB	48 KB
	DMI	128 KB	144 KB
	Overlay	8 KB	8 KB
PCP	Frequency (max.)	180 MHz	200 MHz
	Code Memory	32 KB	32 KB
	Parameter Memory	16KB	16KB
DMA	Channels	16	24
ADC	Σ Analog Inputs	44	44
	ADC Modules / Channels	3 x 16	3 x 16
	FADC Channels	4	4
Timer	Σ Timed IO (max.)	112	112
	GPTA	2	2
	LTCA / cells	1 / 32	1 / 64
	GPT12	-	2
	CCU6	-	2
Interfaces	FlexRay	1 (TC1797 only)	1 (TC1793**F** only)
	CAN nodes / objects	2 / 128	4 / 128
	SSC / ASC	2 / 2	4 / 2
	MLI / MSC	2 / 2	2 / 2
	EBU	1	1
Package		BGA-416	BGA-416
Temperature (ambient)		-40 °C ... +125 °C	-40 °C ... +125 °C

3.5.2 Design Compatibility

The TC1793 has been designed to be 100% pin compatible to the TC1797.

(Care must be taken regarding the configuration of the port pins since the TC1793 provides improved/additional peripheral modules.)

The only major difference is the core voltage which has been reduced from 1.5V to 1.3V. In most cases this could be solved by using a different fixed voltage variant of the respective power supply (e.g. changing from TLE 7368E to TLE 7368-3E) or by changing the setting of the output voltage in case of an adjustable regulator.

While the typical values of the supply currents are in the same region as with the TC1797 care must be taken if the TC1793 is run at frequencies above 200MHz. Here the core supply currents can be significantly higher.

3.5.3 Features, Peripherals & Software Compatibility

The most significant change is the new core revision of the TC1793: TC 1.6 vs. TC1.3.1. Together with the change of the core bus (LMB) to a cross bar (SRI) this results in significant improvements in performance.

The latest revisions of the TriCore tool chains support this new core revision, older tool chains can still be used as the new core revision is binary backwards compatible. Code compiled for TC1.3.1 can be run on the TC1.6 without modification.

The maximum clock rate of the PCP has been slightly increased from 180MHz to 200MHz. There are only a limited number of clock ratios between CPU, PCP, Flash and the busses allowed. Please refer to the respective chapter in the user's manual.

The TC1793 provides bigger caches as well as an additional block of 128KB of local SRAM for data or code.

The size of the data flash has been increased from 64KB to 192KB.

All memories including flash and SRAM can be ECC secured and the memory protection has been further improved implementing 16 data and 8 code ranges.

The number of DMA channels has been increased to 24.

The external bus unit (EBU) provides an improved feature set namely in terms of the memory types supported, e.g. support for SDRAM and DDRAM. The internal connection to the SRI cross bar allow for significantly higher data rates to the external memories or peripherals.

The TC1793 integrates several measures targeted at safety and security applications. These measures e.g. include a safe DMA controller (SDMA), a bus monitor unit (BMU), a memory checker module, a Flexible CRC Engine (FCE) and a secure hardware extension (SHE).

The FCE is meant to be used as a hardware acceleration engine for software applications or operating systems services using CRC signatures.

Following is a description of the more important changes in the peripherals.

In principle the TC1793 can use a peripheral clock of 100MHz instead of 90MHz, for faster data transfers and peripheral clocks. Due to the integer ratios of the clocks this would only be possible if the core is run at 200MHz (or in case of the 200MHz device). In the configuration with the core at 270MHz the peripheral bus runs at 90MHz.

The TC1793 includes four high-speed synchronous serial interfaces (SSC) instead of two. The data transmission over these interfaces can be assured by using the four new SSC guardian modules. These SSCG monitor the data on both the internal bus as well as the actual pin therefore securing the integrity of the data transmitted.

The TC1793**F** incorporates an E-Ray IP-module with two channels performing communication according to the FlexRay™ 1) protocol specification v2.1.

The MultiCAN module implemented provides four independent CAN nodes instead of two.

The TC1793 provides an interface for 'Single Edge Nibble Transmission (SENT)' which is used to connect sensors mainly in the automotive application area.

The number of local timer cells in the LTCA has been increased to 64 as it was in the TC1796.

The TC1793 incorporate several additional timer units: two Capture Compare Units CCU6 and two general purpose timer units (GPT12).

The CCU6 provide two independent timers (T12, T13), which can be used for PWM generation, especially for AC-motor control or power conversion stages. Additionally special control modes for block commutation and multi-phase machines are supported.

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. Its functionality includes enhanced incremental interface modes and clock prescaler support.

The maximum ADC clock has been increased from 10MHz to 18MHz (20MHz for theADC2).

All ADC input channels now include broken wire detection.

The FADC can achieve a slightly shorter conversion time if the increased peripheral clock of 100MHz is used.

4 AUDO MAX

4.1 Placement options

The devices of the AUDO MAX family are offered with several memory sizes and clock frequencies to allow scalability on the system level.

In addition there are two possibilities for PCB placement options providing even higher scalability:

Table 10 Placement options

PG-LQFP-176	TC1728	TC1782
PG-LFBGA-292 / -516	TC1791	TC1798

4.2 TC1728 ⇔ TC1782

As described above the TC1728 and TC1782 are both compatible with the TC1767 from the AUDO FUTURE generation. Consequently it is also possible to design a PCB board which can accommodate both devices.

The most important point to take into account is the fact that the TC1782 has significantly more supply pins compared to the TC1728. On the TC1728 these pins are used for the ports P8, P9 and P10 and alternate functions.

The supply pins which on the TC1728 provide the input voltage for the EVR are ground on the TC1782. In a combined layout it is recommended to leave these pins unconnected.

The analog inputs AN16...31 are overlaid with port P11 on the TC1728 providing additional IO.

Due to the differences in a number of peripheral modules it is impractical to list all pins with different functionality. Therefore the table below only lists pins which changed from being power supply to IO.

Table 11 Changed Functionality from power supply to IO

Pin	TC1728N	TC1782N & TC1782F
84, 91, 99, 123, 170	IO (P8.7, P8.10, P1.4, P8.4, P9.4) & peripherals	V_{DD}
11, 83, 89, 100, 124, 139, 171	IO (P9.7, P8.6, P8.9, P8.12, P8.3, P8.2, P9.3) & peripherals	V_{DDP}
107	V_5 (EVR supply)	IO (P1.4)
22, 70, 155	V_5 (EVR supply)	V_{SS}
12, 82, 85, 92, 125, 140, 172	IO (P9.8, P8.5, P8.8, P8.11, P8.13, P8.1, P9.2) & peripherals	V_{SS}
23, 24, 25, 26	IO (P10.0..10.3) & SSC	V_{DDAF} , V_{DDMF} , V_{SSMF} , V_{FAREF}
27	V_{PDG} (EVR pass gate)	V_{FAGND}
32...48	IO (P11.x) & AN31...16	AN31...16
141	IO (P8.0) & peripherals	V_{DDFL3}

4.3 TC1791 ⇔ TC1798

The high end members of the AUDO MAX family have been designed with special focus on compatibility and scalability. While the TC1793 is pin compatible to the TC1797 from the AUDO FUTURE family, the TC1791 and TC1798 provide the scalability within the family.

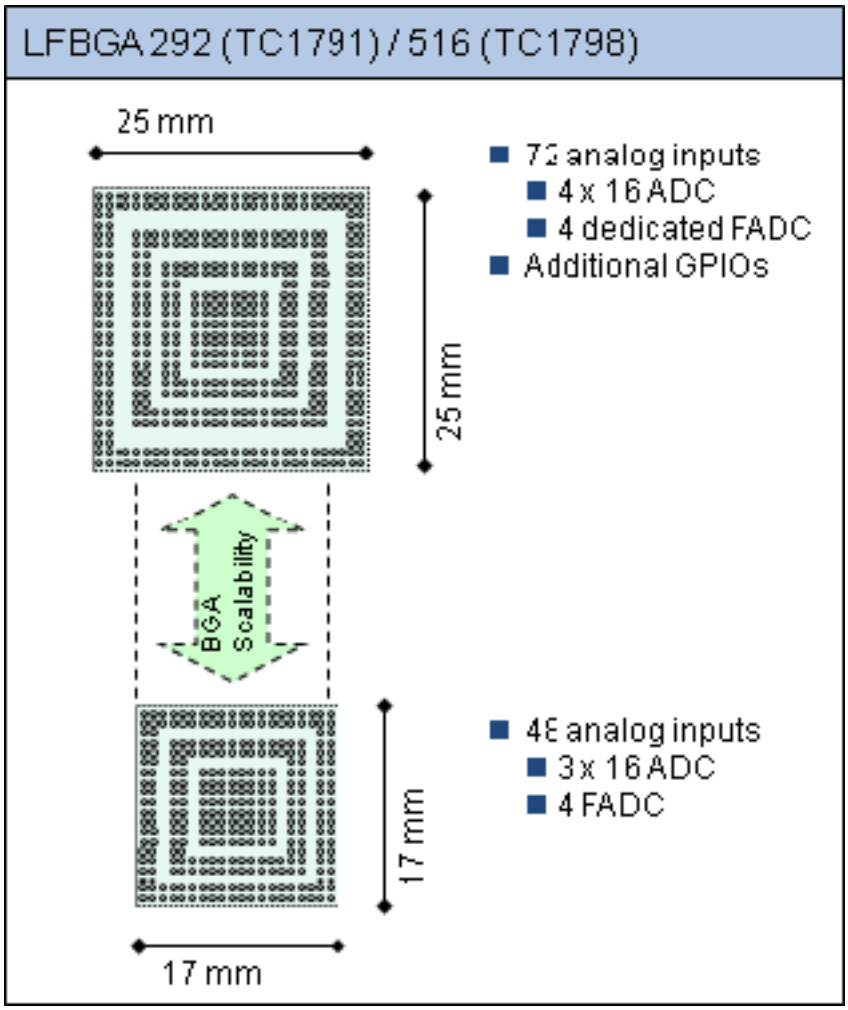
The inner ball rings of the TC1798 are fully compatible both in terms electrical parameters as well as functionalities to the TC1791, so a design created for the TC1798 can also accommodate the TC1791. Software written in a modular way can exploit this as well.

The additional balls of the TC1798 provide the following additional functionality:

Table 12 TC1798 additional IO capabilities

Functionality	Description
EBU	external bus unit for memories & peripherals
P11,12, 15, 16, 18	additional IO ports
Px	additional IO pins in the available ports
ADC3	additional fourth ADC with 16 inputs
FADC	4 dedicated FADC inputs

Figure 2 AUDO MAX high end scalability



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