Application Note, V 1.0, April 2005

AP32086

EMC

Design Guideline for

TC1796

Microcontroller Board Layout

Microcontrollers

Never stop thinking.

Revision History:	2005-04	**V 1.0**
Previous Version:	-	

Page	Subjects (major changes since last revision)

Controller Area Network (CAN): License of Robert Bosch GmbH

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
mcdocu.comments@infineon.com

Edition 2005-04

Published by
Infineon Technologies AG
81726 München, Germany

LEGAL DISCLAIMER

THE INFORMATION GIVEN IN THIS APPLICATION NOTE IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Table of Contents

Page

1 Overview

The TC1796 is a 32-Bit microcontroller in BGA 416-pin package, which requires a carefully designed PCB concerning electromagnetic compatibility. In additional to the Infineon PCB Design Guidelines for Microcontrollers (AP2426), which gives general design rule informations for PCB design, some product-specific recommendations and guidelines for TC1796 are discussed here.

2 General Information

The microcontroller has three supply domains (1.5V Core / 2.5V EBU/ 3.3V I/O Pad), which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain should be made with different planes on a supply layer.

2.1 Ballout of TC1796

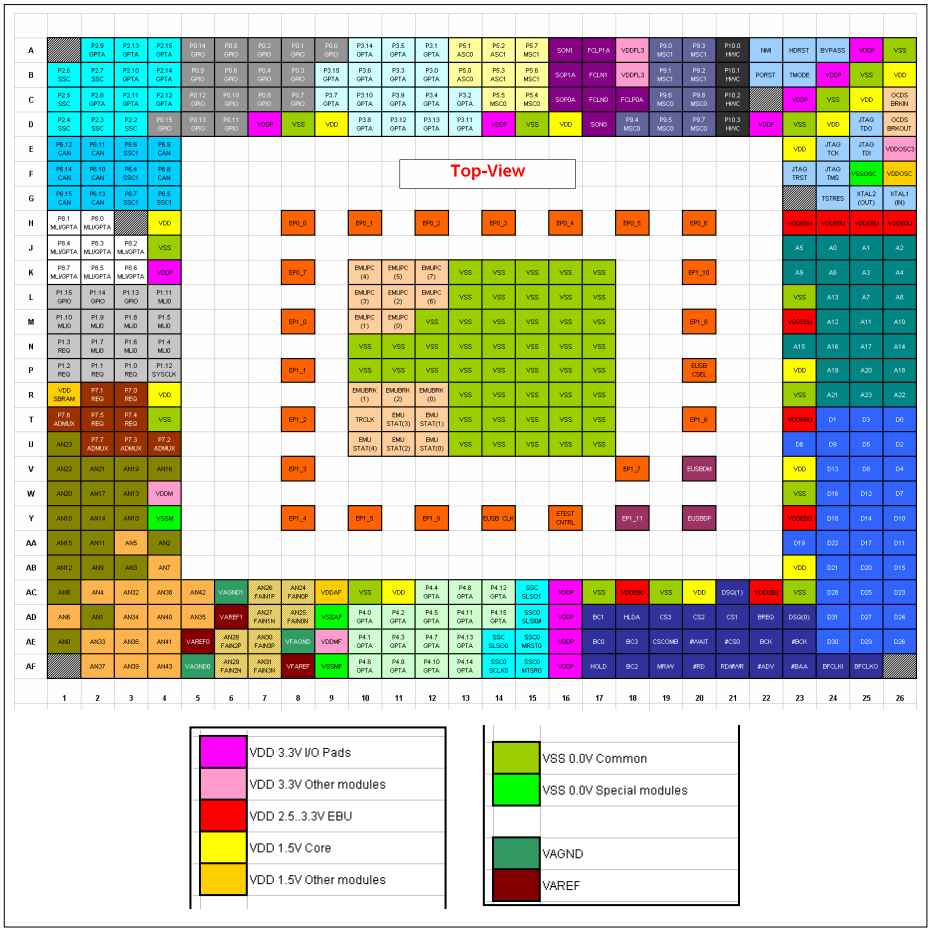

Figure 1 Ballout of TC1796 (Supply pins colored to show the position)

2.2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB, following signals have to be considered as critical. Route these signals with adjacent ground reference and use as less as possible vias (no reference layer change!) route them as short as possible. Routing ground on each side can help to reduce coupling to the other signals.
  - BFCLKO and BFCLKI: Burst Mode Flash Clock Output/Input
  - TCLKO and SYSCLK: Transmit channel clock output/ System clock output
  - Supply pins (core supply)
- Address and data buses can also cause radiation. Using series resistors can help to prevent signal integrity problems. Route bus signals locally between memory and TC1796 avoiding layer changes where possible.
- For unused **"Output, Supply, Input and I/O"** pins following points must be considered:

Table 1

1. Supply Pins (Modules)	- See product specification
2. I/O-Pins	- must be configured as output and driven to static low in the weakest driver mode. - solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering)
3. Output Pins including LVDS	- should be driven static in the weakest driver mode. - if static output level is not possible, the output driver should be disabled. - solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering)
4.Input Pins without internal pull device	- For pins with alternate function see product target specification to define the necessary logic level - must be connected with high-ohmic resitor to GND (range 10k – 1Meg) - groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current)
5. Input Pins with internal pull device	- For pins with alternate function see product specification to define the necessary logic level - must be configured as Pull-down and should activated static low (exception: if the product specification requires high level for alternate functions) - solderpad should not be connected to any other net (isolated PCB-pad only for soldering)

- The ground system must be designed as follows:
  - Separate of analog and digital grounds.
  - The analog ground must be separated into three groups:
    1. Ground for OSC (F25),
    2. Ground for ADC0/1 (AF5, AC6, Y4),
    3. Ground for FADC (AF9, AD9, AE8)
- To reduce the radiation / coupling from oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections of the load capacitors and VSSOSC should also be connected to this island. Traces for load capacitors and Xtal should be as short as possible.
- The power distribution from the regulator to each power plane should be made over filters (EMI filter using ferrite beads).
- A target inductance value of <0.7nH (VDDC), <1.5nH (VDDE), <7nH (VDDP) for the connection of decoupling capacitors to the supply pins is required.
- Inductance/Ferritebeads on supply paths L ~10µH /1A (at regulator output and at the branching to the other module supply pins like VDDOSC, VDDOSC3,VDDFL3…see Figure 2).

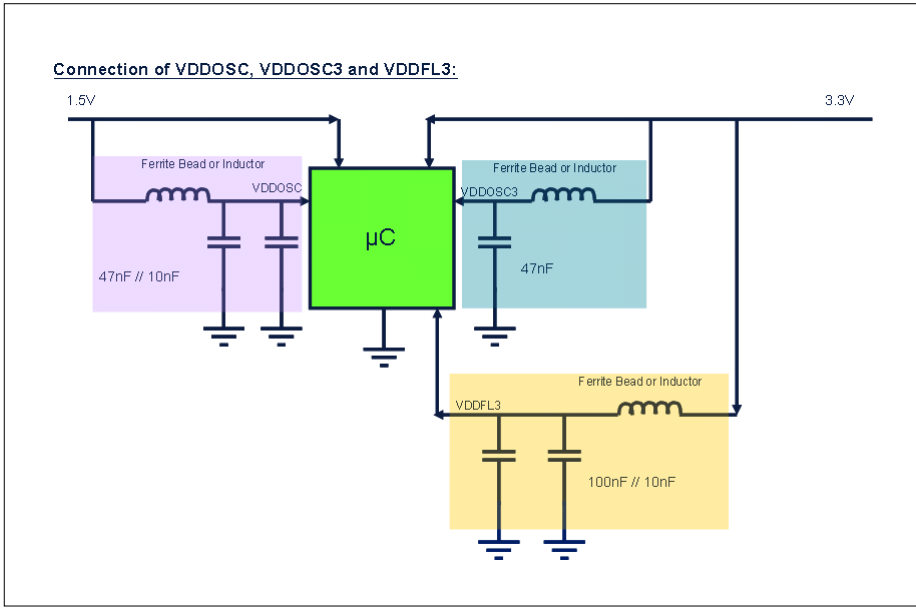

Figure 2 Filtering of VDDOSC, VDDOSC3 and VDDFL3 supply pins

Note: (for BC Step only, for future steps please refer to the corresponding Errata Sheet):
Because of long-term PLL-Jitter issue, caused by noise on VDD, an additional measure has to be taken into the care. To reduce the long-term PLL-Jitter to max. 15ns, some additionally decoupling capacitors must be placed on VDD Pins: Four 10µF capacitors have to be connected parallel to the capacitors on pins E23 (47nF//10µF), D24 (47nF//10µF), P23 (100nF//10µF) and V23 (100nF//10µF). For details of long-term PLL-Jitter see the corresponding Errata Sheet document .

2.3 Decoupling

- All three supply domains of TC1796 should be decoupled separately (see decoupling layout example)
- Type of capacitors:
- Values: 10nF, 47nF, 100nF
- X7R Ceramic Multilayer (Low ESR and low ESL)
- All supply balls should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS balls should be connected to the GND layer (see layout example on next pages).
- The decoupling capacitors should be placed directly under the IC or if neccesary, some capacitors can be placed on top layer close to the supply pins of the IC.
- Ground plane on bottom layer can be used to connect the capacitors If no plane is used, they should be connected with vias to the GND layer.
- Multiple vias can be used at capacitors to get a low impedance connection between capacitors and power/GND planes or balls.
- All capacitors must be placed as close as possible to the related supply pin group.
- For packages of BGA type, most Vss pins are grouped in the center of the controller. In general, the corresponding Vdd pins are located on the inner row of the outer circle. This pinning allows a short connection to the decoupling capacitors, when placed on the opposite side of the PCB.

A power-plane/grounding concept example for a 32-bit microcontroller with BGA package can be seen in figure 3. This layout example shows three supply domains (1.5V, 2.5V, 3.3V), where 1.5V is core supply, 2.5V is external bus unit supply and 3.3V is pad supply voltage.

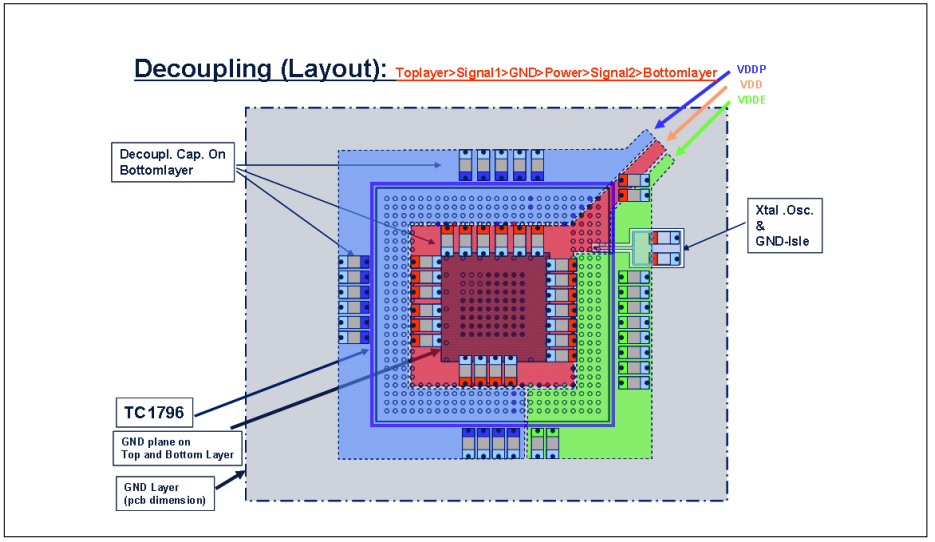

Figure 3 Decoupling of TC1796 (Layout example)

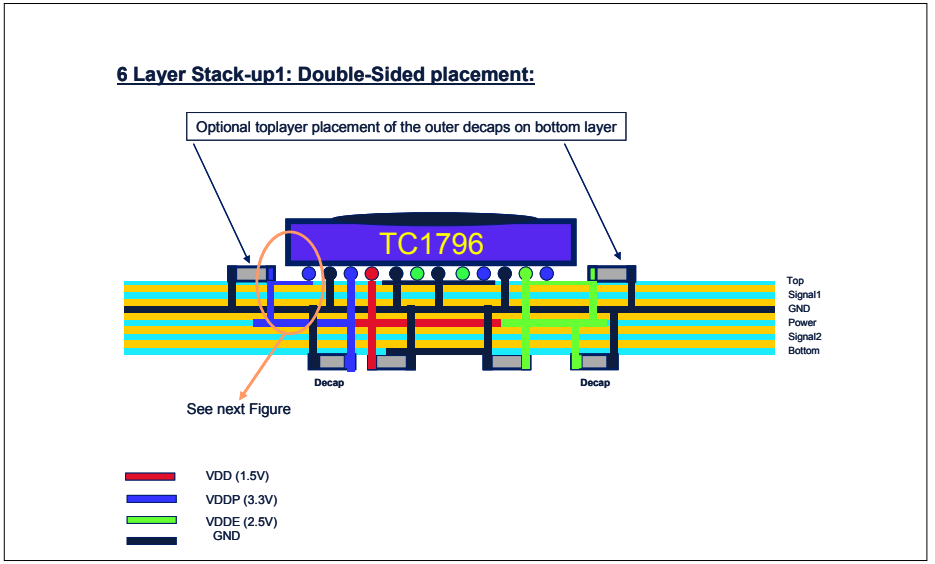

Figure 4 6-Layer PCB: Stack-up

The general way is to connect the VDD and GND first to the capacitors and then connect to the balls of the IC. The GND and VDD supply planes are on the 3rd and 4th layer. Additionally there is an other GND plane on the 2nd layer.

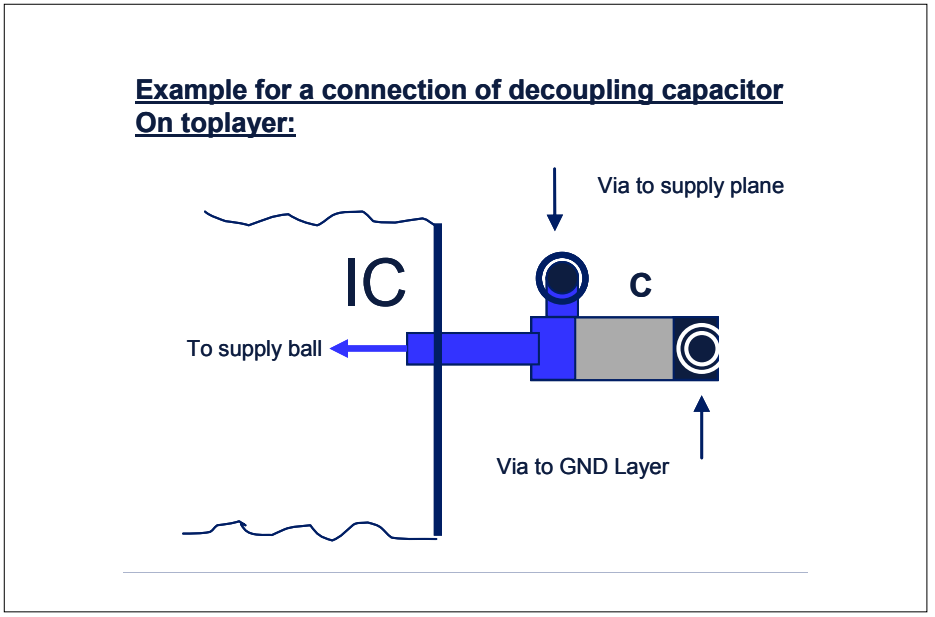

Figure 5 Connection of a decoupling capacitor

Table 2 Decoupling Capacitor List:

Capacitor Type		Supply	Pins	Remarks
100nF	X7R	VDD	H4	
100nF	X7R	VDD	R4	
100nF	X7R	VDD	AC11	
100nF	X7R	VDD	AC20	
100nF	X7R	VDD	AB23	
100nF	X7R	VDD	V23	← 10µF Parallel *)
100nF	X7R	VDD	P23	← 10µF Parallel *)
100nF	X7R	VDD	D9	
100nF	X7R	VDD	D16	
47nF	X7R	VDD	B26	
47nF	X7R	VDD	C25	
47nF	X7R	VDD	D24	← 10µF Parallel *)
47nF	X7R	VDD	E23	← 10µF Parallel *)
10nF	X7R	VDDP	A25	
10nF	X7R	VDDP	B24	
10nF	X7R	VDDP	C23	
10nF	X7R	VDDP	D22	
10nF	X7R	VDDP	D14	
10nF	X7R	VDDP	D7	
10nF	X7R	VDDP	K4	
10nF	X7R	VDDP	AC16	
10nF	X7R	VDDP	AD16	
10nF	X7R	VDDP	AE16	
10nF	X7R	VDDP	AF16	
47nF	X7R	VDDE	H26	
47nF	X7R	VDDE	H24	
10nF	X7R	VDDE	H25	
10nF	X7R	VDDE	H23	
10nF	X7R	VDDE	M23	
10nF	X7R	VDDE	T23	
10nF	X7R	VDDE	Y23	

10nF	X7R	VDDE	AC23	
10nF	X7R	VDDE	AC18	
10nF	X7R	VDDAF	AC9	
10nF	X7R	VDDM	W4	
10nF	X7R	VDDMF	AE9	
47nF	X7R	VDDOSC	F26	
47nF	X7R	VDDOSC3V3	E26	
47nF	X7R	VDDFL3	A18	
47nF	X7R	VDDFL3	B18	
47nF	X7R	VDDSBRAM	R1	

Total = 9 x 100nF, 11 x 47nF, 21 x 10nF, (4 x 10µF, for BC Step only)

*Note: *) for BC Step only, for future steps please refer to the corresponding Errata Sheet*

http://www.infineon.com

Published by Infineon Technologies AG