

AP32058

OCDS L2 Trace Port Connector

TriCore Based Boards

AI ICore



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OCDS L2 Trace Port Connector**Revision History: 2001-12****V2.3**

Previous Version: V2.2

Page	Subjects (major changes since last revision)
	Major changes and corrections to the technical content and document layout and design.
	Adapted to reflect current signal naming conventions.
	Table footnotes added.
	V2.1 & V2.2 were intermediate versions.

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1 Introduction

This document describes the Infineon Technologies OCDS Level 2 TriCore trace-port connector.

This connector is specified for TriCore derivatives running with frequencies up to 80 MHz maximum. For frequencies beyond 80 MHz use the *OCDS L1/L2 & Nexus High-Speed Connector* (see Application Note AP32060).

In every case you should check with your Emulation Tool supplier the availability of the appropriate Trace Adapter for connecting your Target system.

2 The Connector Layout

2.1 Slow and Fast Signals, Shielding

The trace hardware must buffer all signals just after the connector, so the connector itself does not need to be highly shielded.

2.2 Mechanical

The following OCDS Level 2 connector should be used. The advantage of this connector is that it has more stability in the narrow direction.

"AMP System 50 Board Mounted Connectors" (AMPMODU) 40 pins.
Part number: 104549-6.

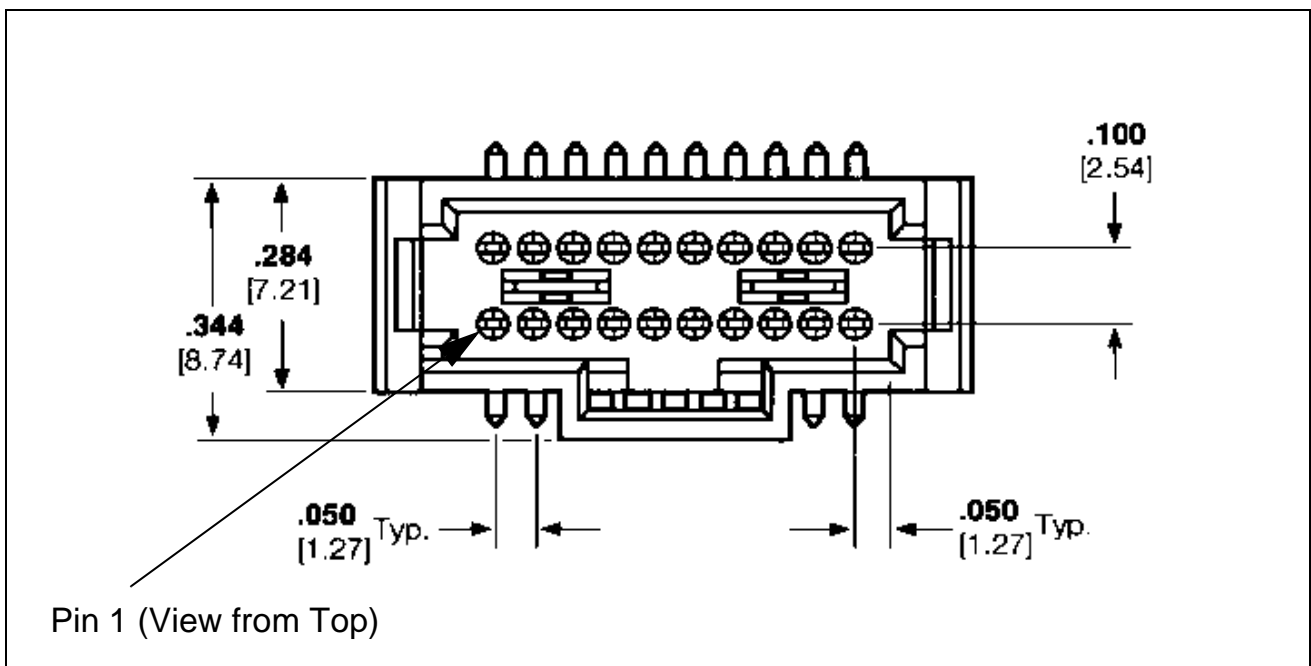


Figure 1 An AMPMODU Connector

The Connector Layout

Table 1 Pin Number Orientation

2	4	6	8	...	36	38	40
1	3	5	7	...	35	37	39

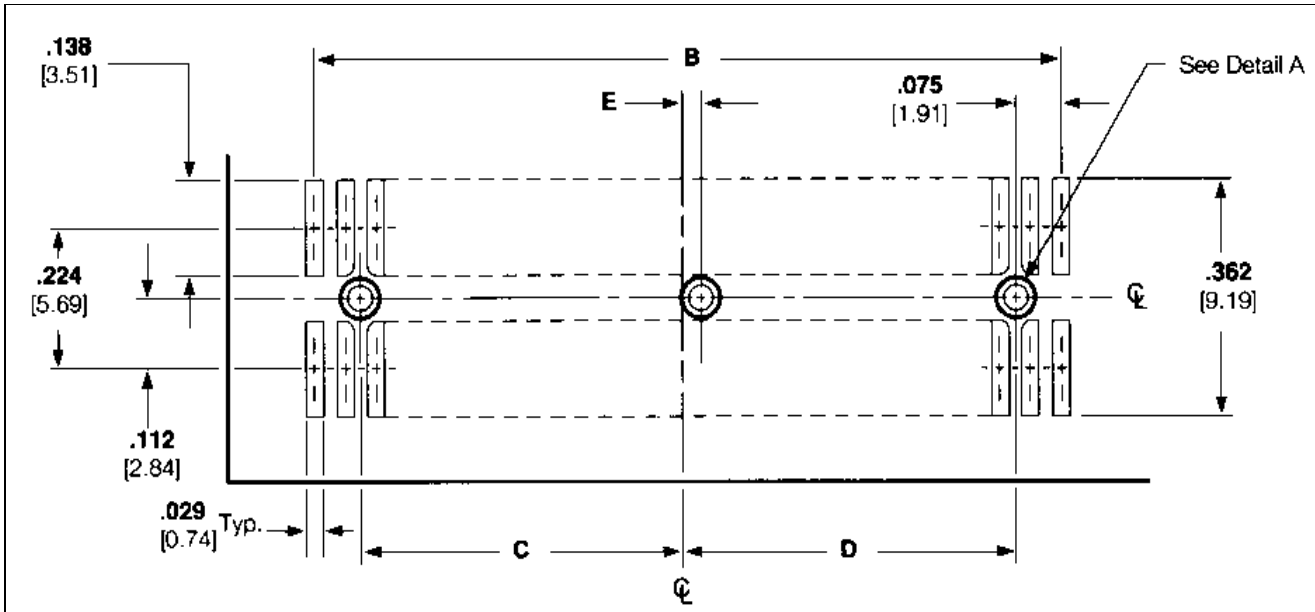


Figure 2 The Board Layout For This Connector.

Table 2 Connector Properties

Item	Size in [inch]	Size in [mm]
Dim. A	1.130	28.70
Dim. B	0.950	24.13
Dim. C	0.400	10.16
Dim. D	0.400	10.16

2.3 Signal Description

Following are the Infineon Technologies JTAG connector signals. Directions are given as follows:

- O = output from the CPU processor board to the debugger
- I = input to the CPU processor board from the debugger

Table 3 Signal Descriptions

Signal Name	Dir	Pin	Comment
CPU_CLOCK	O	1	CPU_CLOCK output
GND		2	Ground
		3	Reserved for future extension
EMUSTAT0	O	4	Pipeline status information
EMUSTAT1	O	5	Pipeline status information
EMUSTAT2	O	6	Pipeline status information
EMUSTAT3	O	7	Pipeline status information
EMUSTAT4	O	8	Pipeline status information
		9	Reserved for future extension
		10	Reserved for future extension
		11	Reserved for future extension
GND		12	Ground
		13	Reserved for future extension
IND PC0	O	14	Indirect PC bus
IND PC1	O	15	Indirect PC bus
IND PC2	O	16	Indirect PC bus
IND PC3	O	17	Indirect PC bus
IND PC4	O	18	Indirect PC bus
IND PC5	O	19	Indirect PC bus
IND PC6	O	20	Indirect PC bus
IND PC7	O	21	Indirect PC bus
		22	Reserved for future extension
		23	Reserved for future extension
		24	Reserved for future extension
		25	Reserved for future extension

Table 3 **Signal Descriptions (cont'd)**

Signal Name	Dir	Pin	Comment
GND		26	Ground
		27	Reserved for future extension
EMUBREAK0	O	28	Breakpoint qualification information
EMUBREAK1	O	29	Breakpoint qualification information
EMUBREAK2	O	30	Breakpoint qualification information
$\overline{\text{BRKOUT}}$	O	31	OCDS Break Out Signal
$\overline{\text{BRKIN}}$	I	32	OCDS Break In Signal
$\overline{\text{PCP_BRK_OUT}}$ ¹⁾	O	33	PCP Break Out Signal
		34	Reserved for future extension
		35	Reserved for future extension
V _{DD}		36	I/O Ring voltage of CPU
		37	Reserved for future extension
		38	Reserved for future extension
		39	Reserved for future extension
GND		40	Ground

¹⁾ This signal is not available on every TriCore Implementation. If the Microcontroller derivative has no corresponding signal, it should be left unconnected in the target hardware.

2.4 Voltage

All Signals have the voltage of the I/O ring. Current Microcontroller implementations have 5 V, 3.3 V or 2.5 V V_{DD} on I/O ring.

The V_{DD} I/O ring should be provided from the target based board to the active buffers at the cable level (if present).

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Dr. Ulrich Schumacher

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