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A/D Converter

C500 and C166 Microcontroller Families

Analog Aspects

Microcontrollers

Infineon technologies

Never stop thinking.

A/D Converter
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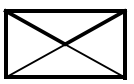

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1 Introduction

For analog signal measurement on most members of the C500 and C166 microcontroller families, an A/D (Analog/Digital) converter with multiplexed input channels and a sample and hold circuit has been integrated on-chip. Depending on the device type of the C500/C166 Family, an 8-bit or 10-bit A/D converter with 4, 8, 10, 12, 15, 16 or 24 multiplexed input channels, is integrated. The A/D converter uses the method of successive approximation.

In principle, the A/D converter can be divided in two parts, the analog interface (including the converter with sample and hold circuit) and the digital part, which contains different registers and the digital control unit. This Application Note provides basic information and recommendations concerning the analog part of the A/D converter. Please refer to the corresponding User's manual for the description concerning the digital part of the A/D converter.

Based on the history and evolution of the microcontrollers, there are different implementations of the A/D converter available. This Application Note is referred to the actual status of A/D converters, which are implemented in the C500/C166 Family. The differences of the analog part concern mainly the values in the A/D converter characteristics specified in the Data Sheet. For details, please use the corresponding Data Sheet.

The resolution (r) of the A/D converter refers to the number of quantization levels, an analog input voltage can be determined to. This number of smallest levels is given in bits and one of them is an LSB. **Figure 1** shows an example of an A/D converter with 1024 quantization levels. This A/D converter has a 10-bit resolution. An input voltage of 5 V is quantized with a step size of 5 V / 2^{10} = 4,88 mV.
This theoretical accuracy of an A/D converter is degraded by inaccuracies of the A/D converter itself (total unadjusted error). Further the accuracy of the total A/D conversion system is degraded by the involved external elements which are connected to the analog input ANx and to the reference voltage V_{AREF}.
It is the task of the system designer to keep the inaccuracies caused by the external circuits as low as possible. This application note provides the necessary basic information to optimize the external circuits of the A/D converter.

2 Transfer Characteristic and Error Definition

The following diagrams show the ideal transfer characteristic of an A/D converter and the error definition for the different kind of errors:

- Offset error
- Gain error
- Differential nonlinearity error (DNLE)
- Integral nonlinearity error (INLE)

The total unadjusted error (TUE) is specified in the Data Sheets of the C500 and C166 microcontrollers.

2.1 Ideal Transfer Characteristic

Figure 1 defines the ideal transfer characteristic for an A/D converter. The Ideal Transfer Curve (1) transfers each input to an output.

The Ideal ADC Transfer Curve (2) includes a quantization error, since all analog input values are presumed to exist, they must be quantized by partitioning the continuum into discrete digital values. All analog values within a given range (quantization step) are represented by the same digital value, which corresponds to the nominal mid- range value. That is the reason for the quantization uncertainty of +/- 0.5 LSB, which is a natural error and inherent to each A/D converter.

The quantization step size is 1 LSB = V_{AREF} / 2^r. According to the Ideal Transfer Curve (1) the first digital transition, from 0 to 1, occurs at the analog value of 0.5 LSB. That is why the first step width of the Ideal ADC Transfer Curve (2) is 0.5 LSB and the last step width is 1.5 LSB. The inherent quantization error in relation to the analog input voltage is shown in **Figure 2**

The total unadjusted error includes all A/D converter related inaccuracies like production process deviations and internal noise.

The TUE consists of offset error, gain error, DNLE and INLE but it is not simply the sum of individually measured errors. Since some errors of the ADC, like offset and gain error, can compensate each other, the TUE can be far less than the absolute sum of all individual errors. **Figure 1** shows the definition of the TUE in relation to the Ideal ADC Transfer Curve (1).

The real result of the A/D converter is in the range of Ideal ADC Transfer Curve (2) +/- TUE. This area is shaded in **Figure 1** and is between both TUE related to ideal ADC Transfer Curves (3) and (4).

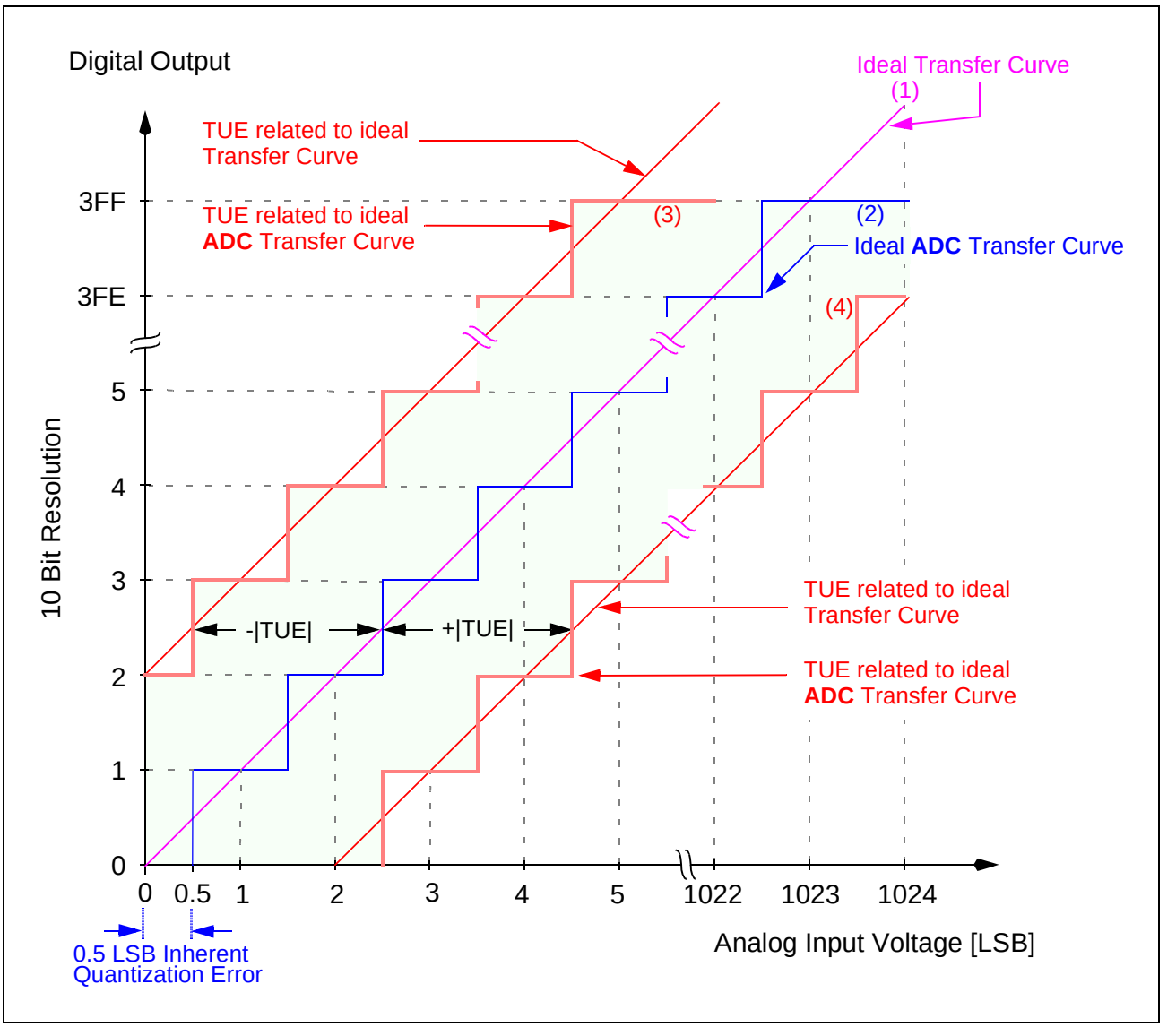


Figure 1 Ideal Transfer Characteristic

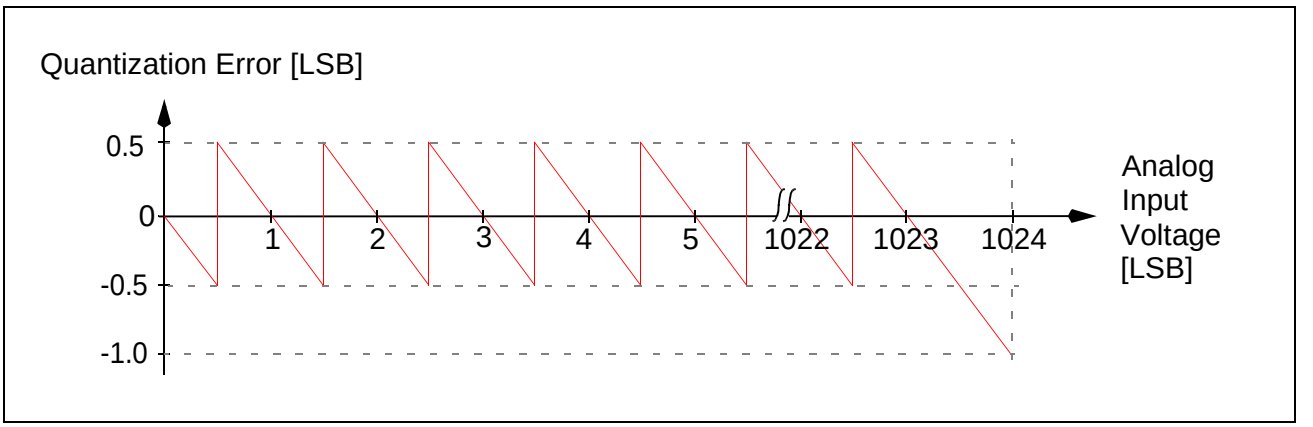


Figure 2 Quantization Error

2.2 Offset Error

The offset error is the deviation from the Ideal ADC Transfer Curve at the lowest transition level on the Real ADC Transfer Curve. It is the input voltage required to bring the digital output to zero and can be measured by determining the first digital transition, from 0 to 1, of the A/D converter. The offset error affects all codes by the same amount.. For the consideration in the figure below, all other kinds of errors (gain, DNLE, INLE) are excluded.

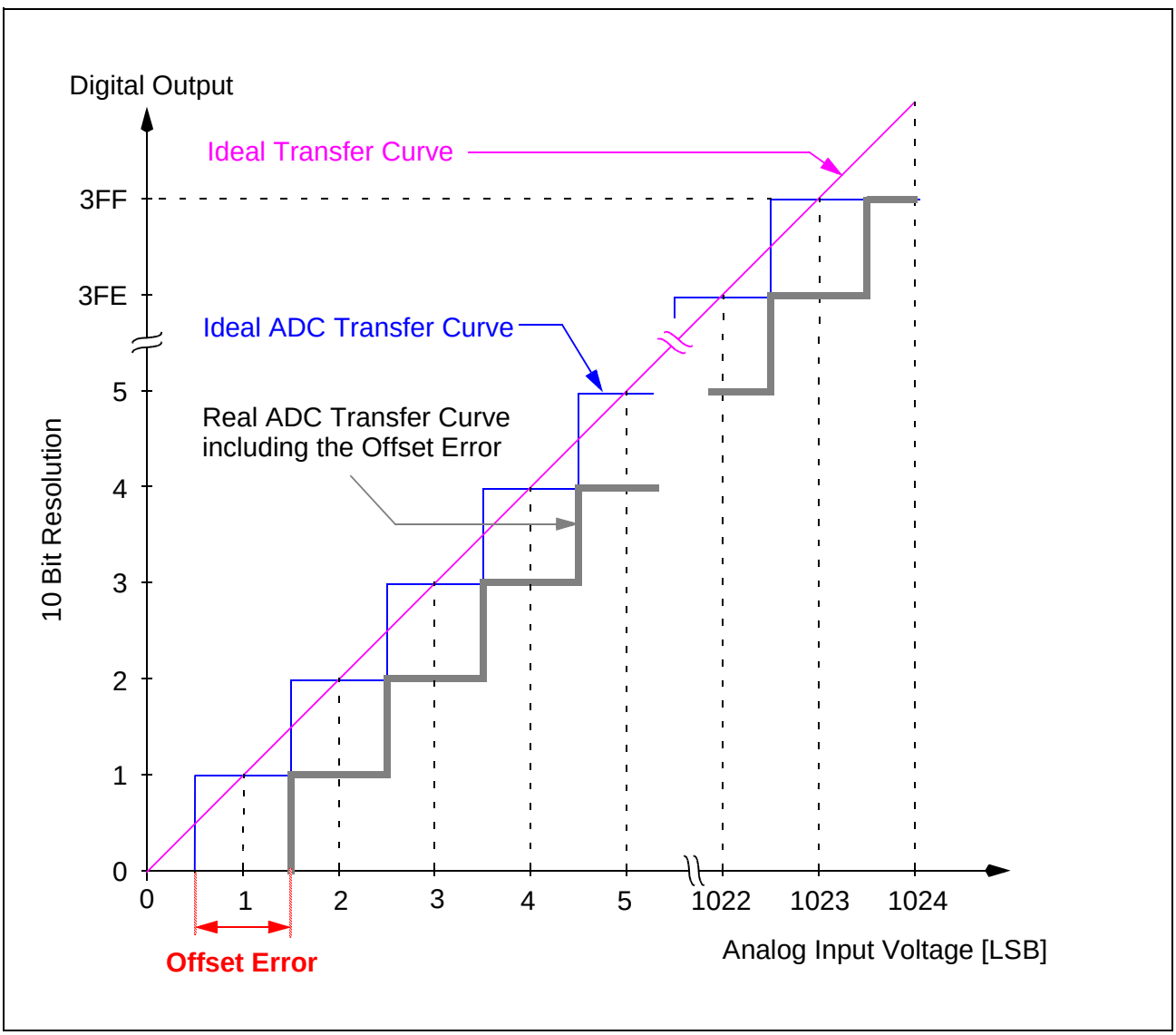


Figure 3 Offset Error

2.3 Gain Error

The gain error is the difference between the slopes of the real ADC Transfer Curve and the Ideal ADC Transfer Curve at the maximum digital out value. For the consideration in the figure below, all other kinds of errors (offset, DNLE, INLE) are excluded.

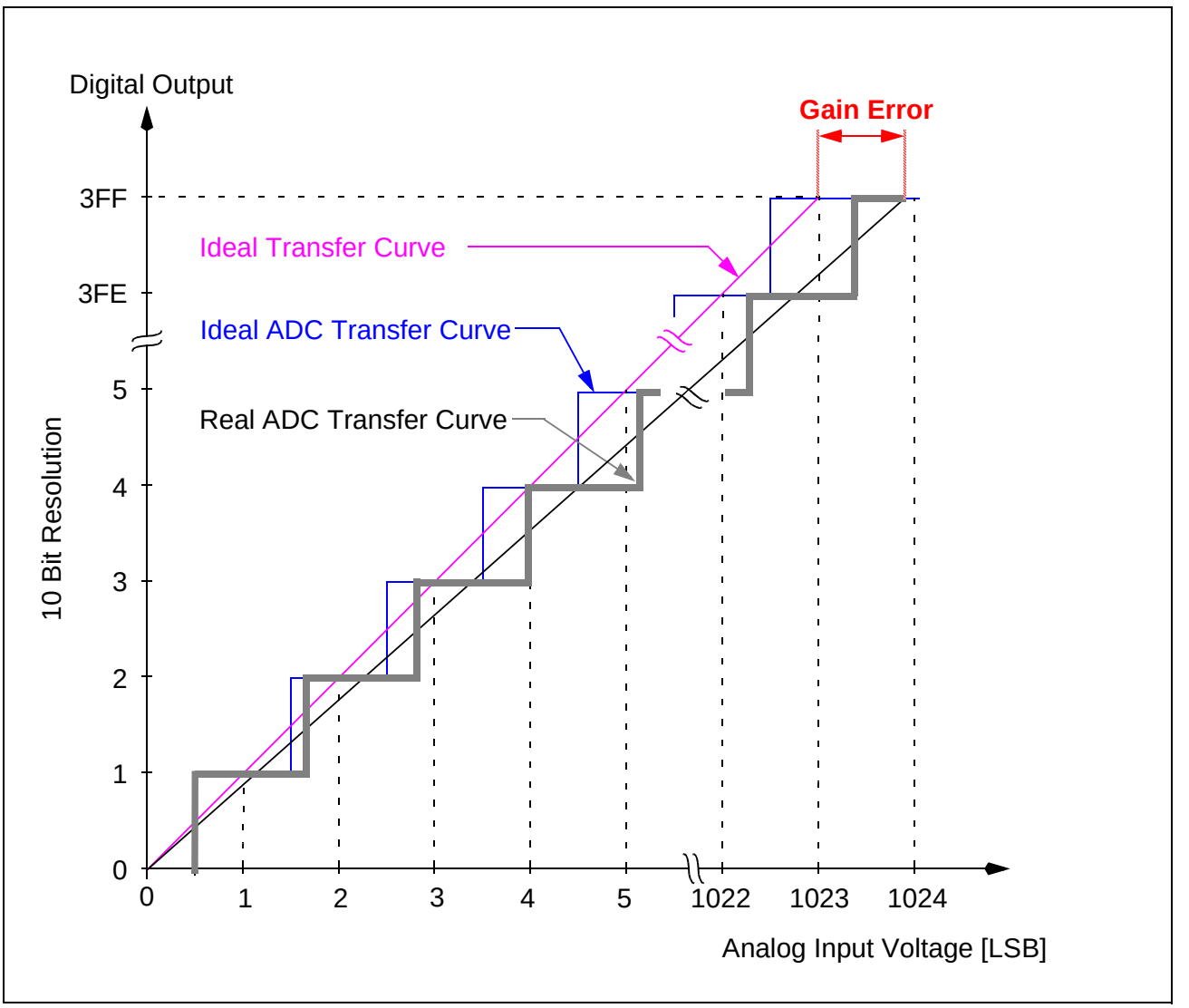


Figure 4 Gain Error

2.4 Differential Nonlinearity Error (DNLE)

The differential nonlinearity error describes variations in the analog value between adjacent pairs of digital numbers, over the full range of the digital output. If each transition step width is exactly 1 LSB, the differential nonlinearity error is zero. If the transitions are 1 LSB +/- 1 LSB, then there is the possibility of a missing codes. If a missing code occurs then one value of the digital output is missing, e.g. the digital output might jump from 0011 to 0101 and missing out 0100; See figure below.

If the differential nonlinearity error is less than 1 LSB, then a missing code is automatically excluded. For the consideration in the figure below, all other kinds of errors (offset, gain, INLE) are excluded.

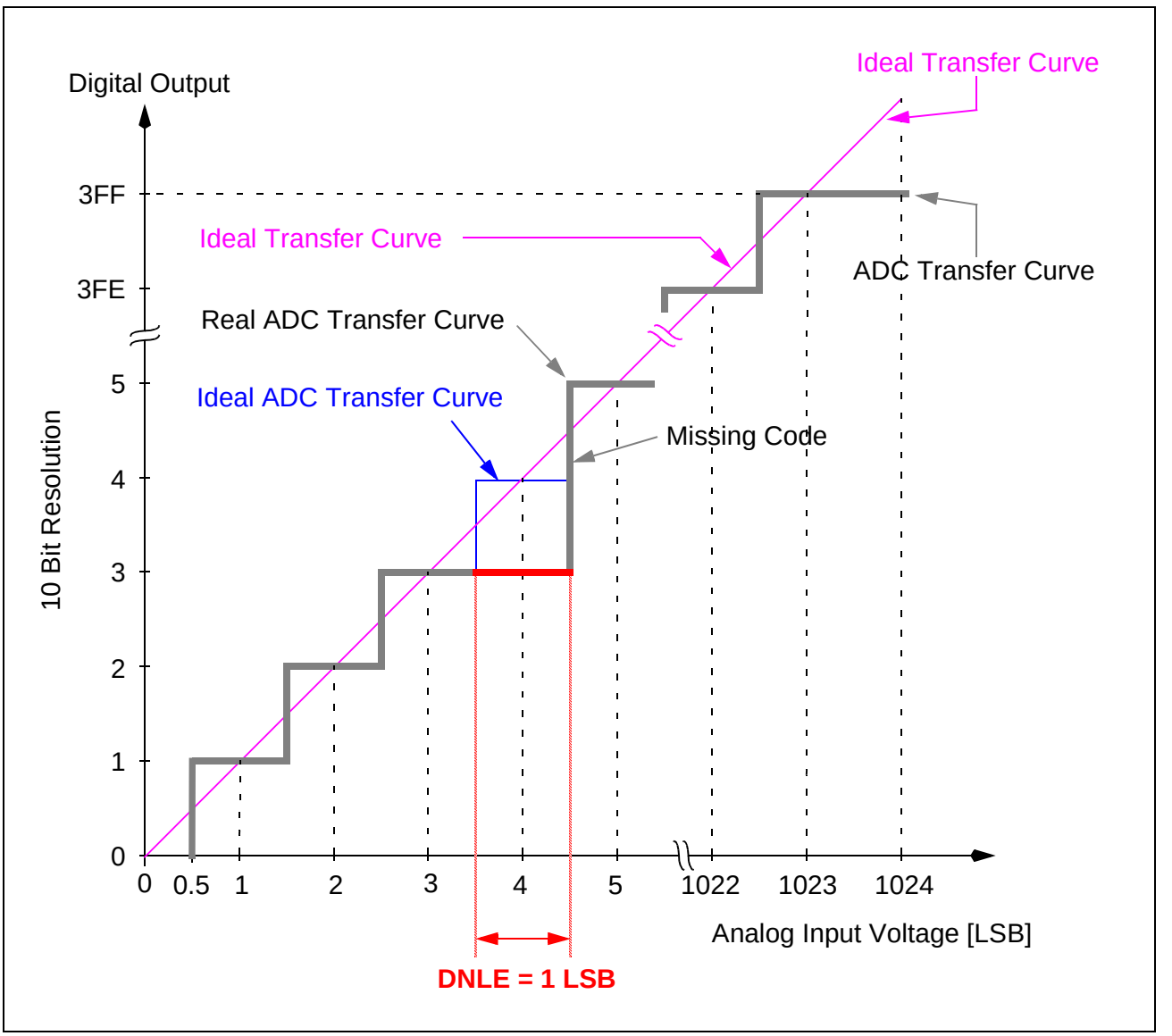


Figure 5 Differential Nonlinearity Error

2.5 Integral Nonlinearity Error (INLE)

The integral nonlinearity error is the maximum difference between the Ideal ADC Transfer Curve and the adjusted Real ADC Transfer Curve (without offset- and gain error). For the consideration in the figure below, DNLE is also excluded.

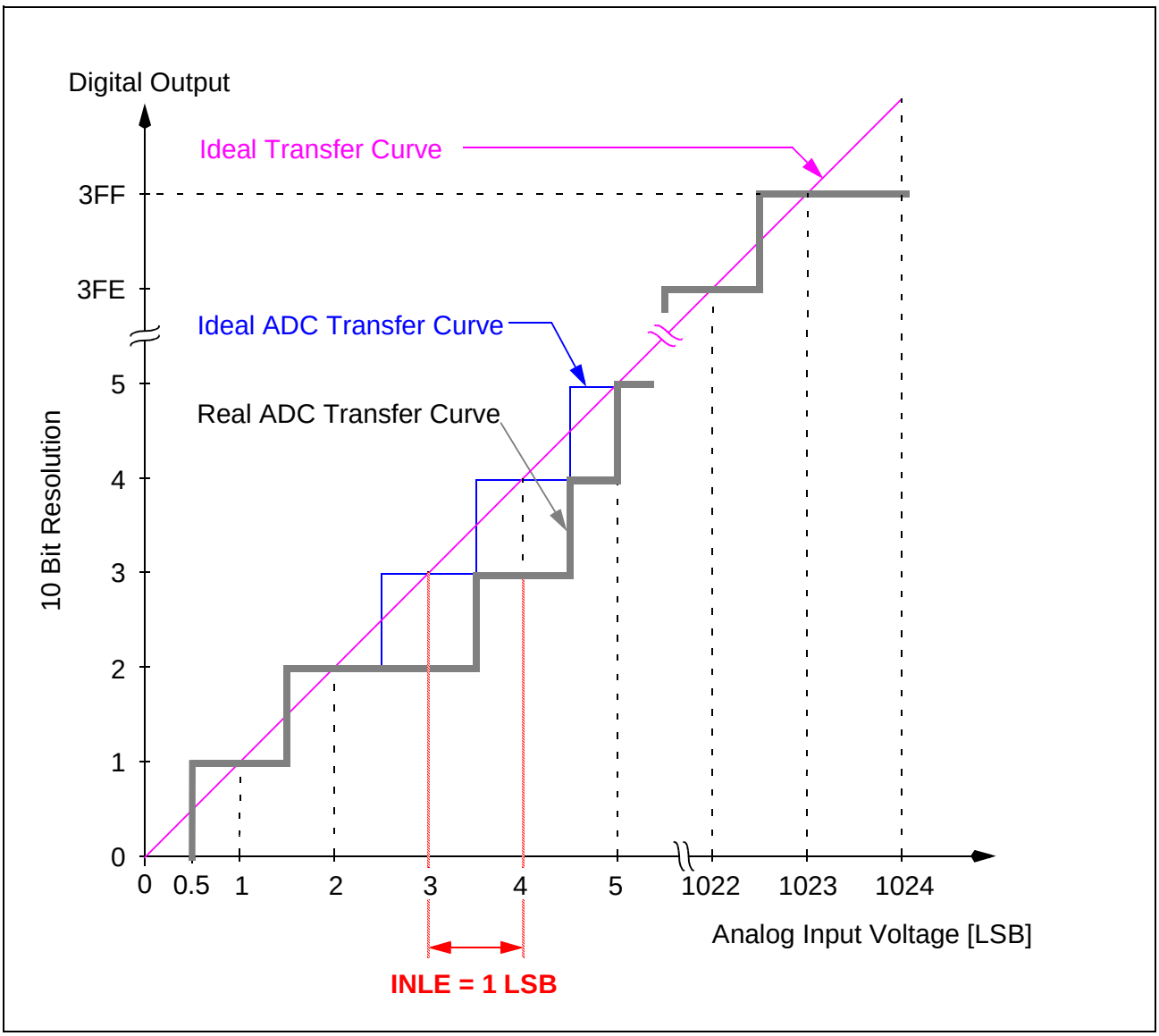


Figure 6 Integral Nonlinearity Error

3 Principle of Conversion

The A/D converter is based on the principle of successive approximation. It uses a capacitor network in order to compare the analog input voltage with the actual digital approximation of this voltage. The capacitor network is also used for the sample and hold function. The conversion is performed in several steps. A total conversion consists of:

- Sample phase
- Charge-redistribution phase (conversion phase)
- Calibration phase
- Write back phase

The sequence of the different phases is shown in **Figure 7**. The total ADC conversion time can be controlled via register ADCON (C166 Family). The block diagram in **Figure 8** is related to an A/D converter with 10 bit resolution and represents the principle connections between the analog input ANx, conversion C-net, comparator and the result register ADDAT.

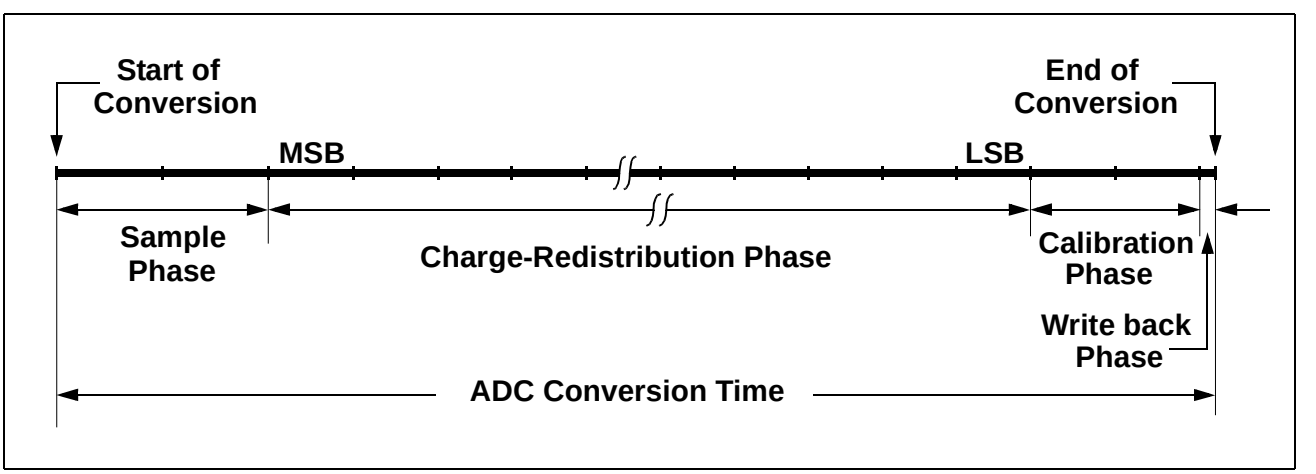


Figure 7 A/D Converter Timing

3.1 Sample Phase

During the sample phase, the conversion control unit connects the capacitors of the conversion C-net to one of the analog input channels via a multiplexer. The capacitor network is thus charged/discharged to the voltage level of the connected analog input channel. The hold capacitor C_{HOLD} at the comparator holds the analog input voltage after sample phase.

3.2 Charge-Redistribution Phase

At the end of the sample phase and with the start of the charge-redistribution phase, the conversion C-net is disconnected from the analog input. The goal now is to reconstruct the voltage level stored in the hold capacitor C_{HOLD} by connecting the capacitors C_9 to C_0 individually to V_{AREF} or V_{AGND}. As the capacitor network (conversion C-net) is binary weighted (i.e. $C_n = 2*C_{n-1}$), the charge of the capacitors C_9 to C_0, corresponds directly to the voltage level of the connected analog input channel. The digital value is found successively starting from the most significant bit down to the least significant bit. The comparator is used to decide whether the actual voltage of the capacitor C_n is below or above the voltage stored in the hold capacitance. The charge-redistribution phase is finished after 10 steps of successive approximation.

The conversion C-net for a 12-bit A/D converter consists of C_{11} to C_0 and 12 steps are required. The conversion C-net for a 8-bit A/D converter consists of C_7 to C_0 and 12 steps are required.

3.3 Calibration Phase

The conversion accuracy depends on the precision of the conversion C-net and the offset voltage of the comparator. In order to correct the errors that are introduced through process variations and offset voltage, an additional C-net (the calibration C-net) is used together with a calibration control logic. A detailed description of the calibration phase is shown in the chapter 4, Calibration Mechanism.

3.4 Write Back Phase

During the write back phase, the result of the successive approximation is copied to the result register ADDAT. The duration of the write back phase is 4 TCL.

During the write back phase, the conversion C-net is precharged with approximately $V_{AREF} / 2$.

Note: Because of parasitic capacitances caused by the pads and the analog multiplexer, the precharge voltage at the pins can differ from $V_{AREF} / 2$.

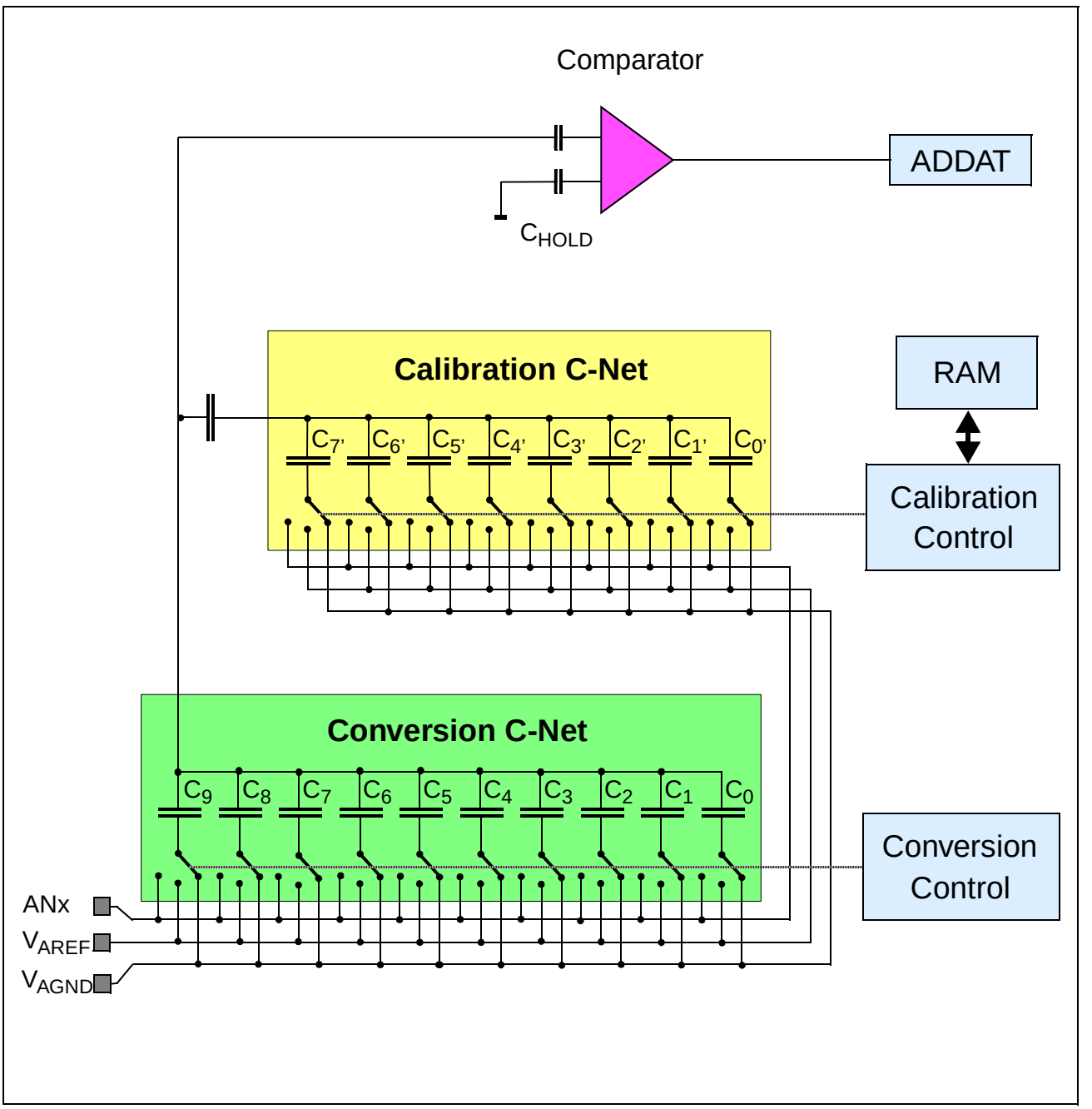


Figure 8 **Block Diagram for the analog Part of a 10-bit A/D Converter with Calibration and Conversion C-Nets**

4 Calibration Mechanism (Error Correction)

An automatic self-calibration mechanism is implemented in the A/D-converter in order to compensate the offset error and to balance differences in the capacitive network. This is due to production variations, which can cause linearity deviations of the A/D conversion. The self-calibration mechanism consists of the calibration capacitor-net, the calibration RAM and the calibration control unit; See **Figure 8**. The self-calibration includes two kinds of calibrations:

- **Offset Calibration** is the adjustment of the offset error.
- **Linearity Calibration** is the binary weight adjustment between the capacitors of the conversion capacitor-net.

4.1 Calibration Principle

The additional correction capacitor-net (calibration C-net) is used to add/subtract a capacitive charge to the comparator input of the A/D converter. This correction C-net allows an adjustment in the range of ± 4 LSB with a resolution of 1/32 LSB within ± 128 steps.

The same calibration C-net is used for both the offset and the linearity calibrations. During offset calibration, the corrective charge, in order to zero-adjust the comparator, is determined. During linearity calibration, for each of the binary weighted capacitors of the conversion C-net, a correction value (with respect to the sum of the remaining capacitors) is determined.

The results of the calibration are stored in the calibration RAM. During normal conversion, the stored values are used to correct the measurement. For this purpose, the calibration control unit is used to calculate the appropriate combination of the calibration capacitors.

4.2 Reset Calibration

After a reset, the contents of the calibration RAM is cleared and the A/D converter automatically starts an initial full calibration sequence (power-up calibration). Both the offset and the linearity deviations are adjusted. This calibration sequence has a duration of $3328*t_{BC}$ (0.66 msec @ f_{CPU} = 20 MHz with the reset values of register ADCON). During the first quarter of this calibration sequence, a coarse adjustment with steps from 0.5 LSB down to 0.1 LSB is performed, which becomes more precise during the following three quarters of the sequence with calibration steps of 0.03 LSB. This scheme, guarantees a very fast reduction of the offset and linearity error.

Note: After reset the positive and negative analog reference voltages (V_{AREF} and V_{AGND}) have to be stable and within the specified range, in order to perform a correct reset calibration.

Note: The reset calibration can be interrupted by any conversion. In this case, the reset calibration is lengthened by the conversion time. The calibration sequence is performed with the actual values of register ADCON. A change of bit field ADCTC (A/D Conversion Time Control) also changes the duration of the calibration sequence.
During the reset calibration sequence the specified maximum TUE can be exceeded.

Note: When entering IDLE or Slow Down Mode, before reset calibration is finished, the reset calibration continues until it is finished. In this case, the Power Down current increases. It is recommended to wait until reset calibration is finished, before entering IDLE or Slow Down Mode.

4.3 Normal Calibration

During A/D converter operation, a re-calibration is performed after each conversion, in order to perform an adaptation to changing operation conditions, e.g. temperature. This re-calibration is performed in single steps, where a maximum change of ± 1/32 LSB of the calibration value is possible.

4.4 Disturbance Filtering

Due to the way the calibration operation is implemented, a filtering of disturbances during the calibration is achieved. For example noise on V_{AREF} or V_{AGND} can disturb calibration, but instead of performing a full correction of a detected deviation (either offset or linearity) in one cycle, the calibration circuit performs a step-by-step reduction of the deviation. Thus, if during one calibration cycle a deviation caused by a disturbance is detected, the last correction value will only be incremented or decremented by one (1/32 LSB). As an example, if the disturbance would cause an offset deviation of 1 LSB, then 32 calibration steps would be necessary to correct for this error. If, however, a deviation occurs during one calibration cycle, but has vanished during the next calibration cycle, the previous change of the correction value will be cancelled again. In other words, a wrong calibration caused by disturbances can only occur if the disturbance lasts for a long time.
Also, disturbances occurring during the reset calibration will be eliminated due to the long calibration sequence and the re-calibration after each conversion.

5 Analog Input AN0 ... ANy

Each application, where an analog voltage has to be measured, needs an accurate calculation of the involved external elements. This is fundamental to ensure the sufficiently charging of the A/D converter input capacitance C_{AIN} to the same potential of the analog source, during the sample time. An insufficient charging of C_{AIN} causes an additional inaccuracy ($Error_{ANx}$) to the TUE of the A/D converter.

This chapter shows how to calculate the external circuits for the analog inputs. The derivation of the necessary formulas is followed by calculation examples.

Because of the different phases of a total conversion (sample- and charge-redistribution time) the calculation examples are shared into different electrical models which fit best to the values of the used external circuits.

The basis for the way of proceeding is the voltage waveform of analog input ANx which can be observed during a conversion.

Note: A detailed solution of the calculation without a simplified electrical model leads to a 2nd order differential equation and will not be discussed in the ApNote.

5.1 Electrical Model of the A/D Converter Input

Figure 9 is a strongly simplified block diagram of the A/D converter. The block diagram includes only the relevant elements necessary for a calculation of the external circuits.
The A/D converter input capacitance C_{AIN} contains the capacitors of the conversion C-net and all parasitic capacitors which have to be considered for the calculation. The A/D converter input capacitance C_{AIN} is specified in the A/D converter characteristics in the Data Sheet. The value of the actual design steps is C_{AIN_max} = 33 pF. Please refer to the Data Sheet for the exact value of the used microcontroller.
R_{AIN} is the internal series resistance of the A/D converter. The value is R_{AIN} = 250 Ω. This value is not explicitly in the Data Sheet, but implicitly in the formula for the calculation of the internal resistance of the analog source R_{ASRC}. The sample switch represents an analog switch closed only during sample time. The multiplexer connects the selected analog input ANx with the internal conversion C-net.

The external capacitance C_{EXT} can be a real external capacitor for noise reduction or only the parasitic capacitance caused by the signal line between analog source and A/D converter input.

The analog voltage source is represented by an ideal voltage source V_0 and a series resistance R_{ASRC}.

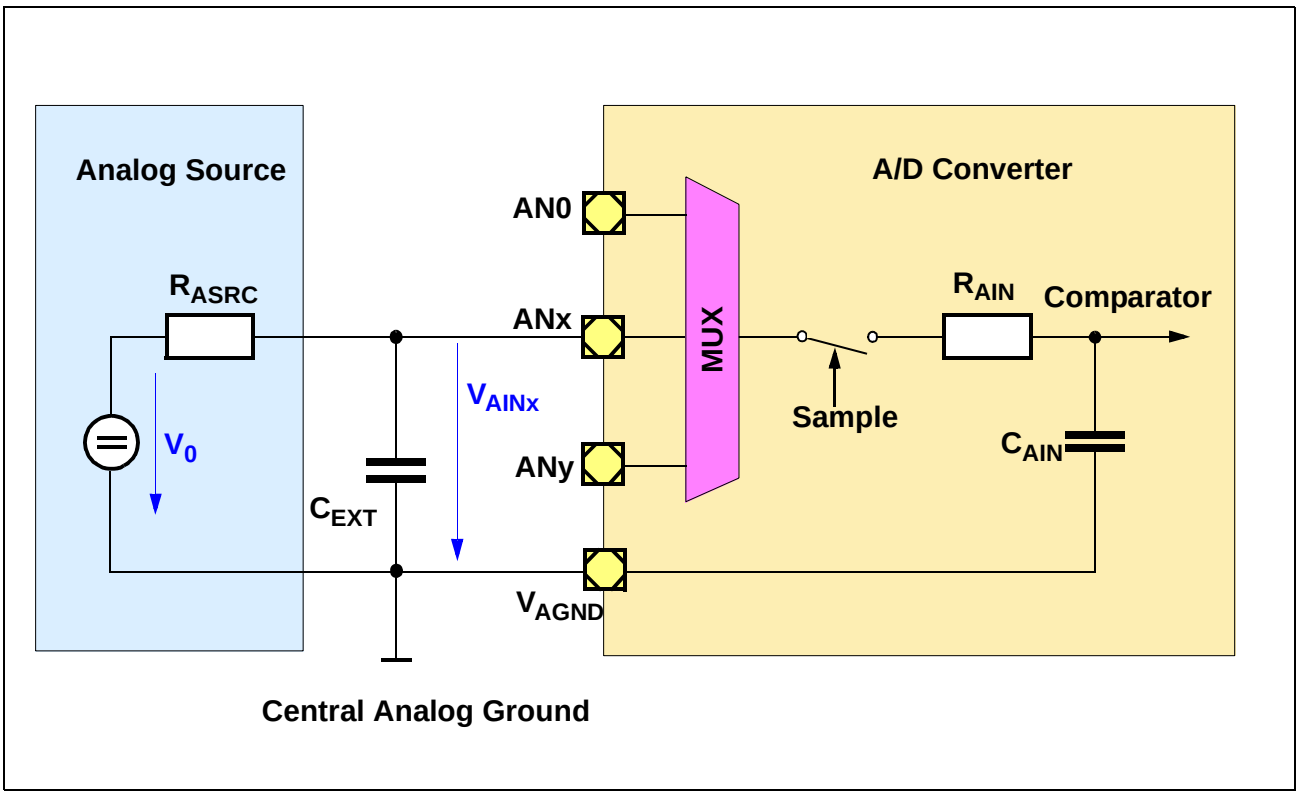


Figure 9 Block Diagram of A/D Converter and Analog Source

5.2 Accuracy at Sample Time

As already described in chapter "Principle of Conversion", a total conversion is divided in two phases: the sample phase and the charge-redistribution phase. The total accuracy of the A/D converter result depends on the TUE, the accuracy of V_{AREF} and the voltage level difference between analog source V_0 and V_{CAIN} ($Error_{ANx}$) at the end of the sample phase. A detailed consideration of the voltage level at C_{AIN} (or ANx, respectively) is the condition to determine the correct values for R_{ASRC}, C_{EXT}, sample time and cycle time of a system.
The worst case voltage deviation for the system is the maximum voltage difference between the precharge voltage of C_{AIN} (approximately V_{AREF} / 2) and V_0 at the beginning of the sample phase. This case is given for $V_0 = V_{AREF}$ or $V_0 = V_{AGND}$. **Figure 10** shows the absolute voltage difference between V_0 and C_{AIN} ($|V_0 - V_{AREF} / 2|$) at the beginning of the sample phase.

The formulas in this ApNote are all related to the possible absolute maximum $V_0 = V_{AREF}$. The result can also be transformed to $V_0 = V_{AGND}$. Voltages used in the calculations are all referred to V_{AGND}.

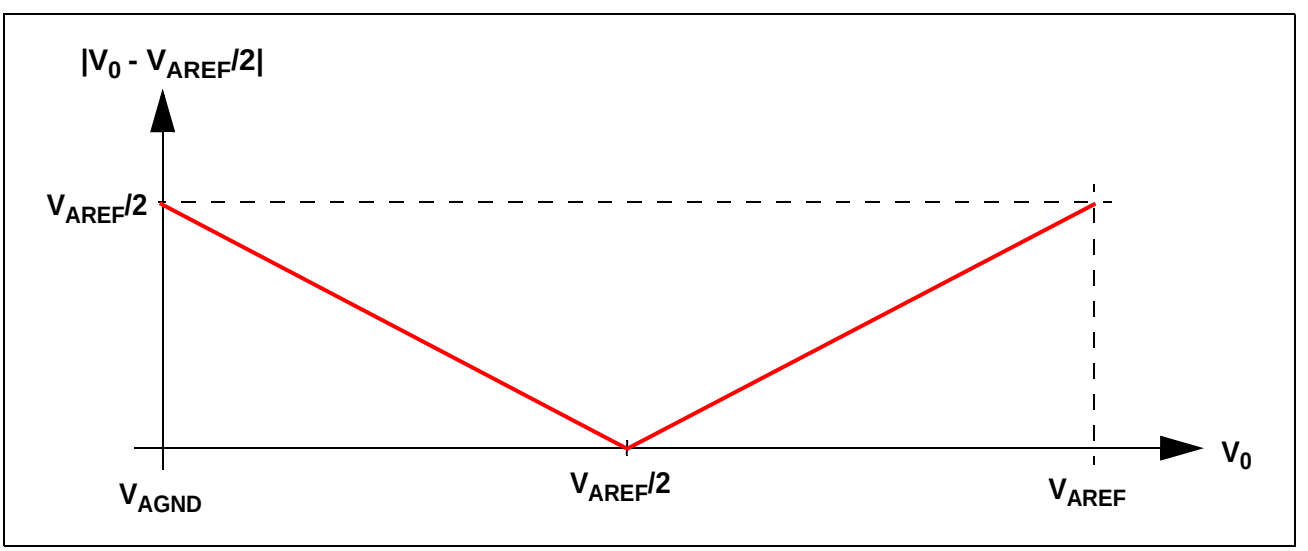


Figure 10 Voltage Difference between V_0 and C_{AIN} ($|V_0 - V_{AREF} / 2|$) at the Start of the Sample Time

Note: The assumed error ($Error_{ANx}$) used in this chapter ("Analog Input AN0 ... ANy") for the calculation examples is referred to the allowed maximum input voltage at ANx ($V_{AINx} = V_{AREF}$). For input voltages at ANx smaller than V_{AREF} the additional inaccuracy at V_{AINx} is proportional less than the value of $Error_{ANx}$ used in the example calculations. The real additional inaccuracy at V_{AINx} is:
$Error_{ANx\_real} = (V_{AINx} / V_{AREF}) * Error_{ANx}$
with the condition $V_{AGND} \leq V_{AINx} \leq V_{AREF}$

5.3 Charge Flow during Sample Time

The input impedance of the A/D converter is mainly capacitive (C_{AIN}) with a small resistive (R_{AIN}) part. This capacitance, however, applies only to the selected analog input pin ANx during the sample time. During the remaining time, the inputs are extremely high impendance (e.g. typical leakage currents are in the range of some 10 nA). See specification in the Data Sheet: Input leakage current of the ADC.
During the sample phase, two different sequential processes are running. First, C_{AIN} is charged from C_{EXT} and the voltages at C_{AIN} and C_{EXT} get the same value. Secondly, the common voltage at C_{AIN} and C_{EXT} is adjusted to V_0 via the resistance of the analog source R_{ASRC}. Depending on the performed phases of the A/D converter different time constants τ have to be considered:

- τ_1 : Time constant at the beginning of the sample time.
  It contains C_{AIN}, C_{EXT} and R_{AIN}
- τ_2 : Time constant during sample time. It contains C_{AIN}, C_{EXT} and R_{ASRC}
- τ_3 : Time constant during and after charge-redistribution phase.
  It contains C_{EXT} and R_{ASRC}

5.3.1 Charge Balance between C_{AIN} and C_{EXT}

The electrical model for τ_1 is shown in **Figure 11**. The voltage at C_{AIN} before switch Sample is closed, is approximately $V_{AREF}/2$ because of precharging C_{AIN} at the end of conversion. The voltage at C_{EXT} is nearly V_0 depending on the cycle time of the conversion.

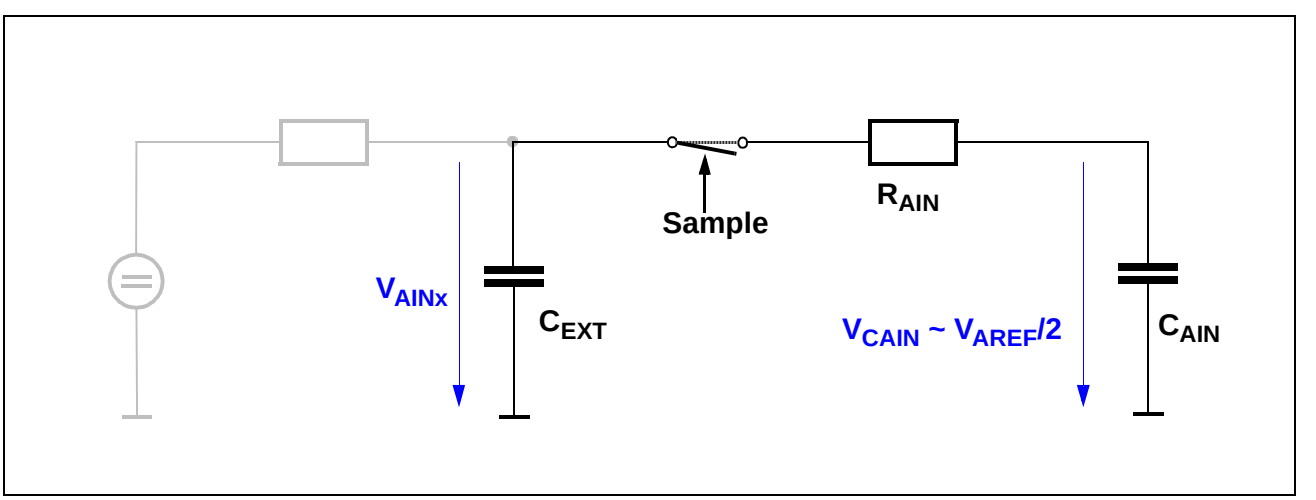


Figure 11 Electrical Model of the A/D Converter during τ_1

When switch Sample is closed, then a charge balance between C_{AIN} and C_{EXT} is done with the time constant τ_1; See **Figure 11**. **Figure 13** presents the corresponding waveform at ANx.

$$\tau_1 = R_{AIN} \cdot \left(\frac{C_{AIN} \cdot C_{EXT}}{C_{AIN} + C_{EXT}} \right)$$

The possible maximum value is τ_1 = 8.25 ns @ C_{AIN} = 33 pF and C_{EXT} = infinite, because R_{AIN} and C_{AIN} are fixed values of the A/D converter. For the calculation of the sample time, which is in the range of some µs, the duration of time constant τ_1 is in most cases negligible (after 7.6*τ the voltage error is less than 0.5 LSB). For typical values of 7.6*τ_1 see **Table 1**.

Table 1 Values for 7.6*τ_1 @ C_{AIN} = 33 pF and R_{AIN} = 250 Ω

C_{EXT}	1 pF	10 pF	100 pF	1 nF	10 nF	100 nF	1 µF
7.6*τ_1	1.84 ns	14.58 ns	47.14 ns	60.70 ns	62.49 ns	62.68 ns	62.70ns

The charge balance between C_{AIN} and C_{EXT} causes a voltage jump V_Δ at the analog input ANx. Depending on the voltage on ANx when the sample phase starts, the voltage can be increased or decreased. The example of **Figure 13** uses the worst case $V_0 = V_{AREF}$. At the end of 7.6*τ_1 the voltage at ANx is reduced (or increased) by the value V_Δ with an accuracy of 0.5 LSB. The charge balance between C_{EXT} and C_{AIN} results in the formula for V_Δ:

$$V_\Delta = \frac{C_{AIN} \cdot (V_0 - V_{CAIN})}{C_{AIN} + C_{EXT}}$$

Table 2 Typical Values for the Voltage Jump V_Δ @ C_{AIN} = 33 pF, Precharge: V_0 - V_{CAIN} = 2.5 V and V_0 = V_{AREF}

C_{EXT}	1 pF	10 pF	100 pF	1 nF	10 nF	100 nF	1 µF
V_Δ	2.4 V	1.9 V	0.6 V	80 mV	8.2 mV	0.8 mV	0.08 mV

5.3.2 Charge of C_{AIN} and C_{EXT} via R_{ASRC}

The electrical model during sample time with τ_2 is shown in **Figure 12**. In this electrical model R_{AIN} is neglected because in typical systems R_{ASRC} >> R_{AIN}. The voltage at C_{AIN} and C_{EXT} is defined by V_0 and V_Δ at the beginning of the second phase ('start-voltage' = V_0 - V_Δ).

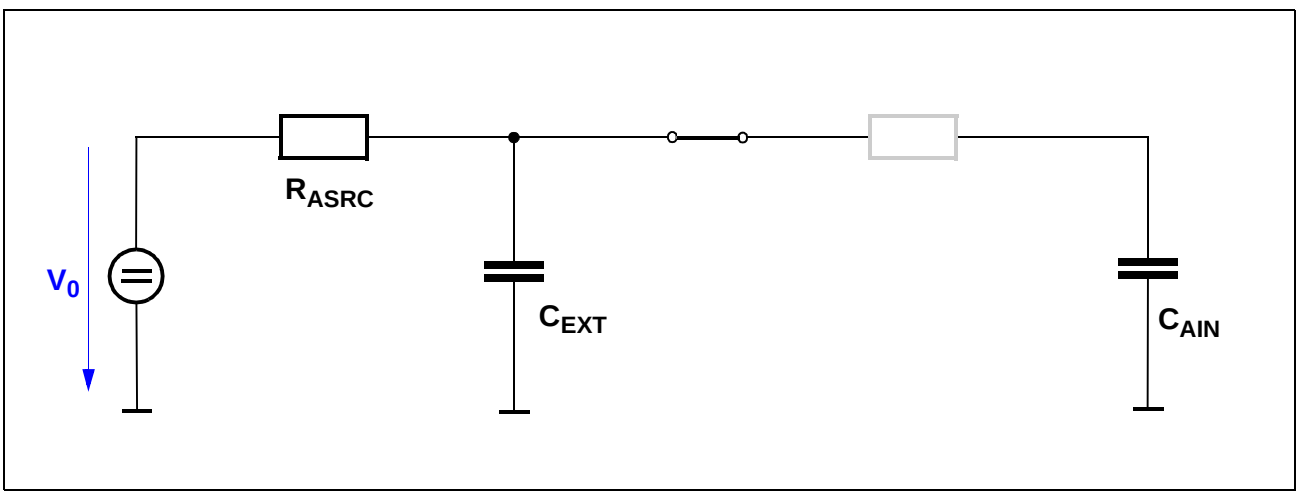


Figure 12 Electrical Model of the A/D Converter during τ_2

After V_Δ has reached the absolute maximum value, C_{EXT} and C_{AIN} are charged via R_{ASRC} from V_0 with the time constant τ_2.

$$\tau_2 = R_{ASRC} \cdot (C_{AIN} + C_{EXT})$$

5.4 R_{ASRC} Calculation with (0 pF < C_{EXT} < (2^r - 1) * C_{AIN})

For reliable results it must be assured that during the sample time the input capacitance C_{AIN} is completely charged to the desired value, which is then digitized by the converter. Under worst case conditions this capacity must be charged or discharged by the half input voltage when $V_0 = V_{AREF}$ or $V_0 = V_{AGND}$.

The input capacitance C_{AIN} of the A/D converter, the external capacitance C_{EXT} and the resistance of the analog source R_{ASRC} form an RC lowpass filter, which has the charging function $V_S(t)$. In normal systems, the sample time $t_S >> \tau_1$, therefore τ_1 is neglected in the formula for $V_S(t)$. The waveform is shown in **Figure 13**.

$$V_S(t) = V_{AREF} - V_\Delta \cdot e^{\frac{-t}{\tau_2}}$$

The voltage on ANx at the end of the sample time can also be described with the formula $V_S(t_S)$. The $Error_{ANx}$ describes the maximum allowed deviation between the voltage on ANx and V_0 when the sample time is finished. An assumed $Error_{ANx}$ of 0.5 LSB is equivalent to 9.76 mV / 2.44 mV / 0.61 mV @ V_{AREF} = 5 V and 8-bit / 10-bit / 12-bit A/D converter resolution.

$$V_S(t_S) = V_{AREF} - Error_{ANx}$$

Now it is possible to calculate the maximum value of the analog source resistance R_{ASRC}. The formula for R_{ASRC} assumes that R_{AIN} = 0 Ω.

$$R_{ASRC} = \frac{t_S}{(C_{AIN} + C_{EXT}) \cdot \ln \frac{V_\Delta}{Error_{ANx}}}$$

The formula is only valid for: $V_\Delta / Error_{ANx} > 1$
An assumed maximum $Error_{ANx}$ = LSB / 2 leads to $C_{EXT} < (2^r - 1) * C_{AIN}$

Depending on the A/D converter resolution the relations between C_{EXT} and C_{AIN} for the calculation of R_{ASRC} are:

8-bit resolution:	0 pF < C_{EXT} < 255 * C_{AIN}
10-bit resolution:	0 pF < C_{EXT} < 1023 * C_{AIN}
12-bit resolution:	0 pF < C_{EXT} < 4095 * C_{AIN}

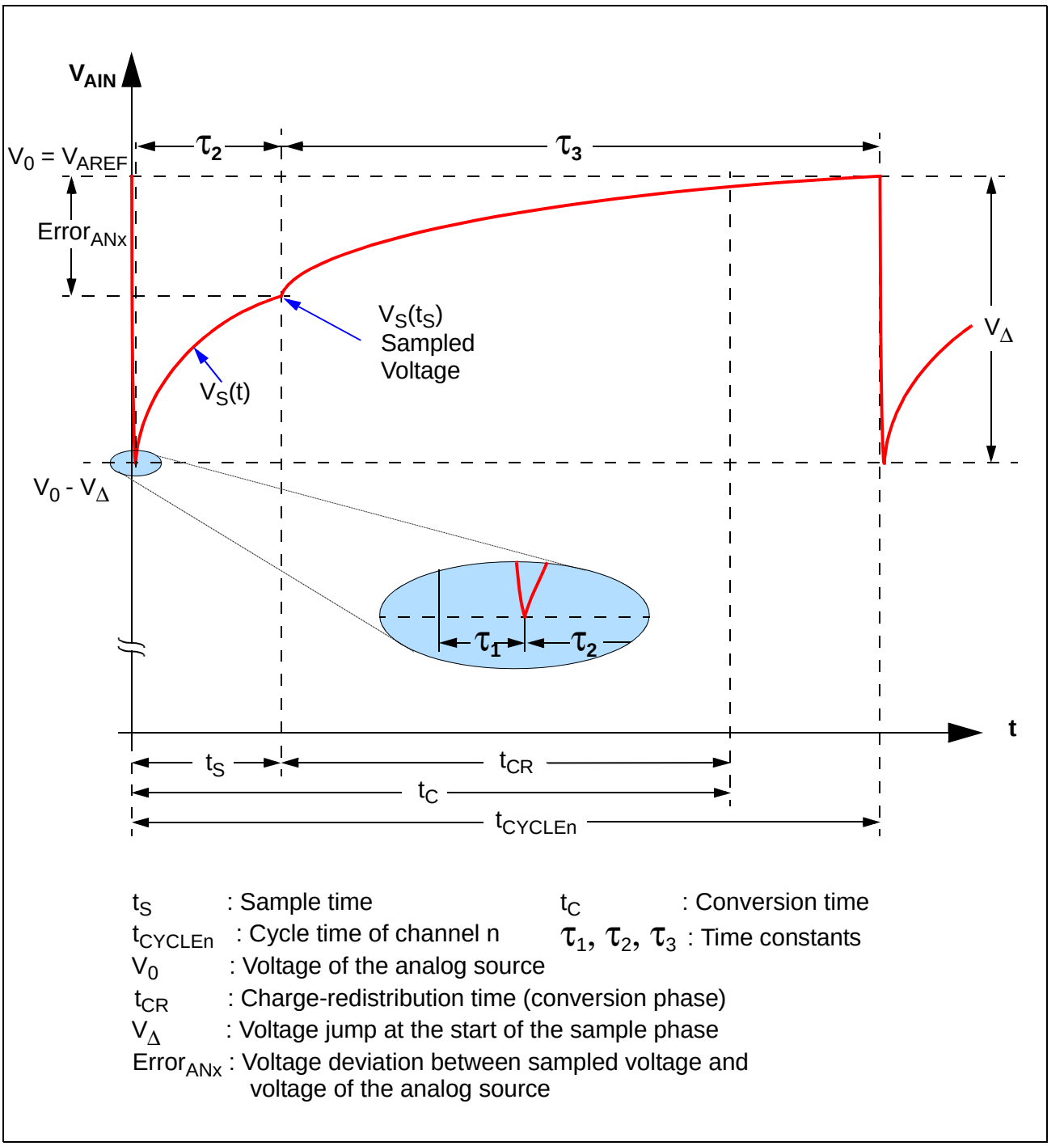


Figure 13 Voltage Waveform at ANx

5.4.1 Charge-Redistribution Time

During the charge-redistribution time, the Sample switch is open and the external capacitance C_{EXT} is charged via the resistor of the analog source R_{ASRC}.

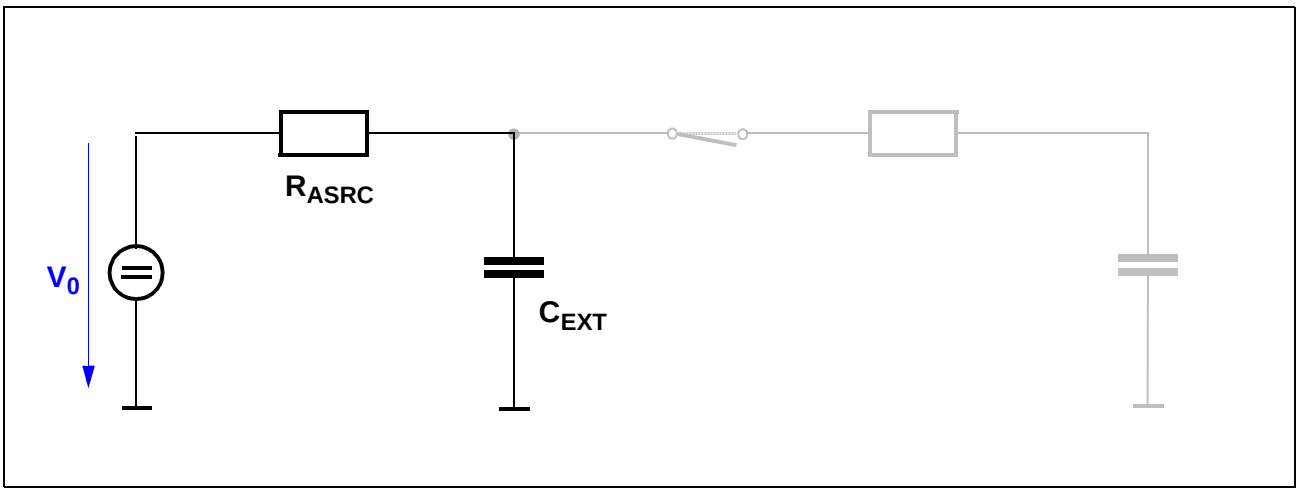


Figure 14 Electrical Model of the A/D Converter during τ_3

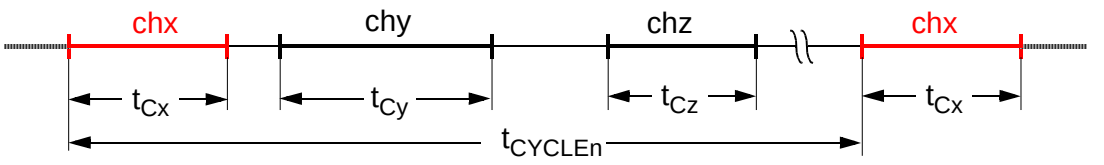
The time constant during and after charge-redistribution time is τ_3.

$$\tau_3 = R_{ASRC} \cdot C_{EXT}$$

While the external capacitance C_{EXT} is charged via R_{ASRC}, the A/D converter performs the successive approximation (charge-redistribution). This is the transformation of the analog voltage into a digital value. The reference for the transformation is the reference voltage at pin V_{AREF} referred to V_{AGND}. It is very important for an exact conversion result to hold the reference voltage and the reference ground on a constant level during the charge-redistribution time. More details can be found in the chapter "Reference Voltage V_{AREF} and V_{AGND}".

5.4.2 Cycle Time

The cycle time t_{CYCLEn} is the duration from the start of a conversion to the next conversion start of the same analog channel. The figure below shows the relation between the conversion time of an analog channel and the cycle time.



t_{Cn} : Conversion time of analog channel n
t_{CYCLEn} : Cycle time of analog channel n
chn : analog channel n

Figure 15 Cycle Time

For continuous conversion mode of a channel, the conversion time t_C can be equal to the cycle time t_{CYCLEn}. The cycle time of consecutive conversions is important for the calculation of the voltage on C_{EXT} at the start of next conversion. The voltage difference between the analog source V_0 and the analog input ANx at the start of a conversion should be 0 V or negligible. The recommendation is:

$$t_{CYCLE} \geq 7.6 \cdot \tau_3 + t_S$$

*Note: After 7.6 * τ_3 the remaining deviation from V_0 is 0.049% of the assumed $Error_{ANx}$ for $V_S(t_S)$.*

5.4.3 Calculation Example with ($0 pF < C_{EXT} < (2^r - 1) * C_{AIN}$)

The assumed values used in the example are:

C_{AIN} = 33 pF, t_S = 1.28 µs, $V_{AREF} = V_0 = 5$ V,
R_{AIN} = 250 Ω, t_C = 7.8 µs, r = 10 (10-bit resolution),
C_{EXT} = 200 pF,
$Error_{ANx} = 0.5\ LSB_{10} = V_{AREF} / 2048 = 2.44$ mV

The calculation results in the values for R_{ASRC} and t_{CYCLEn}.

5.4.3.1 Resistance of the Analog Source R_{ASRC}

First the voltage jump V_Δ during the sample phase is calculated:

$$V_\Delta = (C_{AIN} * (V_{AREF} - V_{AREF}/2)) / (C_{AIN} + C_{EXT})$$
$$V_\Delta = (33\ pF * (5\ V - 2.5\ V)) / (33\ pF + 200\ pF)$$
$$V_\Delta = 354\ mV$$

The allowed maximum resistance of analog source R_{ASRC} is:

$$R_{ASRC} = t_S / ((C_{AIN} + C_{EXT}) * \ln(V_\Delta / Error_{ANx}))$$
$$R_{ASRC} = 1.28\ \mu s / ((33\ pF + 200\ pF) * \ln(354\ mV / 2.44\ mV))$$
$$R_{ASRC} = 1103\ \Omega$$

The table below shows the different results of R_{ASRC} with the assumed values used in the example.

Table 3 Maximum Values for R_{ASRC} and different C_{EXT}

C_{EXT}[pF]	1	20	40	60	80	100	150	200	250	500	1000	10000
R_{ASRC} [kΩ]	5.4	3.7	2.9	2.3	2.0	1.7	1.3	1.1	0.9	0.6	0.35	0.1

*Note: The capacitive load at the analog inputs ANx should be as small as possible because it reduces the allowed resistance of the analog source R_{ASRC}; See **Table 3**. The only exception is the use of a very high external capacitance, which supplies the A/D converter with the necessary charge during the sample phase.*

5.4.3.2 Cycle Time t_{CYCLEn}

The recommended minimum value of the cycle time is

$$t_{CYCLEn} = 7.6 * R_{ASRC} * C_{EXT} + t_S$$
$$t_{CYCLEn} = 7.6 * 1103\ \Omega * 200\ pF + 1.28\ \mu s$$
$$t_{CYCLEn} = 2.95\ \mu s$$

The calculated cycle time is smaller than the conversion time and, in that case, continuous conversion of this analog channel is possible without inserting a waiting period to charge the external capacitance C_{EXT}.

5.5 R_{ASRC} Calculation with ($C_{EXT} > (2^r - 1) * C_{AIN}$)

The selected external capacitance has to be high enough so the total charge, which is necessary to load the internal C-net (C_{AIN}) of the A/D converter, is supplied by the external capacitor C_{EXT}. The considerations below include the value of the external capacitance C_{EXT} with respect to the assumed maximal $Error_{ANx}$ caused by the C_{EXT} and the necessary time t_{CYCLEn} to reload the external capacitor.

5.5.1 External Capacitance C_{EXT}

The calculation of the external capacitance C_{EXT} is based on the assumption that $V_{AREF} - V_{\Delta}$ is the sampled voltage and V_{Δ} is the maximum allowed $Error_{ANx}$; See **Figure 16**. After the charge balance (voltage jump, V_{Δ}) the voltage change at the capacitors during the sample phase is extremely small because of the high time constant τ_3 of the external capacitance and the resistance of the analog source.
The example is calculated with the assumption of a maximum allowed error, $Error_{ANx} = LSB_r / 2$.

$$Error = LSB_r / 2$$
$$Error = V_{AREF} / (2^r * 2)$$
$$Error > V_{\Delta} = (C_{AIN} * (V_{AREF} - V_{AREF}/2)) / (C_{AIN} + C_{EXT})$$

$$C_{EXT} > (2^r - 1) * C_{AIN}$$

Depending on the A/D converter resolution the relations between C_{EXT} and C_{AIN} for the calculation of R_{ASRC} are:

8-bit resolution:	$C_{EXT} > 255 * C_{AIN}$
10-bit resolution:	$C_{EXT} > 1023 * C_{AIN}$
12-bit resolution:	$C_{EXT} > 4095 * C_{AIN}$

The condition $C_{EXT} > (2^r - 1) * C_{AIN}$ allows a free choice of the sample time t_S without consideration of the resistance of the analog source R_{ASRC} but R_{ASRC} has a direct influence on the cycle time t_{CYCLEn} of the conversion.

5.5.2 Cycle Time t_{CYCLEn}

The calculation of the cycle time takes into account that the external capacitor is not totally charged to the voltage of the analog source V_0 (worst case $V_0 = V_{AREF}$ or $V_0 = V_{AGND}$) but a small voltage rest V_R is missing. See **Figure 16**.

With the condition $C_{AIN} << C_{EXT}$ the formula for V_{Δ} can be simplified:

$$V_{\Delta} = (C_{AIN} * (V_{AREF} - V_{AREF}/2)) / (C_{AIN} + C_{EXT})$$
$$V_{\Delta} \sim C_{AIN} * V_{AREF} / 2 * C_{EXT}$$

The condition $V_\Delta + V_R \le Error_{ANx}$ with $V_R = V_{AREF} - V_C(t_{CYCLEn})$ is based on **Figure 16**. The charge curve $V_C(t)$ of the capacitor C_{EXT} via the resistance of the analog source R_{ASRC} is:

$$V_C(t) = V_{AREF} - Error_{ANx} \cdot e^{\frac{-t}{\tau_3}}$$

With an assumed maximum error of LSB_r / 2 ($Error_{ANx} = (V_{AREF} / 2^r) / 2$) and with $\tau_3 = R_{ASRC} * C_{EXT}$ the formulas result in the relation:

$$t_{CYCLE} \ge R_{ASRC} \cdot C_{EXT} \cdot \ln\left(\frac{C_{EXT}}{C_{EXT} - 2^r \cdot C_{AIN}}\right)$$

This formula is only valid for $C_{EXT} > 2^r * C_{AIN}$

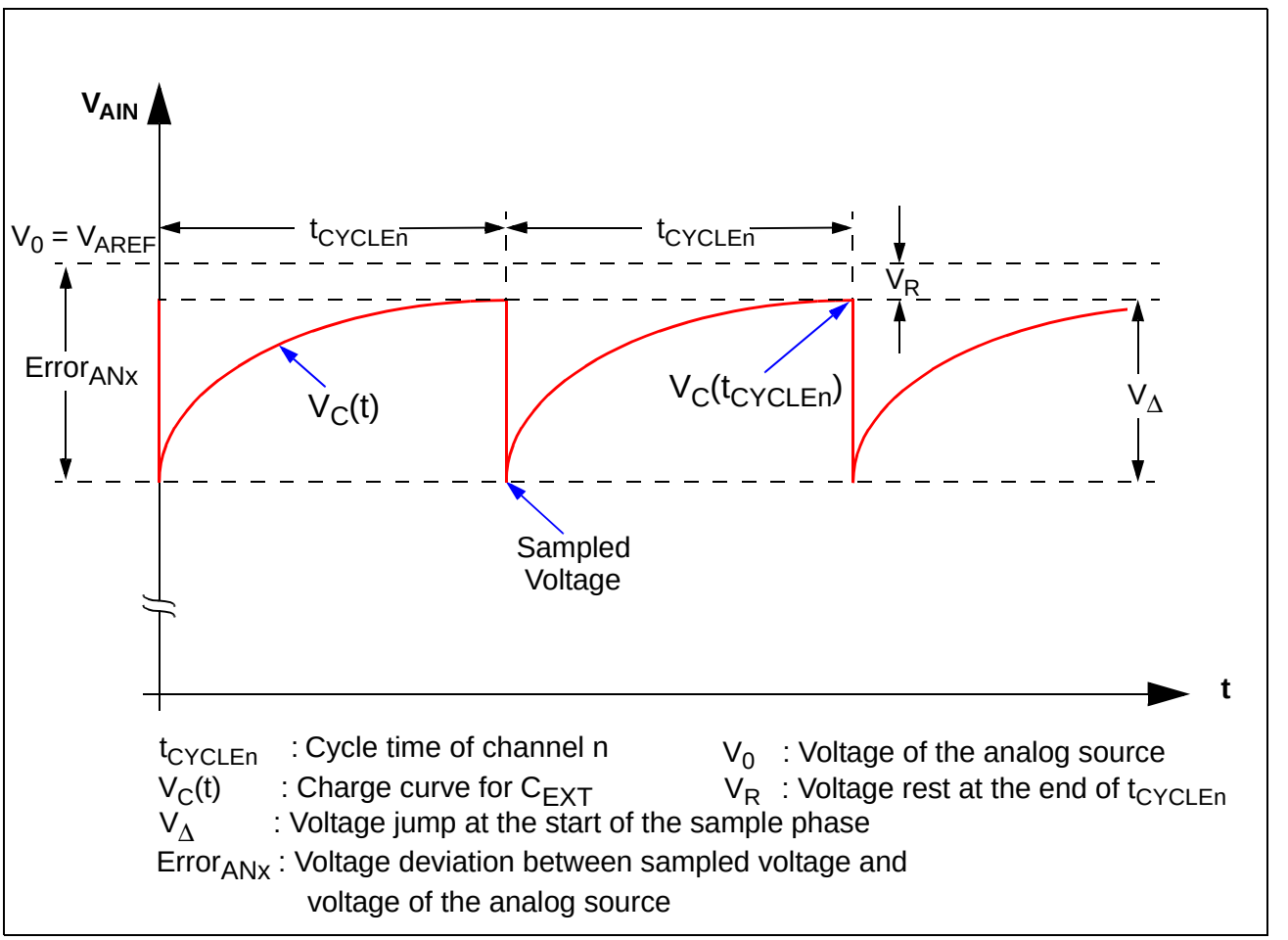


Figure 16 Voltage at C_{EXT} with High Capacitance for Periodical Conversions

5.5.3 Cutoff Frequency f_C

The resistance of the analog source and the external capacitance C_{EXT} act as a low-pass filter with the cutoff frequency f_C. A check is necessary whether the cutoff frequency fits to the frequency of the analog source. If the relation between A/D converter cycle frequency ($f_{CYCLE} = 1 / t_{CYCLEn}$) and the cutoff frequency is $f_{CYCLE} / f_C = 0.1$ then the analog signal is damped with 5 $^{o}/_{oo}$ (~1 LSB).

$$f_C = \frac{1}{2\pi \cdot R_{ASRC} \cdot C_{EXT}}$$

Note: If the external circuit reaches the cutoff frequency then the voltage of the analog source V_0 is damped with the factor -3 dB ($V_{AIN} \sim 0.7 * V_0$ @ cutoff frequency f_C).

5.5.4 Calculation Example with ($C_{EXT} > (2^r - 1) * C_{AIN}$)

The assumed values used in the example are:

C_{AIN}	= 33 pF,	t_S	= 1.28 µs,	$V_{AREF} = V_0 =$	5 V,
R_{AIN}	= 250 Ω,	t_C	= 7.8 µs,	r = 10 (10-bit resolution),	
R_{ASRC}	= 20 kΩ,	C_{EXT}	= 100 nF	($C_{EXT} = 3030 * C_{AIN}$)	

$Error_{ANx} = 0.5\ LSB_{10} = V_{AREF} / 2048 = 2.44$ mV,

The calculation results in the value of cycle time t_{CYCLEn} and cutoff frequency f_C. The values of the external capacitance C_{EXT} and resistance of the analog source R_{ASRC} are in a fixed relation with the cycle time t_{CYCLEn}:

$$t_{CYCLEn} \geq R_{ASRC} * C_{EXT} * \ln(C_{EXT} / (C_{EXT} - 2^r * C_{EXT}))$$
$$t_{CYCLEn} \geq 20\ k\Omega * 100\ nF * \ln(100\ nF / (100\ nF - 2^{10} * 100\ nF))$$
$$t_{CYCLEn} \geq 0.82\ ms$$

The cutoff frequency is calculated via:

$$f_C = 1 / (2 * \pi * R_{ASRC} * C_{EXT})$$
$$f_C = 1 / (2 * \pi * 20\ k\Omega * 100\ nF)$$
$$f_C = 80\ Hz$$

Table 4 includes calculation results of the cycle time in [ms] for different values of C_{EXT} and R_{ASRC} with the assumed values of the example ($Error_{ANx}$ = 0.5 LSB_{10}).

Table 4 Cycle Time t_{CYCLEn} for Different Values of C_{EXT} and R_{ASRC}

t_{CYCLEn} [ms]		C_{EXT} [nF]							
		34	**40**	**50**	**75**	**100**	**500**	**1000**	**10000**
R_{ASRC} [kΩ]	1	0.17	0.07	0.06	0.04	0.04	0.03	0.03	0.03
	5	0.87	0.37	0.28	0.22	0.21	0.17	0.17	0.17
	10	1.73	0.75	0.56	0.45	0.41	0.35	0.34	0.34
	15	2.60	1.12	0.84	0.67	0.62	0.52	0.52	0.52
	20	3.47	1.49	1.13	0.90	0.82	0.70	0.69	0.68
	35	4.33	1.86	1.41	1.12	1.03	0.87	0.86	0.85
	30	5.20	2.24	1.69	1.35	1.24	1.05	1.03	1.02
	40	6.93	2.98	2.25	1.80	1.65	1.40	1.38	1.35
	50	8.66	3.73	2.82	2.25	2.06	1.75	1.72	1.69
	100	17.33	7.45	5.63	4.49	4.12	3.50	3.44	3.38

Table 5 includes calculation results of the cutoff frequency in [Hz] for different values of C_{EXT} and R_{ASRC} with the assumed values of the example ($Error_{ANx}$ = 0.5 LSB_{10}).

Table 5 Cutoff Frequency f_C for Different Values of C_{EXT} and R_{ASRC}

f_C [Hz]		C_{EXT} [nF]							
		34	**40**	**50**	**75**	**100**	**500**	**1000**	**10000**
R_{ASRC} [kΩ]	1	4681	3979	3183	2122	1592	318	159	16
	5	936	796	637	424	318	64	32	3.2
	10	468	398	318	212	159	32	16	1,6
	15	312	265	212	141	106	21	11	1,1
	20	234	199	159	106	80	16	8.0	0.8
	35	187	159	127	85	64	13	6.4	0.6
	30	156	133	106	71	53	11	5.3	0.5
	40	117	99	80	53	40	8.0	4.0	0.4
	50	94	80	64	42	32	6.4	3.2	0.3
	100	47	40	32	21	16	3.2	1.6	0.2

5.6 R_{ASRC} Calculation with (C_{EXT} = 0pF)

In this case, which is in real systems hard to realize, the external capacitance is neglected. The electrical model is shown in **Figure 17**. It can be used for a rough estimation of the external components if the value of C_{EXT} is nearly zero pF. The internal C-net capacitance of the A/D converter is directly charged via R_{ASRC} and R_{AIN}.

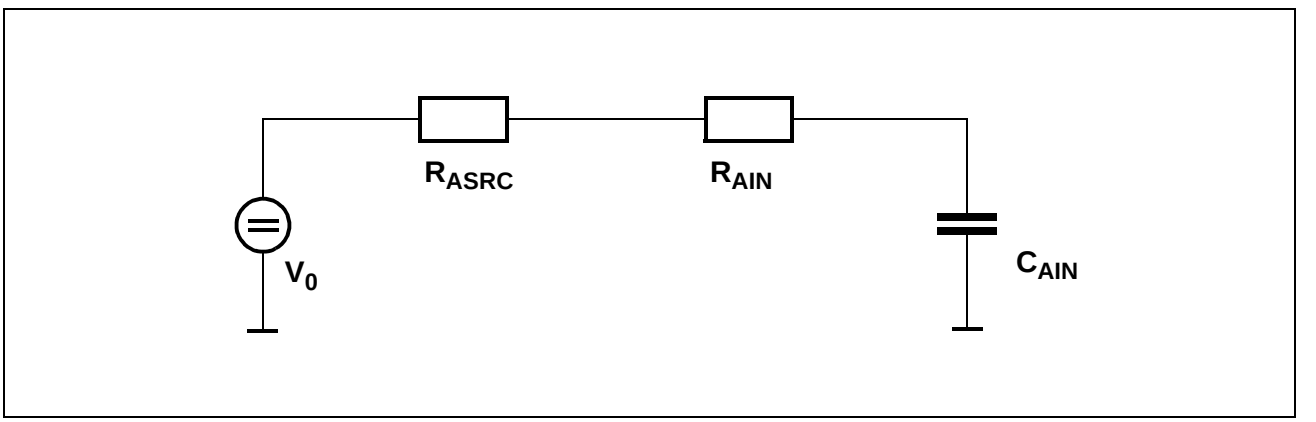


Figure 17 Electrical Model of the A/D Converter during τ_2 with C_{EXT} = 0 pF

5.6.1 Resistance of the Analog Source R_{ASRC}

When the external capacitance is C_{EXT} = 0 pF then time constant τ_1 = 0 s and the maximum voltage jump V_Δ at the beginning of the sample time is approximately $V_{AREF}/2$, equal to the precharge value of the internal C-net.

$$V_\Delta = (C_{AIN} * (V_{AREF} - V_{AREF} / 2)) / C_{AIN}$$
$$V_\Delta = V_{AREF} / 2$$

The resistance of the analog source R_{ASRC}, is calculated via the formula for systems with a small external capacitance but without C_{EXT} and with R_{AIN}.

$$R_{ASRC} = \frac{t_S}{C_{AIN} \cdot \ln \frac{V_\Delta}{Error_{ANx}}} - R_{AIN}$$

The calculation of the cycle time is not necessary because only during sample time, is the internal C-net connected to the analog source. In the other phases of the cycle time, the internal C-net is disconnected from the analog source. Therefore, no capacitance has to be charged via R_{ASRC} until the start of the next sample time.

5.6.2 Calculation Example with (C_{EXT} = 0pF)

The calculation example gives a rough estimation for the allowed maximum of R_{ASRC} if C_{EXT} is nearly zero pF. The assumed values used in the example are:

C_{AIN} = 33 pF, t_S =1.28 µs, V_{AREF} = V_0 = 5 V,
R_{AIN} = 250 Ω, t_C = 7.8 µs, r = 10 (10-bit resolution),
C_{EXT} = 0 pF,
$Error_{ANx}$ = 0.5 LSB_{10} = V_{AREF} / 2048 = 2.44 mV,

The calculation results in the value for R_{ASRC} with $V_\Delta = V_{AREF} / 2$.

$$R_{ASRC} = t_S / (C_{AIN} * \ln(V_\Delta / Error_{ANx})) - R_{AIN}$$
$$R_{ASRC} = 1.28\ \mu s / (33\ pF * \ln(2.5\ V / 2.44\ mV)) - 250\ \Omega$$
$$R_{ASRC} = 5345\ \Omega$$

The table below includes the maximum values for R_{ASRC} and different sample times with the assumed values of the example:

Table 6 Maximum Values for R_{ASRC} and sample Times t_S @ C_{EXT} = 0 pF

t_S [µs]	1	2	3	4	5	6	7	8	9	10
R_{ASRC} [kΩ]	4.1	8.5	12.9	17.2	21.6	26.0	30.4	34.7	39.1	43.5

Note: The leakage current specified in the Data Sheet can have an influence to the accuracy of the analog input voltage, when the values of R_{ASRC} exceeds a certain limit. This limit depends on the allowed inaccuracy referred to V_{AINx} which is given by the system demands. See chapter “Overload and Leakage Current”.

5.6.3 Calculation Example with the Formula in the Data Sheet

The A/D converter Characteristics in the Data Sheet (example for C166 Family) include the formula for the calculation of the maximum 'Internal resistance of analog source'. With t_S in ns and R_{ASRC} in kΩ the formula is:

$$R_{ASRC} \leq t_S / 450 - 0.25$$

This formula in the C166 Family Data Sheets is based on the assumption, that the analog input ANx is only loaded with a small external parasitic capacitance: $C_{EXT} < 65$ pF. For systems with an external capacitance, which exceeds this value, the external components have to be calculated as shown in the previous chapters.

The table below includes the maximum values for R_{ASRC} calculated with the formula in the Data Sheets of the C166 Family.

Table 7 Maximum Values for R_{ASRC} and sample Times t_S @ C_{EXT} = 65 pF

t_S [µs]	1	2	3	4	5	6	7	8	9	10
R_{ASRC} [kΩ]	2.0	4.2	6.4	8.6	10.9	13.1	15.3	17.5	19.8	22.0

Note: The leakage current specified in the Data Sheet can have an influence to the accuracy, see note at **Table 6***.*

6 Reference Voltage V_{AREF} and V_{AGND}

During the charge-redistribution phase, and also during the calibration phase, each group of capacitors from the C-net is individually switched to either V_{AREF} or V_{AGND}. Because of this switching and the according charge transfers in the C-net, the A/D converter requires a dynamic current at pin V_{AREF}.

Thus, the resistance of the voltage reference source has to be low enough to supply the current for the charge-redistribution- and calibration phase. The external circuit at V_{AREF} has a direct influence to the required resistance of the voltage reference. If an external capacitance C_{AREF}, between V_{AREF} and V_{AGND}, is used then the voltage reference has to supply a small continuous current to charge the external capacitor. The necessary peak current during the charge-redistribution phase is supplied by the external capacitance C_{EXT}. The continuous current and the charge duration (t_{CYCLE}) have to be high enough to fill the external capacitance to a sufficient voltage level before the next charge-redistribution phase starts.

If there is no external capacitance between V_{AREF} and V_{AGND} then the voltage reference has to supply the peak current directly. The maximum allowed resistance R_{AREF} between the voltage reference V_{RF} and V_{AREF} using no external capacitance C_{AREF} is specified in the Data Sheets of the C500/C166 Family.

The specified value for R_{AREF} in the Data Sheet is the worst case for the calculation of the minimum sourcing peak current, which has to be supplied by the voltage reference.

$$I_{AREF} \geq \frac{V_{RF}}{R_{AREF}}$$

6.1 Sources for the Voltage Reference

Depending on the system demands, several different kinds of voltage references can be used in a system. The supply voltage of the microcontroller can be selected for the reference voltage, but the accuracy is in percentage range. The accuracy of an external high precision voltage reference is in the per mille range.

6.1.1 Supply Voltage of the Microcontroller

In most systems, the voltage reference used for the A/D converter is the supply voltage V_{DD} of the microcontroller. The typical accuracy of voltage regulators is 2 %; See power semiconductor family TLE42xx from Infineon Technologies.
When using the digital supply voltage of the microcontroller, it is recommended to insert a low pass filter between V_{DD} and V_{AREF} for the voltage reference; See figure below. The low pass filter suppresses noise on pin V_{AREF} to improve the accuracy of the A/D converter results.

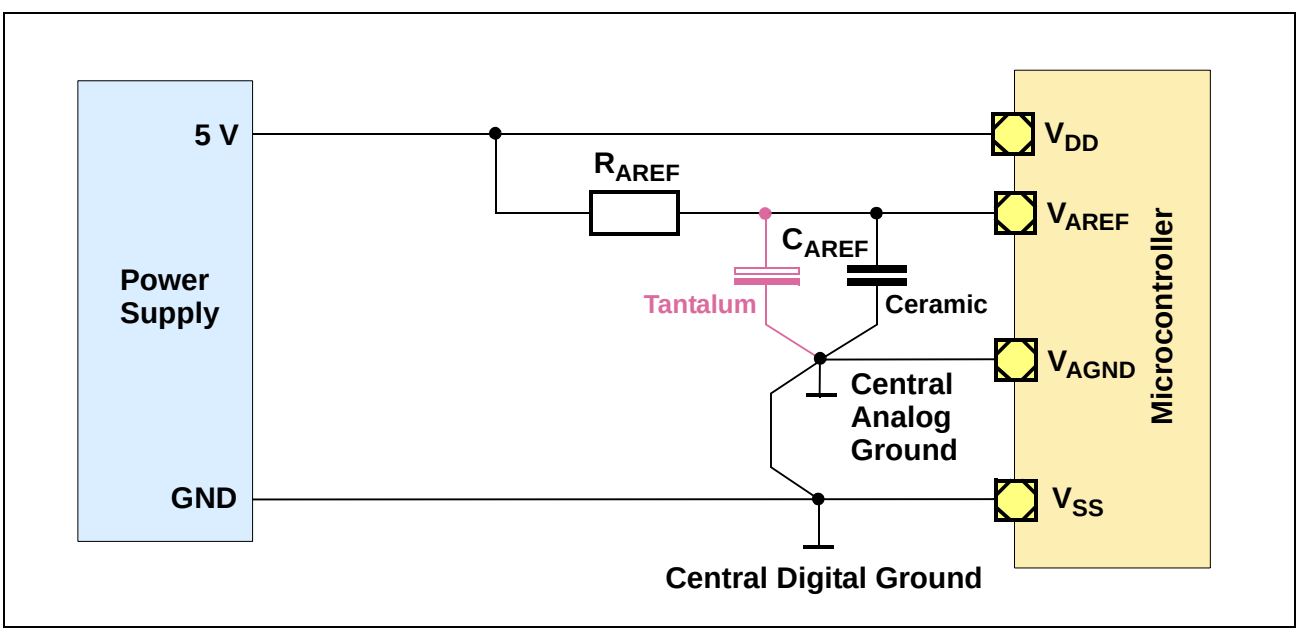


Figure 18 Supply Voltage used for Voltage Reference

The values of the capacitance C_{AREF} and the resistor R_{AREF} depend on the characteristics of the system. Typical values are R_{AREF} = 47 Ohm and C_{AREF} = 100 nF @ r = 10 and C_{AIN} = 33 pF. The cutoff frequency of this low pass filter is f_C = 34 kHz. If there is noise on the system supply voltage with a very low frequency, then the cutoff frequency can be reduced via an appropriate tantalum capacitance in parallel to C_{AREF}, which stabilizes the voltage reference.

Note: The impedance and the noise caused by the connection between Central Analog Ground and Central Digital Ground should be as low as possible.

6.1.2 External Voltage Reference

The source for an external voltage reference can be a standard supply voltage with increased accuracy or with less noise. For systems where a high accuracy is demanded, high precision voltage reference can be used with a typical accuracy in the range of 2.5 mV ... 20 mV.

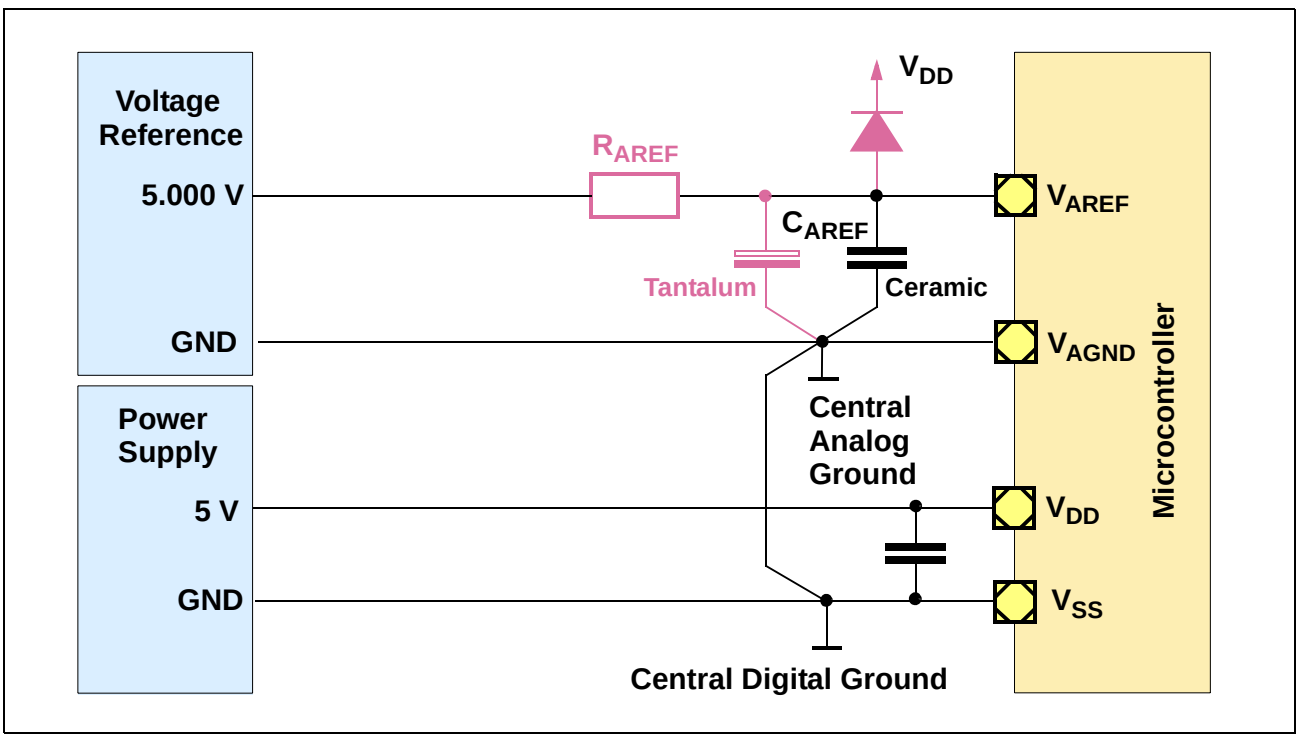


Figure 19 External Voltage Reference

*Note: If the supply voltage of the microcontroller and the voltage reference of the A/D converter are switched on and off at different times, then it is very important that the voltage reference is switched on or off only when the supply voltage of the microcontroller is **on** otherwise the voltage reference supplies the system with current via the ESD clamp diode. In that case, it is necessary to reduce the overload current to the specified absolute maximum ratings; See chapter overload and leakage current. The overload current can be reduced via a resistor or a diode. If the additional external clamp resistor causes an unacceptable additional error at V_{AREF} then an external clamp diode should be used.*

6.2 R_{AREF} Calculation Including an External Capacitance

The calculation is based on the assumption that there is an external capacitance C_{AREF} between V_{AREF} and V_{AGND}. The selected external capacitance has to be high enough that the total charge, which is necessary to load the internal C-net (C_{AIN}) for a total conversion phase, is supplied by the external capacitor C_{AREF}.

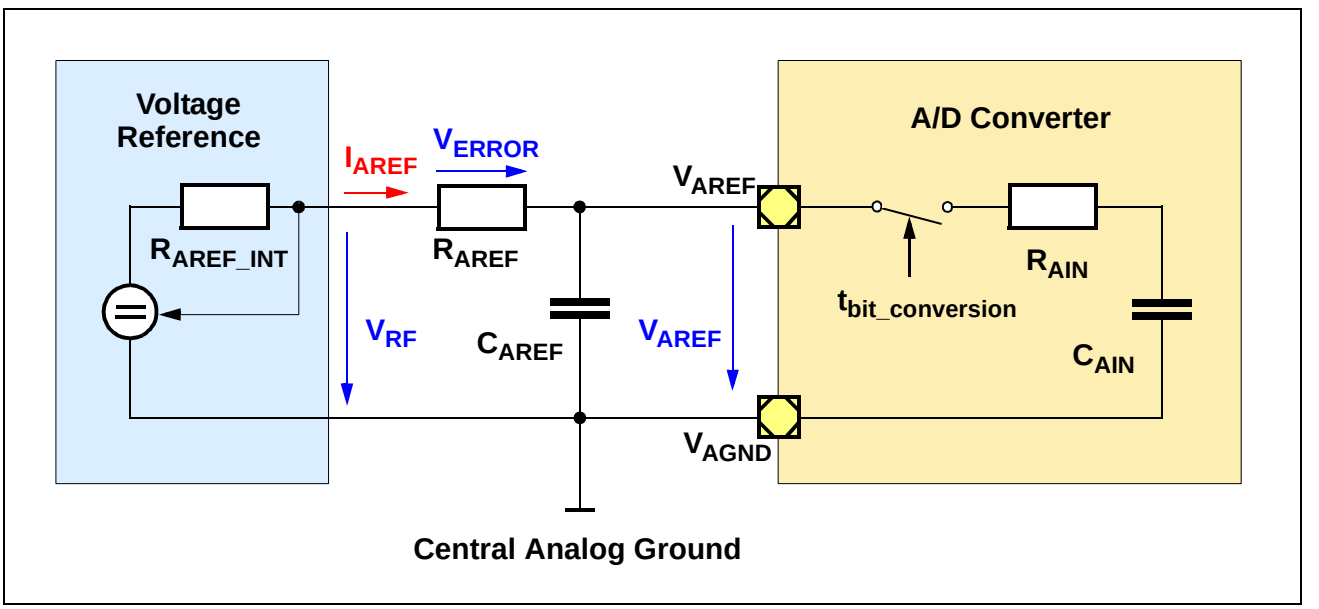


Figure 20 A/D Converter during Conversion Phase with C_{AREF}

The following considerations include the value of the external capacitance C_{AREF} with respect to the assumed maximum voltage error at V_{AREF} ($Error_{AREF}$) caused by C_{AREF} and the necessary time t_{CYCLE} to reload the external capacitor.

The relation between the external capacitance C_{AREF}, the internal C-net C_{AIN} and the assumed maximum error caused by C_{AREF} is:

$$C_{AREF} \geq 2^{r+E} \cdot (C_{AIN}) / 2$$

with:

r = 8: 8-bit resolution
r = 10: 10-bit resolution
r = 12: 12-bit resolution

E = 0: $Error_{AREF} = 1\ LSB_r$
E = 1: $Error_{AREF} = LSB_r / 2$
E = 2: $Error_{AREF} = LSB_r / 4$

$Error_{AREF} = 1 / 2^E\ LSB_r$
$LSB_r = V_{AREF} / 2^r$

Note: The maximum voltage error ($Error_{AREF}$) at V_{AREF} caused by C_{AREF} is referred to the allowed maximum input voltage at ANx ($V_{AINx} = V_{AREF}$). For input voltages at ANx smaller than V_{AREF} the additional inaccuracy at V_{AINx} is proportional less than the value of $Error_{AREF}$ used in the example calculations. The real additional inaccuracy at V_{AINx} is:
$Error_{AREF\_real} = (V_{AINx} / V_{AREF}) * Error_{AREF}$
with the condition $V_{AGND} \leq V_{AINx} \leq V_{AREF}$

The condition ($C_{AREF} \geq 2^{r+E} \cdot C_{AIN} / 2$) allows a free choice of the A/D converter basic clock t_{BC} but the cycle time t_{CYCLE} has a direct influence on the accuracy of the conversion. The cycle time has to be long enough to recharge the external capacitance C_{AREF} before the next charge-redistribution phase is started.

The external capacitance C_{AREF} has to be charged from the voltage reference. The minimum current, which is drawn from the voltage reference, is based on the charge that is necessary for a complete conversion. The charge Q for a complete charge-redistribution phase and a calibration phase is:

$$Q = C_{AIN} \cdot V_{AREF}$$

The current for the voltage reference depends on the minimum cycle time for a total conversion:

$$I_{AREF} = \frac{Q}{t_{CYCLE}}$$

The external resistance R_{AREF} between the voltage reference and the input V_{AREF} of the A/D converter has an enormous influence on the accuracy. This resistor should be chosen as small as possible! Because the continuous current I_{AREF} causes a voltage difference V_{ERROR} between the voltage reference V_{RF} and the reference voltage input V_{AREF} of the A/D converter; See **Figure 20**.

$$V_{ERROR} = R_{AREF} \cdot I_{AREF}$$

6.2.1 Calculation Example:

The assumed values used in the example are:

C_{AIN} = 33 pF, R_{AIN} = 250 Ω, V_{RF} = 5 V,
t_{BC} = 160 ns, r = 10, (10-bit resolution)

t_{CYCLE} = 7.8 µs (C166 Family: minimum time @ f_{CPU} = 20 MHz),
E = 2, $Error_{AREF}$ = 0.25 LSB, V_{ERROR} = V_{RF} / 4096 = 1.22 mV

The value for the external capacitance between V_{AREF} and V_{AGND} is:

$$C_{AREF} \geq 2^{r+E} * C_{AIN} / 2$$
$$C_{AREF} \geq 2^{10+2} * 33pF / 2$$
$$C_{AREF} \geq 68\ nF$$

Note: A typical recommendation for the value of the external capacitance is C_{AREF} = 100 nF

With the assumption V_{AREF} = V_{RF}, the minimum continuous current which has to be supplied by the voltage reference is:

$$I_{AREF} \geq C_{AIN} * V_{AREF} / t_{CYCLE}$$
$$I_{AREF} \geq 33\ pF * 5\ V / 7.8\ \mu s$$
$$I_{AREF} \geq 21\mu A$$

The allowed maximum value for the resistor R_{AREF} between voltage reference V_{RF} and input V_{AREF} of the A/D converter is:

$$R_{AREF} \leq V_{ERROR} / I_{AREF}$$
$$R_{AREF} \leq 1.22\ mV / 21\mu A$$
$$R_{AREF} \leq 58\ \Omega$$

Note: In case of an overload condition, it is possible that R_{AREF} has to be increased, to limit the overload current to the specified values. If that value of R_{AREF} exceeds the demanded error of the system, an external diode between V_{AREF} and V_{DD} can reduce the overload current; See **Figure 19**.

6.3 R_{AREF} Calculation based on the Formula in the Data Sheet

The calculation of R_{AREF} in the Data Sheets of the C500/C166 Family is based on the assumption that there is no external capacitance between V_{AREF} and V_{AGND}. The electrical model for the calculation is shown in the figure below.

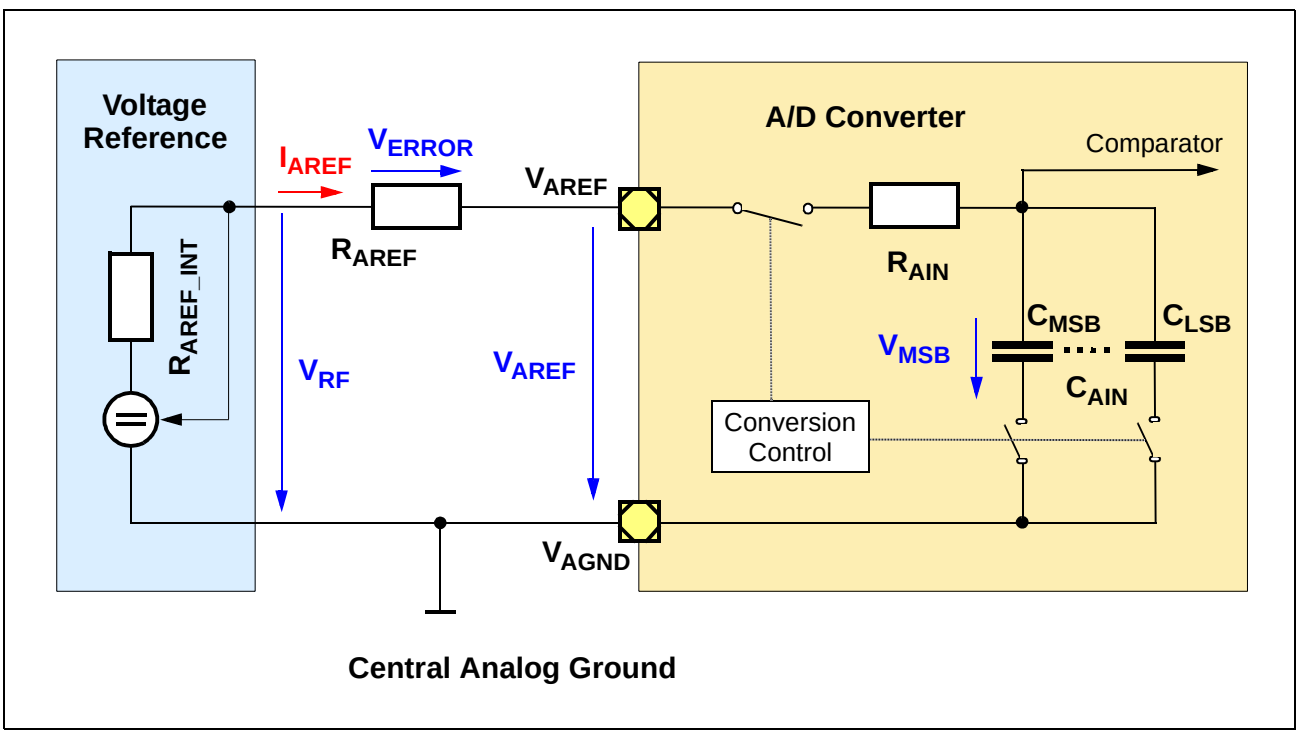


Figure 21 A/D Converter during Conversion Phase without C_{AREF}

During charge-redistribution time (successive approximation), all capacitors of the A/D converter are charged with $V_{AREF}/2$ and compared with the sampled voltage from analog input ANx. The successive approximation is started with the MSB and finished with the LSB. The capacitor of the MSB needs most charge from the voltage reference due to the binary weighting. The available time to charge the MSB to $V_{AREF}/2$ and to compare the MSB voltage with the sampled voltage is $4*t_{BC}$ (t_{BC}: Basic Clock frequency can be controlled via register ADCON). Typically half the time can be used to charge MSB to $V_{AREF}/2$ (value depends on device type and on technology). The other half is necessary for the comparison of the values by the comparator of the A/D converter.

The worst case for the maximum allowed resistance between voltage reference V_{RF} and input V_{AREF} of the A/D converter is the conversion of the MSB. The capacitance C_{MSB} is charged with $V_{AREF}/2$ and the voltage wave form at the comparator input is:

$$V_{MSB}(t) = (V_{AREF}/2) \cdot \left(1 - e^{\frac{-t}{(R_{AREF} + R_{AIN}) \cdot C_{MSB}}}\right)$$

The maximum allowed value for R_{AREF} with ($V_{MSB}(t_{BC}) = V_{AREF}/2 - Error_{MSB}$) is:

$$R_{AREF} \leq \frac{t_{BC} \cdot 2}{C_{MSB} \cdot \ln \frac{V_{AREF}}{Error_{MSB} \cdot 2}} - R_{AIN}$$

The figure below shows the comparator voltage $V_{MSB}(t)$ during the conversion of the MSB. The conversion of the MSB lasts $4*t_{BC}$.

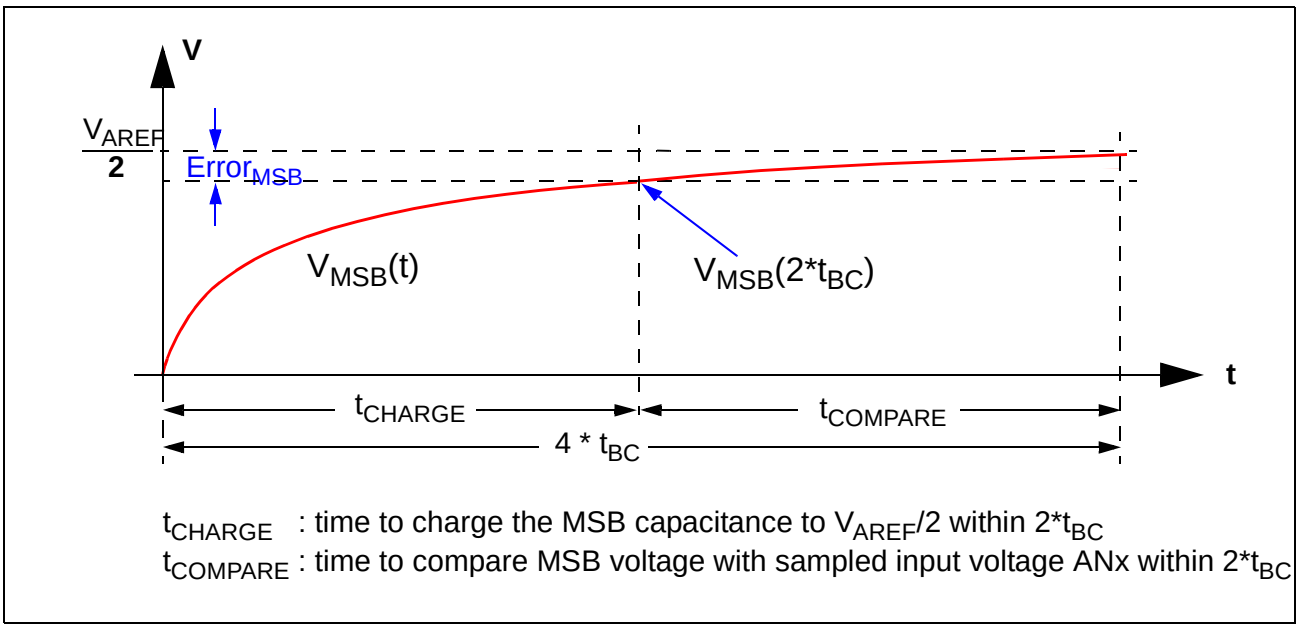


Figure 22 Comparator Voltage during Conversion of MSB

The formula in the Data Sheet can be derived from the relation above. The typical value C_{MSB} of a 16-bit microcontroller used for the calculation is C_{MSB} = 16.5 pF ($C_{MSB} = C_{AIN} / 2$). The assumed maximum $Error_{MSB}$ caused by R_{AREF} is LSB/2 = $V_{AREF}/(2*2^{10})$.

$$R_{AREF} \leq \frac{t_{BC}}{57 \cdot 10^{12}} - R_{AIN}$$

This relation rounded with R_{AREF} in kΩ and t_{BC} in ns results in the Data Sheet formula:

$$R_{AREF} \leq t_{BC} / 60 - 0.25$$

6.3.1 Calculation Example:

For a system using an f_{CPU} = 25 MHz and a t_{BC} = 160 ns the allowed maximum value for R_{AREF} is:

$R_{AREF} = 160\ ns / 60 - 0.25$ with R_{AREF} in kΩ and t_{BC} in ns
$R_{AREF} = 2.4\ k\Omega$

The minimum current which has to be supplied by the voltage reference is:

$I_{AREF} \geq V_{AREF} / R_{AREF}$
$I_{AREF} \geq 5\ V / 2400\ \Omega$ with V_{AREF} = 5 V
$I_{AREF} \geq 2.1\ mA$

The calculated current is not a continuous one. It is a peak current which flows only at the beginning of MSB conversion and becomes smaller with each converted bit down to the LSB.

Note: This value of R_{AREF} assumes that no external capacitance between V_{AREF} and V_{AGND} is used.

6.4 Ratiometric Configuration

In a non-ratiometric configuration there is no relation between the voltage of the analog source and the reference voltage at pin V_{AREF}. Both, the accuracy of the reference voltage and the accuracy of the analog source have an influence to the accuracy of the total A/D conversion system, because any changes in the supply voltage of the analog source results in a change at the analog input voltage ANx seen by the A/D converter. Since the voltage reference is independent from the analog source excitation, the ADC conversion result will reflect the changed excitation

Figure 23 shows the principle of a ratiometric configuration. The same voltage reference source is used for the analog source excitation and the reference voltage input V_{AREF}. Therefore a given change in the analog source excitation causes the same change at the reference voltage V_{AREF}. The A/D converter conversion result is the ratio of the analog input ANx, to the reference voltage V_{AREF}. Since both, the analog input ANx and the reference voltage V_{AREF} are derived from the same voltage reference source, changes do not cause measurement errors. Hence, the A/D converter conversion result is independent to variations in the analog source excitation or variations in the reference voltage input V_{AREF}. Because of that a stable voltage reference is not necessary to achieve an accurate measurement result.

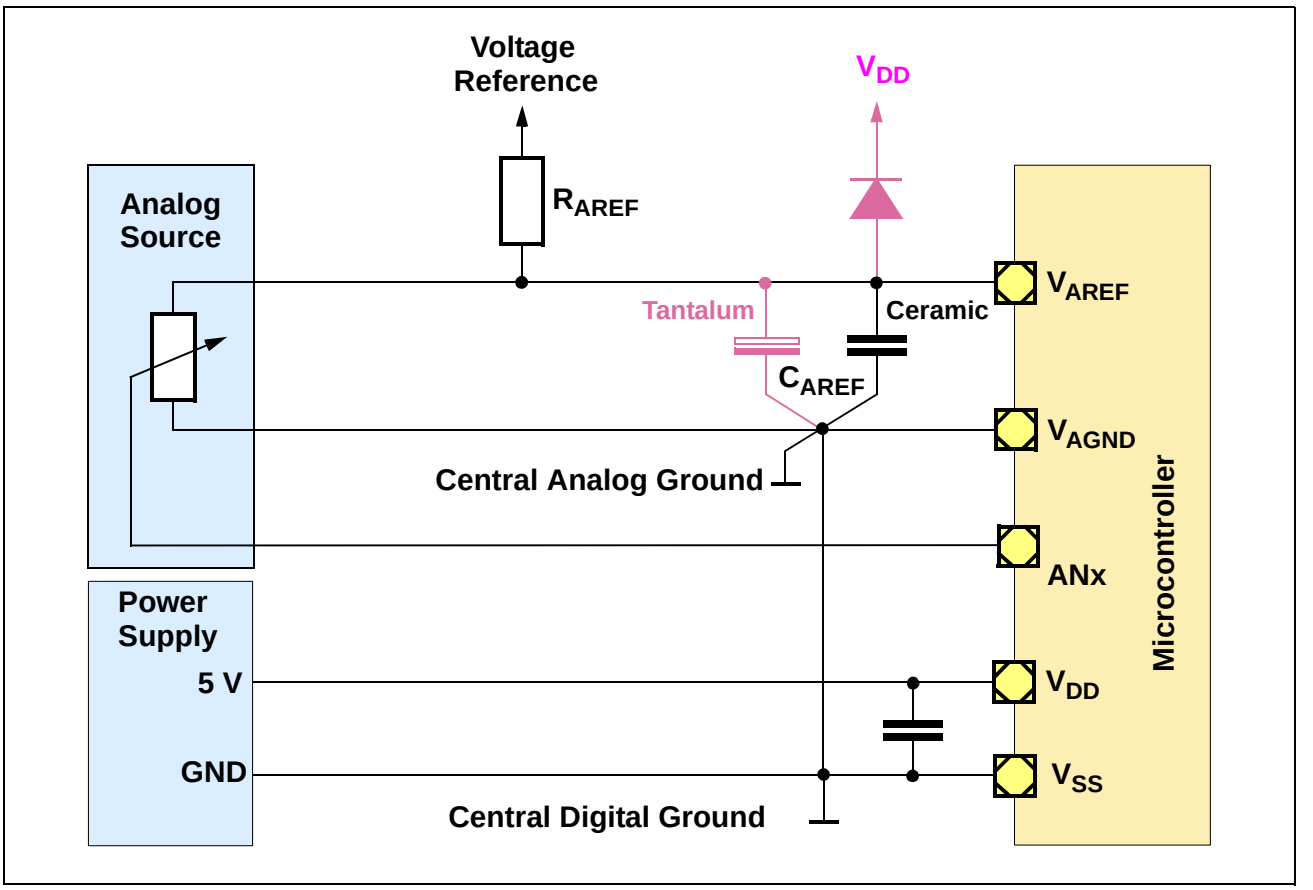


Figure 23 Ratiometric Configuration

7 Overload and Leakage Current

Both, overload and leakage currents are specified in the Data Sheet. Consideration of overload and leakage currents can have an influence on the design of the external components of the analog source. **Figure 24** is a simplified electrical model with ESD structure (clamp diodes) and leakage current of an analog input.

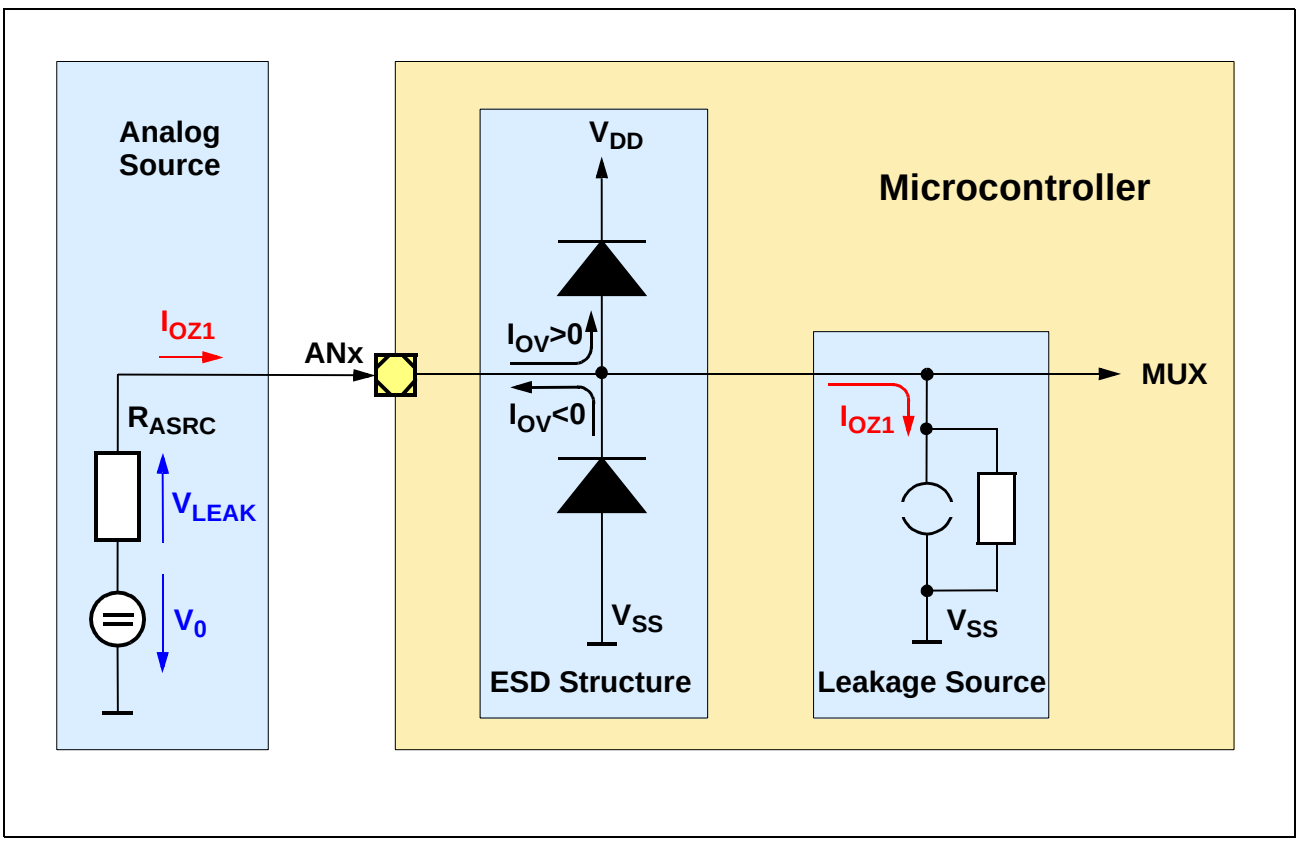


Figure 24 A/D Converter Input with ESD Structure and Leakage Source

*Note: The ESD structure of the reference voltage V_{AREF} and the reference ground V_{AGND} is the same as shown in the **Figure 24**.*

7.1 Leakage Current

The maximum input leakage current of the A/D converter is specified in the Data Sheet in section 'DC Characteristics'. The input leakage current is the sum of all currents which can flow into or out of an input pin caused by parasitic effects of the input structure, see **Figure 24**.

The symbols in the Data Sheets of the C500 and C166 Family used for the input leakage current of the A/D converter are different. For the C166 Family it is I_{OZ1} and for the C500

Family it is I_{LI}. In this Application Note the symbol I_{OZ1} is used for the input leakage current.

The specified value of the A/D converter input leakage current depends on the device type. Please refer to the Data Sheet for the exact value.

The input leakage current has to be taken into account for the calculation of the maximum allowed error of the A/D converter result referred to the analog source. Because the resistance of the analog source R_{ASRC} and the input leakage current I_{OZ1} can cause an additional error via the external 'leakage voltage' V_{LEAK}.

$$V_{LEAK} = I_{OZ1} * R_{ASRC}$$

The leakage voltage V_{LEAK} can cause an additional unadjusted error AUE_{LEAK}.

$$AUE_{LEAK} = V_{LEAK} / 1LSB$$

7.1.1 Calculation Example

Assumed system values:

AUE_{LEAK} = 0.25 LSB		Assumed maximum additional unadjusted error caused by resistance of the analog source R_{ASRC}
V_{AREF}	= 5 V	1 LSB = 4.9 mV (10-bit A/D converter)
I_{OZ1}	= |± 200 nA|	Specified maximum input leakage current

What is the allowed maximum resistance of the analog source R_{ASRC} ?

$R_{ASRC} = V_{LEAK} / I_{OZ1}$
$R_{ASRC} = AUE_{LEAK} * 1LSB / I_{OZ1}$
$R_{ASRC} = 0.25\ LSB * 4.9\ mV / 200\ nA$
$R_{ASRC} = 6125\ \Omega$

Note: The specified maximum Input Leakage Current of |+/- 200 nA| can reduce the conversion accuracy when the external resistance has a high value (>10 kOhm).

7.2 Overload Current

An overload condition is not a normal operating condition. It occurs if the standard operating conditions are exceeded, i.e. the voltage on an A/D converter input pin V_{AINx} exceeds the specified range ($V_{AINx} > V_{DD} + 0.5$ V or $V_{AINx} < V_{SS} - 0.5$ V). The supply voltage must remain within the specified limits.

In case of an overload condition on an A/D converter input pin, one of the clamp diodes becomes conductive. If $V_{AINx} > V_{DD} + 0.5$ V then the clamp diode connected to V_{DD} begins to conduct. If $V_{AINx} < V_{SS} - 0.5$ V then the clamp diode connected to V_{SS} begins to conduct; See **Figure 24**.

The overload current has to be taken into account for the calculation of external resistors which protect the microcontroller inputs. These external resistors guarantee that, in case of a system error, the specified maximum value of the overload current will not be exceeded. The calculation also has to consider the specified absolute sum of input overload currents on all port pins of the microcontroller and especially the specified absolute sum of the A/D converter input.

7.2.1 Overload Current and Absolute Maximum Ratings

The parameters of the **Absolute Maximum Ratings** are stress ratings only and functional operation of the microcontroller is not guaranteed at these or other conditions above the 'operation conditions'. Stresses above the absolute maximum ratings may cause permanent damage to the microcontroller. Exposing the microcontroller to absolute maximum rating conditions for extended periods may affect device reliability.

When the system is switched off or in periods where it is not necessary to guarantee correct operation, the absolute maximum ratings are the fundamental information for the calculation of the input overload current, which may occur in case of a system error. In those cases the specified maximum overload current is $I_{OV} = \pm 10$ mA on any pin and the absolute sum of input overload currents on all port pins is 100 mA. For the exact values, please refer to the Data Sheet.

7.2.1.1 Calculation Example

Assumed system values:

V_{DD}	= 0 V	System supply voltage is off (worst case)
V_{Err_max}	= 12 V	Maximum voltage of the analog signal in case of a fatal system error
I_{OV_max}	= |±10 mA|	Specified absolute maximum rating of the overload current

What is the minimum value for the external resistor R_P to protect an analog input pin for a short time overload condition?

R_P = $(V_{Err\_max} - V_{DD} - 0.5\ V) / I_{OV\_max}$
R_P = $(12\ V - 0\ V - 0.5\ V) / 10\ mA$
R_P = $1150\ \Omega$

7.2.2 Overload Current and Operating Conditions

The **Operating Conditions** must not be exceeded in order to ensure correct operation of the microcontroller. The specified operating conditions allow a maximum overload current of $I_{OV} = \pm 5$ mA on any pin and the absolute sum over input overload currents on all port pins is |50| mA. The specified TUE of the A/D converter is guaranteed only if the absolute sum of input overload currents on all analog input pins does not exceed 10 mA. For the exact values please refer to the Data Sheet.

7.2.2.1 Calculation Example

Assumed system values:

V_{DD}	= 4.5 V	Minimum system supply voltage during operating conditions (worst case)
V_{Err_max}	= 12 V	Maximum voltage of the analog signal in case of a fatal system error
I_{OV_max}	= |±5 mA|	Specified maximum of the overload current during operating conditions

What is the minimum value of the external resistor R_P to protect an analog input of the microcontroller and to ensure correct operation?

R_P = $(V_{Err\_max} - V_{DD} - 0.5\ V) / I_{OV\_max}$
R_P = $(12\ V - 4.5\ V - 0.5\ V) / 5\ mA$
R_P = $1400\ \Omega$

8 PCB and Design Considerations

This chapter is a brief introduction in mixed signal board design with a list of guidelines for optimum printed circuit board layout for microcontrollers with on-chip A/D converter.

8.1 Component Placing

- Partition the board with all analog components grounded together in one area and all digital components in the other. Common power supply related components should be centrally located.
- Mixed signal components, including the microcontroller, should bridge the partitions with only analog pins in the analog area, and only digital pins in the digital area. Rotating the microcontroller can often make this task easier.

8.2 Power Supply

- Place the analog power and voltage reference regulators over the analog plane. The same holds for the digital power regulators.
- Analog power traces should be over the analog ground plane. The same holds for the digital power traces.
- Decoupling capacitors should be close to the microcontroller pins, or positioned for the shortest connection to pins with wide traces to reduce impedance.
- If both large electrolytic and small ceramic capacitors are recommended, make the small ceramic capacitor closest to the microcontroller pins.

8.3 Ground Planes

- Have separate analog and digital ground planes on the same layer, separated by a gap, with the digital components over the digital ground plane, and the analog components over the analog ground plane.
- Analog and digital ground planes should only be connected at one point (most cases). The best place is below the microcontroller. Have vias available in the board to allow alternative points.
- The analog to digital ground plane connection should be near to the power supply, or near to the power supply connections to the board, or near to the microcontroller.
- For boards with more than 2 layers, do not overlap analog related and digital related planes. Do not have a plane that crosses the gap between the analog ground plane and the digital ground plane region.

8.4 Signal Lines

- Analog signal traces should be over the analog ground plane.
- Digital power and digital signal traces should be over the digital ground plane.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane. These regions should not be left floating, which only makes the interference worse. Using ground plane fill has shown to reduce digital to analog coupling by up to 30 dB.

8.5 Clock Generation

- Locate quartz crystal, ceramic resonator or external oscillator as close as possible to the microcontroller.
- Keep digital signal traces, especially the clock signal, as far away from analog input and voltage reference pins as possible.
- Avoid multiple oscillators or asynchronous clocks. Best results are obtained when all circuits are synchronous to the A/D converter sampling clock.

9 Used Short Cuts

ADC : Analog Digital Converter
ANx : Analog input X
AUE_{Leak} : Additional unadjusted error caused by the leakage current

C_{AIN} : A/D converter input capacitance (internal C-net)
C_{AIN_max} : Maximum of the A/D converter input capacitance
C_{AREF} : External capacitance connected to the reference voltage input V_{AREF}
C_{EXT} : External capacitance connected to the analog input
C_{HOLD} : Hold capacitance of the A/D converter
C_{LSB} : LSB of the internal C-net
C_{MSB} : MSB of the internal C-net
C-Net : Internal A/D converter capacitor network.
C_9 - C_0 : C-net for conversion (10-bit resolution).
$C_{7'}$ - $C_{0'}$: C-net for calibration.
chn : Analog channel n

DNLE : Differential nonlinearity error

E : Variable for allowed Error to calculate C_{AREF}
$Error_{AINx}$: Maximum deviation between the voltage on ANx and V_0 when the sample time is finished
$Error_{AINx\_real}$: Real deviation between the voltage on ANx and V_0 referred to the actual voltage at ANx
$Error_{AREF}$: Maximum voltage error at V_{AREF} caused by C_{AREF}
$Error_{MSB}$: Missing voltage to charge the MSB capacitance of the internal C-net to $V_{AREF/2}$ during charge-redistribution phase
ESD : Electrostatic discharge

f_{CPU} : CPU frequency
f_C : Cutoff frequency
f_{CYCLE} : Cycle frequency (f_{CYCLE} = 1 / t_{CYCLEn})

INLE	: Integral nonlinearity error
I_{AREF}	: Current of the voltage reference
I_{Li}	: Input leakage current (C500 Family)
I_{OV}	: Overload current
I_{OV_max}	: Specified maximum rating of the overload current or : Specified maximum of the overload current during operating conditions
I_{OZ1}	: Input leakage current (C166 Family)
LSB	: Least significant bit (general)
LSB_r	: Least significant bit referred to r-bit resolution ($LSB_r = V_{AREF} / 2^r$)
MSB	: Most significant bit
Q	: Charge for a complete charge-redistribution- and a calibration phase
r	: Resolution of the A/D converter
R_{AIN}	: Internal series resistance of the A/D converter
R_{ASRC}	: Internal resistance of the analog source
R_{AREF}	: Resistance between voltage reference and V_{AREF} input
R_{AREF_INT}	: Internal resistance of the voltage reference
R_P	: External resistor R_P to protect an analog input in case of an overload condition
t_{BC}	: A/D converter basic clock
t_C	: Conversion time
t_{Cn}	: Conversion time of analog channel n
t_{CR}	: Charge redistribution time
t_{CYCLE}	: Cycle time
t_{CYCLEn}	: Cycle time of analog channel n
t_{CHARGE}	: Time to charge the MSB capacitance to $V_{AREF}/2$ within $2*t_{BC}$
$t_{COMPARE}$	: Time to compare MSB voltage with sampled input voltage ANx within $2*t_{BC}$
t_S	: Sample time
TCL	: Internal clock, 2 * TCL = 1 / fcpu
τ_1, τ_2, τ_3	: Time constants for the different phases of a conversion
TUE	: Total unadjusted error

V_{AREF} : Reference voltage input for the A/D converter
V_{AGND} : Reference ground for the A/D converter
V_{ANx} : Voltage at the analog input ANx
V_{CAIN} : Voltage at the internal C-net
$V_C(t)$: Charge curve of C_{EXT} for a total cycle
$V_C(t_{CYCLE})$: Voltage of C_{EXT} at the end of a total cycle
V_{DD} : Supply voltage
V_{ERROR} : Voltage at R_{AREF}
V_{ERR_max} : Maximum voltage of an analog signal in case of a fatal system error
V_{Leak} : Leakage voltage at R_{ASRC}
V_{MSB} : Voltage at the internal MSB of the C-net
$V_{MSB}(t)$: Comparator voltage during conversion of MSB
$V_{MSB}(2t_{BC})$: Comparator voltage after $2*t_{BC}$
V_R : Missing rest voltage at the end of a conversion cycle
V_{RF} : Voltage reference
V_{SS} : Digital GND
$V_S(t)$: Voltage during sample time
$V_S(t_S)$: Voltage at the end of sample time
V_0 : Voltage of the analog source
V_Δ : Voltage jump at the beginning of the sample time

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