Application Note, V1.1, October 2007

AP16120

XC2000 & XE166 Families

Scalable Pads - Electrical Specification. Scalable Output Drivers in 130nm CMOS Technology

Microcontrollers

Never stop thinking

Edition 2007-10

Published by
Infineon Technologies AG
81726 Munich, Germany

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Revision History:	2007-10	**V1.1**
Previous Version: none	-	
Page	Subjects (major changes since last revision)	

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1 Preface

Output driver scaling, also referred to as „slew rate control“, is an effective technique to reduce the electromagnetic emission of an integrated circuit by reducing the driver strength and/or smoothing the rising and falling edges of one or more pad output drivers.

Output driver scaling makes sense only when a certain margin regarding signal frequency and/or capacitive output load is available. Any driver scaling must maintain proper signal integrity.

This application note presents a huge set of output driver characterization data, which shall enable the system designers to select proper driver settings to reduce the electromagnetic emission caused by the driver switching, while maintaining the desired signal integrity. Parameters under consideration are switching frequency, capacitive output load, and ambient temperature.

Chapter 2 introduces physical basics behind the scaling.

Chapter 3 describes the XC2000 software initialization for timing and emission measurements.

Chapter 4 provides values and comparison diagrams of measured rise/fall times under various conditions.

Chapter 5 compares several measured electromagnetic emissions under various conditions.

Chapter 6 recommends useful settings for the drivers by introducing signal categories and giving lots of decision tables and graphs.

Annex A shows the waveforms of all measured rise/fall times.

Annex B shows all measured emission spectra used for the discussions in Chapter 5.

Annex C explains all abbreviations used in this application note in a glossary.

Guideline to use this application note

In most cases an appropriate driver setting is searched for, based on a given signal data rate, a given capacitive load connected to this signal, and a given maximal ambient temperature. In this case the diagrams given in Chapter 6 provide the required pad driver settings. These suitable pad driver settings lead to minimum electromagnetic emission under the given constraints for data rate, capacitive load, and operating temperature.

In addition, the measured values of rise and fall times for all driver settings listed in comparison diagrams can be referred in Chapter 4.

The impact of driver settings on electromagnetic emission can be estimated from the comparison diagrams in Chapter 5.

Annex A and B serve as data pool for detailled timing and electromagnetic emission behaviour for all pad driver settings under various temperature and capacitve load conditions. Note that emissions are always measured at room temperature (25°C).

Important notes

The information given in this application note is valid for Infineon microcontrollers of the XC2000 and XE166 families, fabricated in 130 nm CMOS technology. The application note refers to the XC2000 microcontroller family, however the same data also applies to the XE166 microcontroller family.

Please note that all numbers given in this application note are not guaranteed in the microcontroller data sheets. They are verified by design without being monitored during the IC fabrication process. The numbers are based on timing measurements performed on center lot devices. Fabrication process windows may lead to deviations of below 10%.

2 Introduction

The output driver scaling principle of the XC2000 microcontrollers is shown in Fig. 1. The driver configuration is possible by setting corresponding control bits in the port-related output control registers. Fig. 2 shows the bit contents of these registers.

2.1 Pad driver scaling in detail

2.1.1 Driver characteristics

Basically, we distinguish between driver control and edge control. Driver control bits set the general DC driving capability of the respective driver. Reducing the driver strength increases the output's internal resistance which attenuates noise that is imported/exported via the output line.

For a given external load, charging and discharging time varies with the driver strength, thus the rise/fall times will change accordingly. For driving LEDs or power transistors, however, a stable high output current may still be required independent of low toggle rates which would normally allow to decide for weaker drivers due to their low transitions and thus low noise emission.

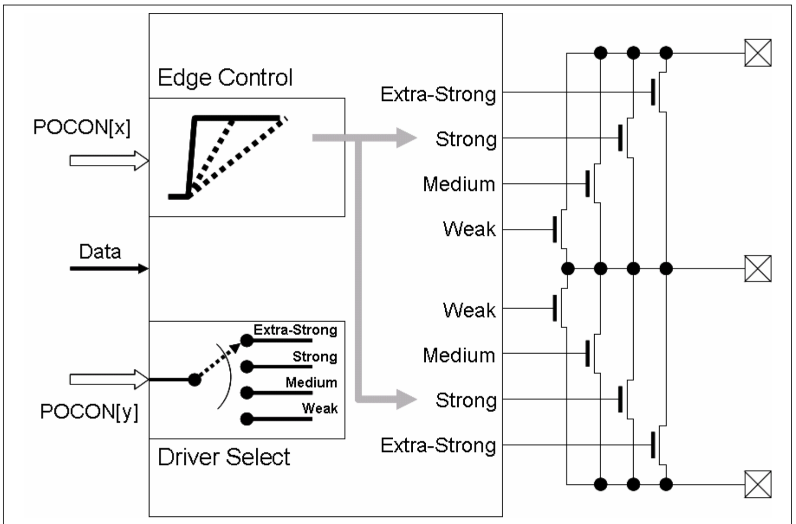

Figure 1: Pad output driver schematic

The controllable output drivers of the XC2000 pins feature three differently sized transistors (strong, medium, and weak) for each direction (push and pull). The time of activating/deactivating these transistors determines the output characteristics of the respective port driver.

The strength of the driver can be selected to adapt the driver characteristics to the application's requirements:

In **Strong Driver Mode**, the medium and strong transistors are activated. In this mode the driver provides maximum output current even after the target signal level is reached.

In **Medium Driver Mode**, only the medium transistor is activated while the other transistors remain off.

In **Weak Driver Mode**, only the weak transistor is activated while the other transistors remain off. This results in smooth transitions with low current peaks (and reduced susceptibility for noise) on the cost of increased transition times, i.e. slower edges, depending on the capacitive load, and low static current.

The XC2000 microcontrollers offer a system clock output EXTCLK at Port 2.8 which is able to drive an external load at original or down-scaled toggle rate. To serve clock rates above 40MHz, this pin EXTCLK is equipped with an additional **Extra-Strong Mode** driver whose driving capability exceeds the one of the standard "Strong-Sharp" driver.

Port x Output Control Register XSFR (E8A0$_H$+2*x) **Reset Value: 0000$_H$**

15	14 13 12	11	10 9 8	7	6 5 4	3	2 1 0
PPS 3	PDM3	PPS 2	PDM2	PPS 1	PDM1	PPS 0	PDM0
rw	rwr	rw	rw	rw	rw	rw	rw

Field	Bit	Type	Description	
PDM0, PDM1, PDM2, PDM3	[2:0], [6:4], [10:8], [14:12]	rw	**Port Driver Mode x**	
			Code Driver strength [1)]	Edge Shape[2)]
			000 Strong driver	Sharp edge mode
			001 Strong driver	Medium edge mode
			010 Strong driver	Soft edge mode
			011 Weak driver	
			100 Medium driver	
			101 Medium driver	
			110 Medium driver	
			111 Weak driver	

1) Defines the current the respective driver can deliver to the external circuitry.
2) Defines the switching characteristics to the respective new output level. This also influences the peak currents through the driver when producing an edge, ie when changing the output level.

Figure 2: Port output control register specification

Deviating from Fig. 2, pins [12:8] of Port2 are configured by bit field PDM2, but pin 8 uses its extra-strong driver whenever PDM3 contains an odd number.

2.1.2 Edge Characteristics

Signal slopes or edges define the rise/fall time for the respective output, i.e. the output transition time. Soft edges reduce the peak currents that are drawn when changing the voltage level of an external capacitive load. For a bus interface, however, sharp edges may still be required. Edge characteristic are controlled by the pad pre-driver which controls the final output driver stage.

The Port Output Control registers POCONx provide the corresponding control bits. A 3-bit control field configures the driver strength and the edge shape. Word ports consume four control nibbles each, byte ports consume two control nibbles each, where each control field controls 4 pins of the respective port. Fig. 2 shows an example of a POCON register and the allocation of control bit fields and port pins.

In this guideline, the scaling effects of the XC2000 microcontrollers' output drivers fabricated in 130nm CMOS technology are described. It serves as a reference addendum to the respective microcontroller product specifications where the individual bit settings can be found.

2.2 Physical basics

Two main constraints have to be met when deciding for a certain clock driver setting: signal integrity and power integrity. Both issues will be discussed after a general introduction to capacitive load charging.

2.2.1 Load charging

Generally, a switching transistor output stage delivers charge to its corresponding load capacitor during rising edge and draws charge from its load capacitor during falling edge. Timing diagrams normally show the signal's voltage over time characteristics. However, the resulting timing is a result of the electrical charge transfer described above. Charge is transferred by flowing current.

A bigger pad driver means a smaller resistance in the loading path of the external load. Fig. 3 shows the load current and voltage of two examples of pad drivers connected to a load of C=40pF. The strong driver has an output resistance of 25Ω, the weak driver 50Ω. For times t<0, the output voltage is 0V. At t=0, the load capacitor C is connected to the target output voltage U=5V via the respective driver pullup transistor. As a reaction, the load current steps immediately to the value I=U/R. I is bigger for smaller values of R. This means that the strong driver generates a bigger current jump and charges the load capacitor in a shorter time.

In time domain this leads to bigger reflections for not adapted driver impedances. Since typical trace impedances range from 60 to 120Ω , a strong driver with Z=10Ω is poorly adapted and may cause big voltage over- and undershoots. A weak driver with Z=100Ω may fit perfectly and generate a clean voltage switching signal without over- or undershoots. These effects are discussed in chapter 2.2.2.

In frequency domain, the current peak which is resulting from the charging of the load capacitor and from the over- or undershoots, causes significant RF energy and thus electromagnetic emission on the pad power supply. These effects are discussed in chapter 2.2.3.

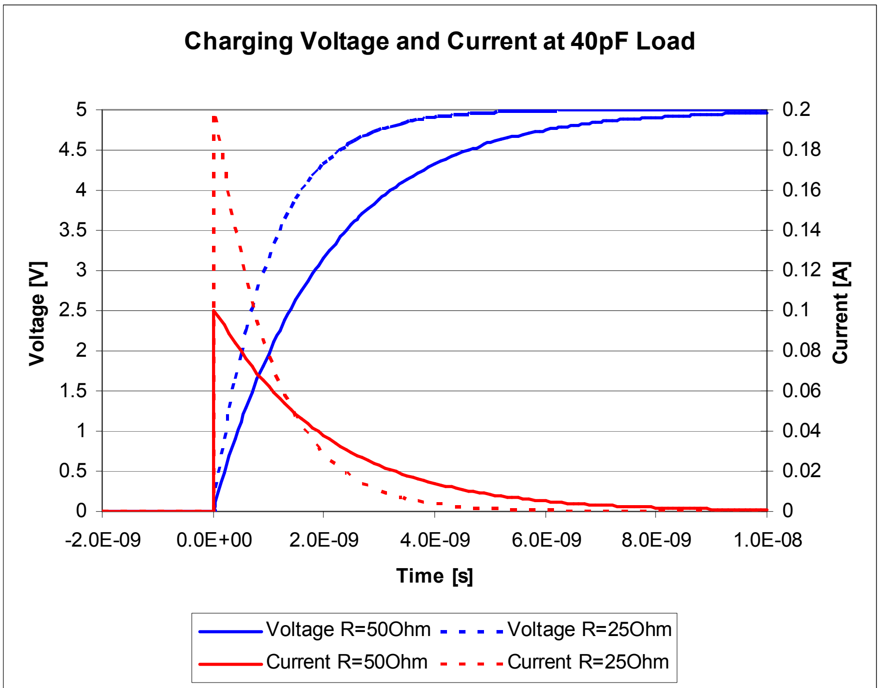

Figure 3: Current-/voltage charging curves for different driver strengths

Not only the pad driver

impedance, but also the connected capacitive load determines the electromagnetic emission amplitudes. Fig. 4 illustrates the differences in charging current and voltage between a capacitive load of 40pF and one of 20pF. In both cases, the driver impedance is set to 50Ω.

As expected, the charging voltage increases faster for a smaller load. However, the starting value of the charging current is only determined by the driver impedance and is thus load-independent. The load affects only the speed of load current decrease. It decreases faster if the load is smaller. This means on the other hand a bigger di/dt for smaller loads, resulting in higer emission for smaller loads.

This disadvantage can be compensated by chosing a smaller pad driver, i.e. a weaker driver setting, causing bigger driver impedance and thus smaller di/dt for the charging current.

The selection of a weaker driver setting slows down the pad switching time, so care must be taken to maintain the required signal integrity.

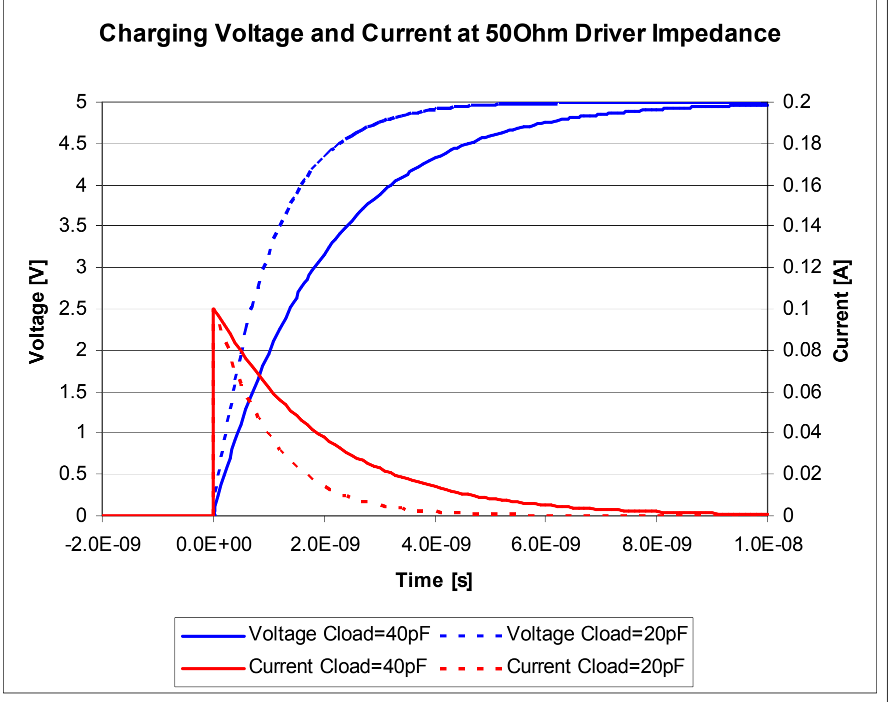

Figure 4: Current-/voltage charging curves for different capacitive loads

2.2.2 Signal integrity

Maintaining signal integrity means to select the rise/fall times such that all signal handshaking and data communication timings and levels are ensured for proper system operation. This means the data interchange between the microcontroller and external ICs like Flash memory, line drivers, receivers and transmitters etc. runs properly.

Therefore, it has to be taken into account that CMOS transistors become slower with rising temperature. Thus the timing of a critical signal has to be matched for proper operation at highest ambient temperature. Depending on the application, common temperature ranges are up to 85°C or up to 125°C. Several automotive control units specify an ambient temperature range from -40°C up to 125°C. The die temperature may reach values up to 150°C during operation.

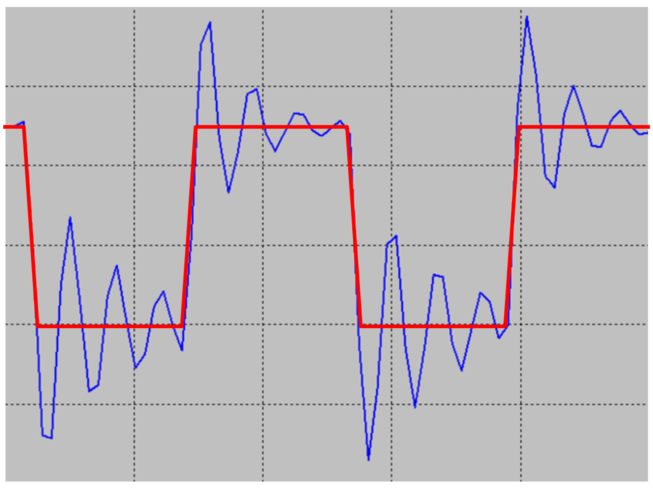

Figure 5: Signal over- and undershoots

Rules:

- Choose driver characteristics to meet the DC driving requirements. Make sure that the DC current provided by the microcontroller's pad drivers is sufficient to drive actuators into the desired logic state.
- Choose edge settings to meet system timing constraints at the highest system temperature. Make sure that no too strong driver settings are selected. This

would lead to unnecessarily fast signal edges, causing two disadvantages regarding electromagnetic emission: (1) The slopes are too fast and cause undesired high emission energy at higher frequencies; (2) Over- and undershoot appears with the danger of latchup, spikes leading to wrong logic states or increased data stable delays and undesired high frequency emission.

- If system timing requires short signal rise/fall times, series termination is recommended to avoid over-/undershoot at signal transitions, see Fig. 5. The value of the termination resistor has to be chosen identical to the signal line impedance.

2.2.3 Power integrity / Electromagnetic emission

Any switching between low and high voltage levels generates RF noise. This happens whenever the switching voltage or the switching current has no sinusoidal shape. Switching currents are mainly responsible for electromagnetic emission because of the voltage drop across line inductances such as bond wires and lead frames. Any shapes other than sinusoidal are composed by the overlay of multiple frequencies, also known as harmonics. To reach a significantly steep edge of a trapezoidal voltage of a clock signal, short current pulses during the edges are required. These switching currents are outlined as nearly triangular peaks which are composed from the base frequency and a set of odd and even harmonics, depending on the exact pulse shape.

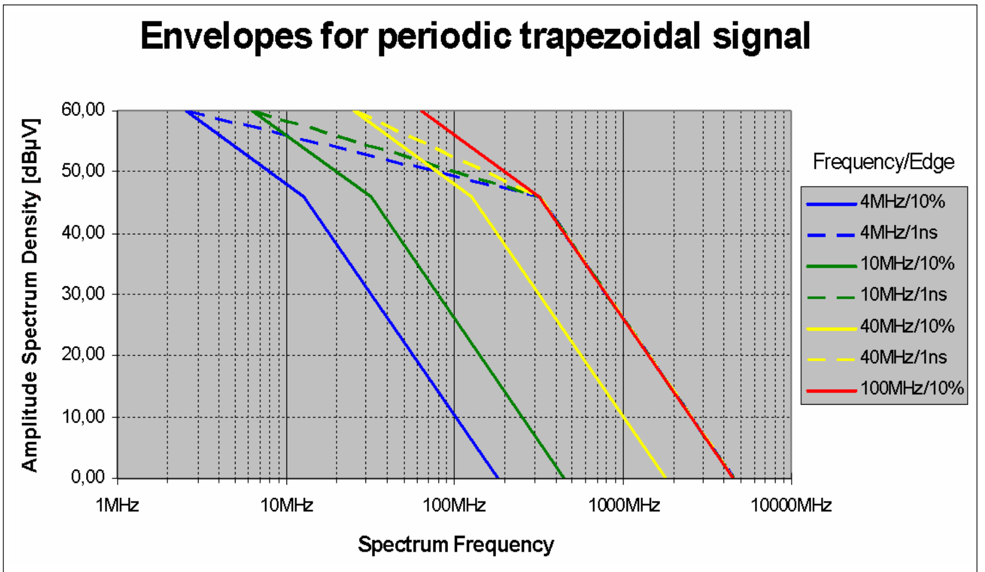

Figure 6: Spectrum envelope for different clocks and edges

The steeper a switching pulse is, the higher frequencies are required to form the rising and falling edges. A rise time of 1ns leads to a spectrum composed from harmonics up to at least 500 MHz.

Assuming a 100MHz (10ns period) clock signal consisting of 10% rise time, 40% high level, 10% fall time and 40% low level, this clock signal already generates at least harmonics up to 500MHz.

Unfortunately not the clock frequency, but the rise/fall times determine the resulting RF spectrum. Even if a clock driver operates at a relatively low toggle rate, it may generate the same RF spectrum as if it would operate at a significantly higher toggle rate – as long as its rise/fall times are not adjusted to the lower toggle rate by slowing down the transitions. For example, if the mentioned 100MHz clock driver operates at only 10 MHz, its rise/fall times should be extended from 1 ns to 10 ns, still maintaining the 10% ratio relatively to the clock period time. Fig. 6 illustrates that behaviour.

Rule:

- Choose driver and edge characteristics to result in lowest electromagnetic emission while meeting all system timing requirements at highest system temperature.

3 XC2000 Test Configuration

Timing and EMI measurements in this docment use the active EXTCLK (P2.8) pin. P2.8 offers the full scale of driver settings: extra-strong, strong-sharp, strong-medium, strong-soft, medium, weak.

Roughly, these settings can be linked to driven data rates, as documented in Chapter 6. Note that the actual data rate which can be driven by the selected driver depends on additional parameters like external capacitive load, pad supply voltage and ambient temperature.

The "standard" driver settings for EXTCLK are configured by bit field PDM2 in the Port2 Control Register (P2_POCON; address $E8A4_H$), see Fig. 7. The extra-strong driver is selected whenever PDM3 contains an odd number.

Port x Output Control Register XSFR ($E8A0_H$+2*x) **Reset Value: 0000_H**

15	14–12	11	10–8	7	6–4	3	2–0
PPS 3	PDM3	PPS 2	PDM2	PPS 1	PDM1	PPS 0	PDM0
rw	rwr	rw	rw	rw	rw	rw	rw

Field	Bit	Type	Description
PDM0, PDM1, PDM2, PDM3	[2:0], [6:4], [10:8], [14:12]	rw	**Port Driver Mode x** Code Driver strength 1) — Edge Shape2) 000 Strong driver — Sharp edge mode 001 Strong driver — Medium edge mode 010 Strong driver — Soft edge mode 011 Weak driver 100 Medium driver 101 Medium driver 110 Medium driver 111 Weak driver

1) Defines the current the respective driver can deliver to the external circuitry.

2) Defines the switching characteristics to the respective new output level. This also influences the peak currents through the driver when producing an edge, ie when changing the output level.

Figure 7: Port output control register specification

EXTCLK (P2.8) is activated and configured by the following register settings:

External Clock Control Register (EXTCON; address $FF5E_H$):

EXTCON[4:0]=00101_B

Select f_{PLL} as clock source and enable this clock on P2.8.

Port2 Control Register (P2_POCON; address $E8A4_H$):

Contents select the driver strength, see Table 1.

Driver Setting	Abbreviation	Data rate 1)	P2_POCON
Weak	WEA	≤ 500 kHz	03xxh
Medium	MED	≤ 4 MHz	04xxh
Strong-soft	SSO	≤ 25 MHz	02xxh
Strong-medium	SME	≤ 40 MHz	01xxh
Strong-sharp	SSH	≤ 66 MHz	00xxh
Extra-strong	XST	80 MHz	1xxxh

Table 1: Driver settings in the XC2000 family

1) Operating conditions are: VDDP0=5.0V, C_{LOAD}=10pF, T_A=25°C, VOL<10%, VOH >90%.

4 Measured Timings

4.1.1 Measurement conditions and naming conventions

The test configuration listed in chapter 3 applies. Accordingly, all timings are measured at EXTCLK (P2.8).

In addition, the following parameters are varied for timing measurements:

- Pad supply voltage VDDP0 in 2 steps: 3.3V and 5.0V.
- Capacitive load in 5 steps: 10pF, 15pF, 22pF, 33pF, 47pF
- Ambient temerature in 3 steps: -40°C, +25°C, +125°C
- For rise/fall time values at other temperatures, a linear interpolation can be done.
- Electromagnetic emission is always measured at T_A=25°C.

Load capacitors are selected in a way that together with the measurement probe capacitance of 3pF total capacitance values of 13pF up to 50pF are reached. Table 2 shows the reference between real loads and numbers given in the result diagrams. For easy reading, these capacitances are referred to the SMD capacitor values as 10, 15, 22, 33, 47pF in the result diagrams.

SMD load capacitor	Probe capacitance	Resulting physical capacitance
10pF	3 pF	13 pF
15 pF	3 pF	18 pF
22 pF	3 pF	25 pF
33 pF	3 pF	36 pF
47 pF	3 pF	50 pF

Table 2: Overview of capacitive loads used for timing measurements

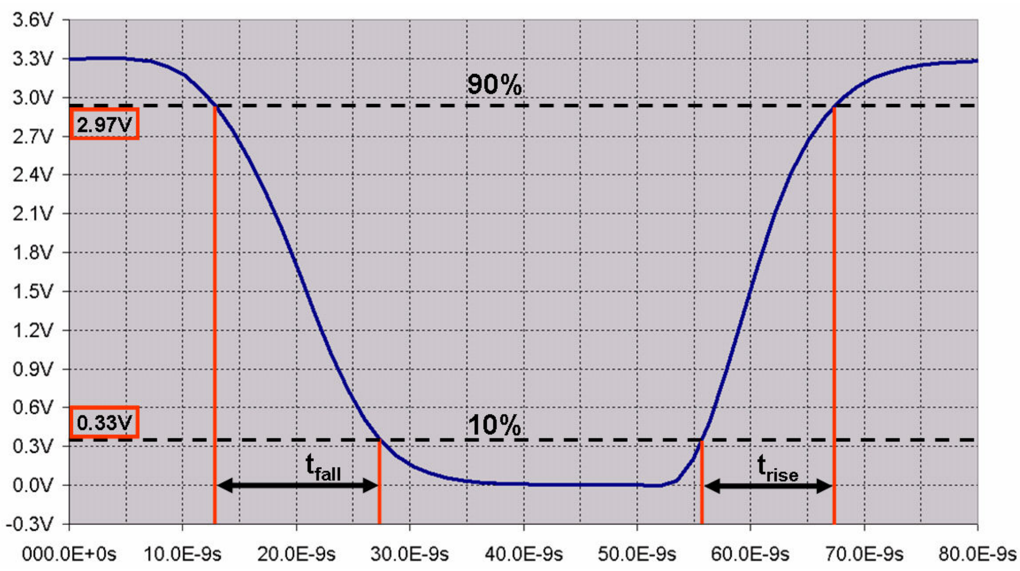

Figure 8: Voltage level references for timing measurement at VDDP0=3.3V

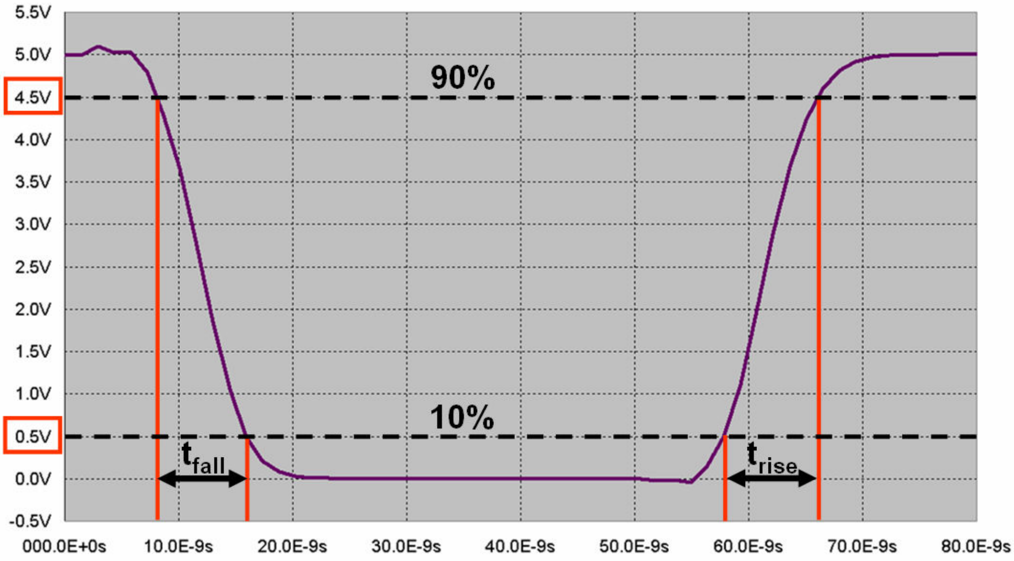

Figure 9: Voltage level references for timing measurement at VDDP0=5.0V

The results given in Table 4 and in the diagrams of Chapter 4.1.3 show the measured rising and falling edge timings. The reference points are 10% and 90% as indicated in Fig. 8 and 9.

Table 3 lists all parameter variations and test names for reference. These test names are used to indicate the driver settings and load configurations used inChapter 4.1.3. All measurements have been performed for VDDP0=3.3V and VDDP0=5.0V at ambient temperatures T_A=-40°C, 25°C and 125°C.

Test Name	Driver strength	Connected physical capacitor	Resulting load capacitance
XS-10pF	Extra-strong	10pF	13 pF
XS-15pF	Extra-strong	15 pF	18 pF
XS-22pF	Extra-strong	22 pF	25 pF
XS-33pF	Extra-strong	33 pF	36 pF
XS-47pF	Extra-strong	47 pF	50 pF
SH-10pF	Strong-sharp	10pF	13 pF
SH-15pF	Strong-sharp	15 pF	18 pF
SH-22pF	Strong-sharp	22 pF	25 pF
SH-33pF	Strong-sharp	33 pF	36 pF
SH-47pF	Strong-sharp	47 pF	50 pF
SM-10pF	Strong-medium	10pF	13 pF
SM-15pF	Strong-medium	15 pF	18 pF
SM-22pF	Strong-medium	22 pF	25 pF
SM-33pF	Strong-medium	33 pF	36 pF
SM-47pF	Strong-medium	47 pF	50 pF
SO-10pF	Strong-soft	10pF	13 pF
SO-15pF	Strong-soft	15 pF	18 pF
SO-22pF	Strong-soft	22 pF	25 pF
SO-33pF	Strong-soft	33 pF	36 pF
SO-47pF	Strong-soft	47 pF	50 pF
ME-10pF	Medium	10pF	13 pF
ME-15pF	Medium	15 pF	18 pF
ME-22pF	Medium	22 pF	25 pF
ME-33pF	Medium	33 pF	36 pF
ME-47pF	Medium	47 pF	50 pF
WE-10pF	Weak	10pF	13 pF
WE-15pF	Weak	15 pF	18 pF
WE-22pF	Weak	22 pF	25 pF
WE-33pF	Weak	33 pF	36 pF
WE-47pF	Weak	47 pF	50 pF

Table 3: Abbreviations used in the timing result diagrams

4.1.2 Rise/fall time values

Table 4 lists the measured 10% / 90% rise and fall times of all driver, voltage, load and ambient temperature conditions. The related waveform are shown in Annex A.

Driver = „Extra-sharp"; VDDP0 = 3.3V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	2.03	1.85	2.53	2.29	3.03	2.57	3.82	3.17	4.86	4.02
+25	2.24	1.94	4	2.82	4.17	2.9	4.86	3.68	5.8	4.39
+125	3.62	2.17	4.45	3.08	4.87	4.08	5.89	4.6	7.1	5.69

Driver = „Extra-sharp"; VDDP0 = 5.0V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	1.62	1.58	1.94	1.91	2.09	2.12	2.56	2.52	3.21	3.21
+25	1.77	1.63	2.16	2.23	2.22	2.25	2.76	2.73	3.43	3.42
+125	1.8	1.68	2.46	2.29	2.88	2.96	3.69	3.43	4.39	3.98

Driver = „Strong-sharp"; VDDP0 = 3.3V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	4.38	4.73	5.06	5.39	6.34	5.9	7.36	6.46	9.29	7.7
+25	5.3	5.53	7.23	6.6	7.15	6.85	8.65	7.75	10.43	8.57
+125	6.2	6.05	8.06	7.46	9.27	8.38	10.8	9.24	12.48	10.34

Driver = „Strong-sharp"; VDDP0 = 5.0V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	2.63	3.49	3.55	3.76	3.99	4.15	4.64	4.83	5.64	5.62
+25	3.29	3.81	4.33	4.63	4.42	4.6	5.15	5.33	6.58	6.53
+125	3.99	4.47	5	5.23	5.91	5.93	7.38	7	8.62	7.72

Driver = „Strong-medium"; VDDP0 = 3.3V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	9.85	9.49	10.45	10.2	11.55	11	12.26	11.6	14	13.06
+25	11.94	11.01	13.35	12.23	14.1	12.7	13.9	13.85	16.6	15.28
+125	13.6	13.05	16.24	14.6	18.19	16.24	19.2	16.86	20.46	17.85

Driver = „Strong-medium"; VDDP0 = 5.0V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	5.89	6.09	6.56	6.7	6.89	6.91	7.5	7.7	8.9	8.93
+25	6.85	6.84	8.05	8.15	8.28	8.14	9.15	8.92	10.35	10.2
+125	8.77	8.4	10.09	9.69	11.2	10.51	12.69	11.69	13.1	12.59

Driver = „Strong-soft“; VDDP0 = 3.3V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	13.7	13.7	14.8	15.02	16.38	16.34	16.6	16.4	19.06	17.66
+25	16	15.44	17.9	18.08	18.75	18.55	19.7	19.5	21	20.63
+125	18.62	18.42	21.58	21	24.15	21.91	26.84	24.6	25.49	24.86

Driver = „Strong-soft“; VDDP0 = 5.0V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	8.08	8.49	8.97	9.26	9.3	9.7	9.94	10.49	11.2	11.47
+25	9.3	9.73	10.75	11	11.13	11.32	11.65	12.15	13	13.25
+125	11.92	11.73	13.9	12.92	14.91	14.49	16.6	15.59	17	16.2

Driver = „Medium“; VDDP0 = 3.3V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	21.6	25.4	25.4	27.05	28.29	30.55	31.56	34.06	37.8	38.24
+25	25.86	29.2	32.1	34.7	33.9	35.5	38.1	38.95	42.13	42.68
+125	30.6	34.24	38.2	40.4	43.59	45.15	49.04	49.24	54.12	51.24

Driver = „Medium“; VDDP0 = 5.0V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	14.2	17.25	16.41	19.32	18.34	20.66	20.89	23.31	24.99	27.29
+25	16.01	18.8	22	23.73	21.3	23.47	24.6	26.8	29	30.8
+125	20.8	23.29	24.73	27.8	28	31	32.6	35.19	36.09	37.89

Driver = „Weak“; VDDP0 = 3.3V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	121	278.64	137.6	276.92	145.68	279.69	161.09	290.13	187.25	314.9
+25	142	312.46	169.15	334.5	174.9	348.37	197.95	357.5	219.2	349.88
+125	163	370.44	195.92	393.11	216.67	425.59	247.04	436.91	266	432.24

Driver = „Weak“; VDDP0 = 5.0V

	C_L=10pF		C_L=15pF		C_L=22pF		C_L=33pF		C_L=47pF	
T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)	t_R (ns)	T_A (°C)	t_R (ns)	t_F (ns)	t_R (ns)	t_F (ns)
-40	75.01	137.61	90.41	148	93	147.41	103.61	150.1	120.21	170.2
+25	85.21	154.93	108	175.4	108.85	173.25	125.5	185.45	141.05	203.1
+125	108.2	193.69	126.21	214.6	142.59	223.61	163.21	243.09	174.4	246.21

Table 4: Measured rise/fall times

4.1.3 Rise/fall time diagrams

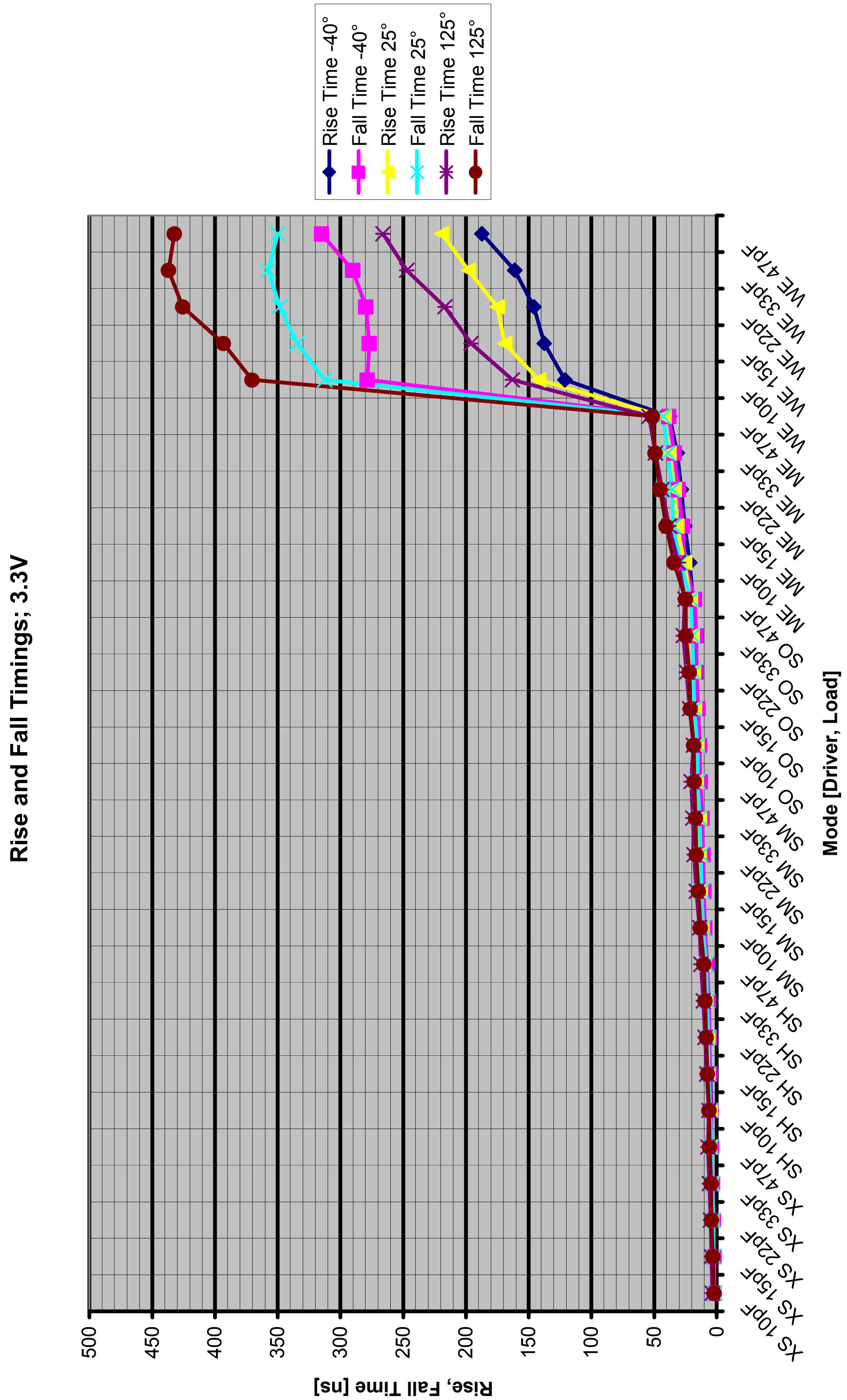

Figure 10: Rise/fall time values for all driver settings at VDDP0=3.3V

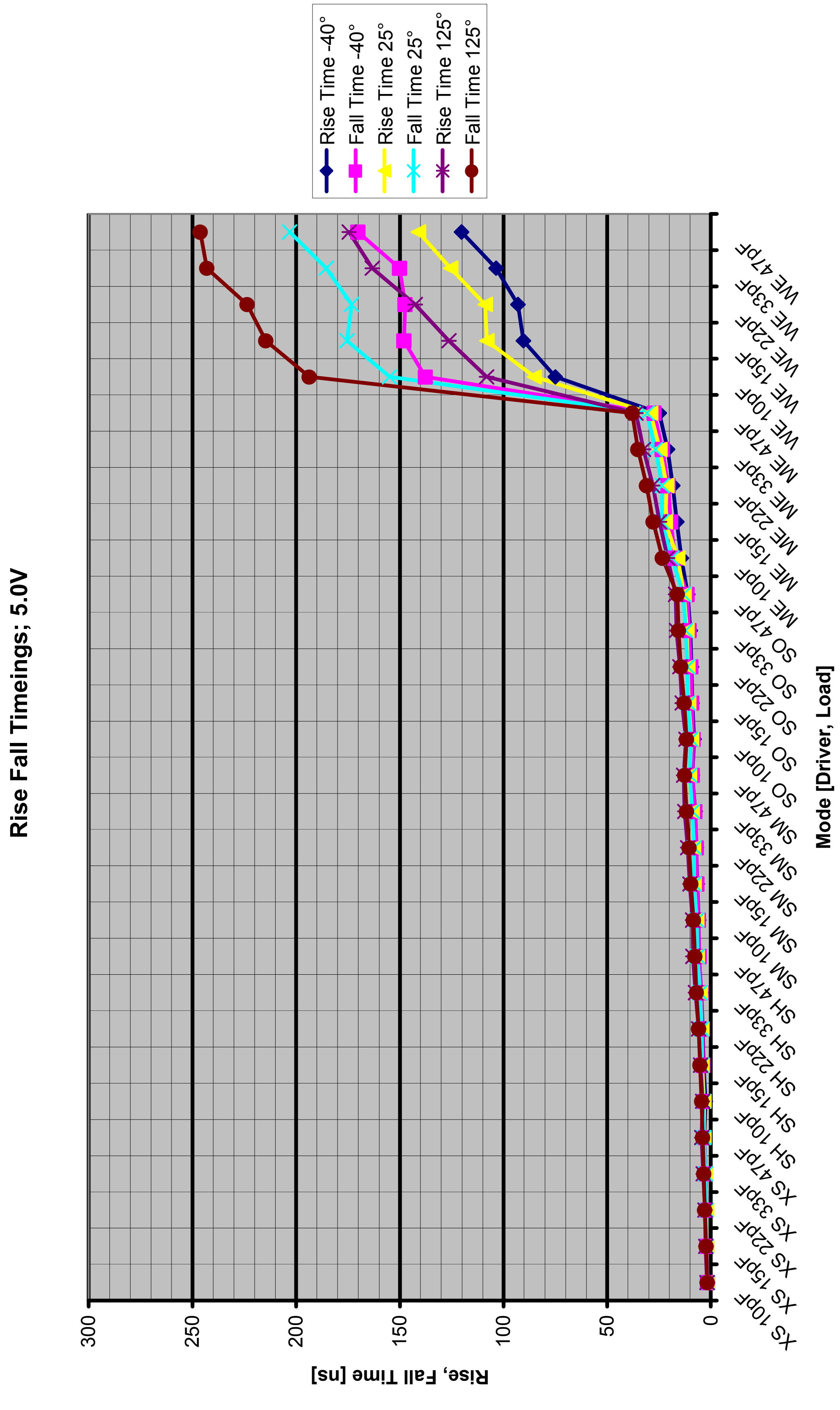

Figure 11: Rise/fall time values for all driver settings at VDDP0=5.0V

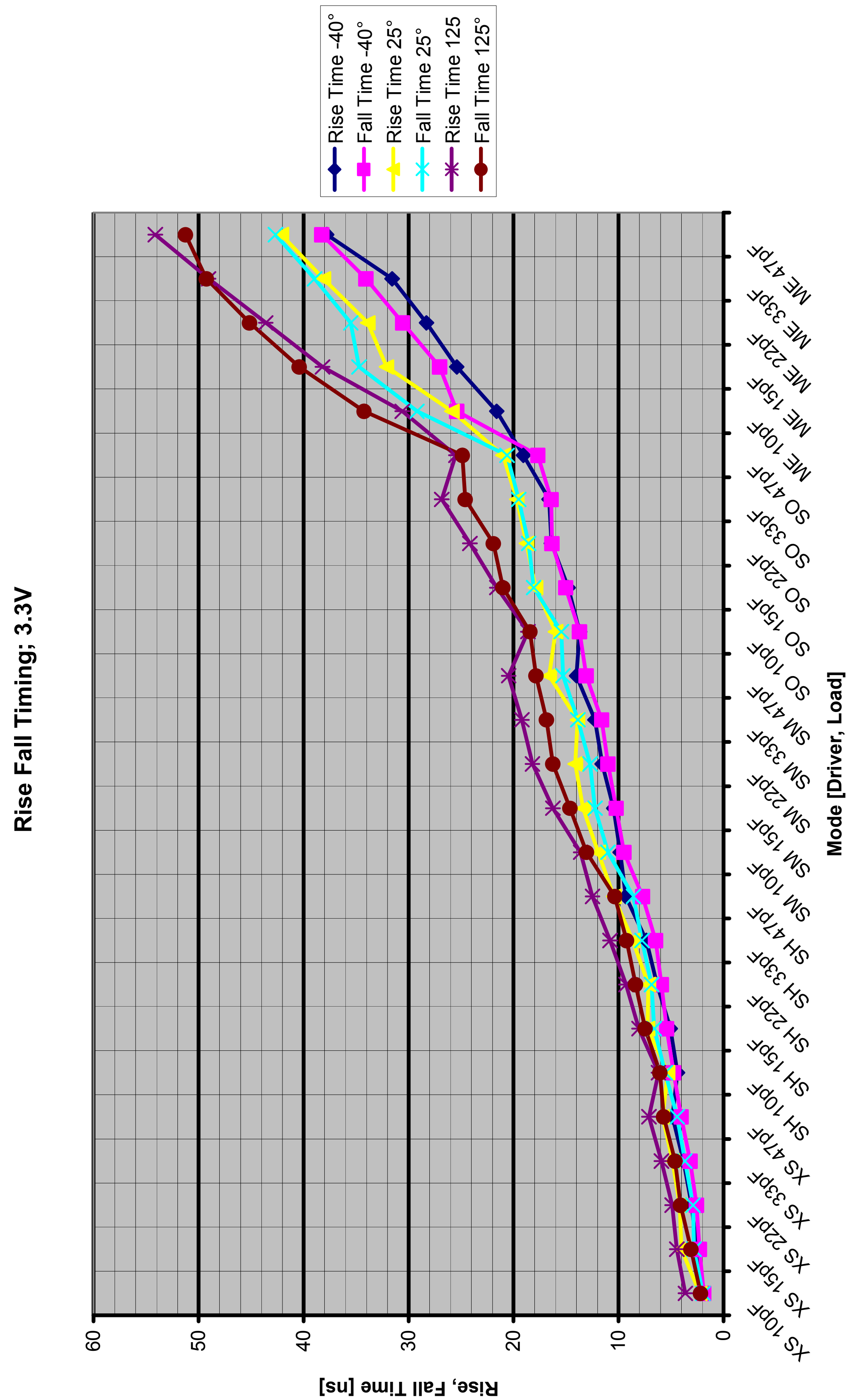

Figure 12: Rise/fall time values for all but weak driver settings at VDDP0=3.3V

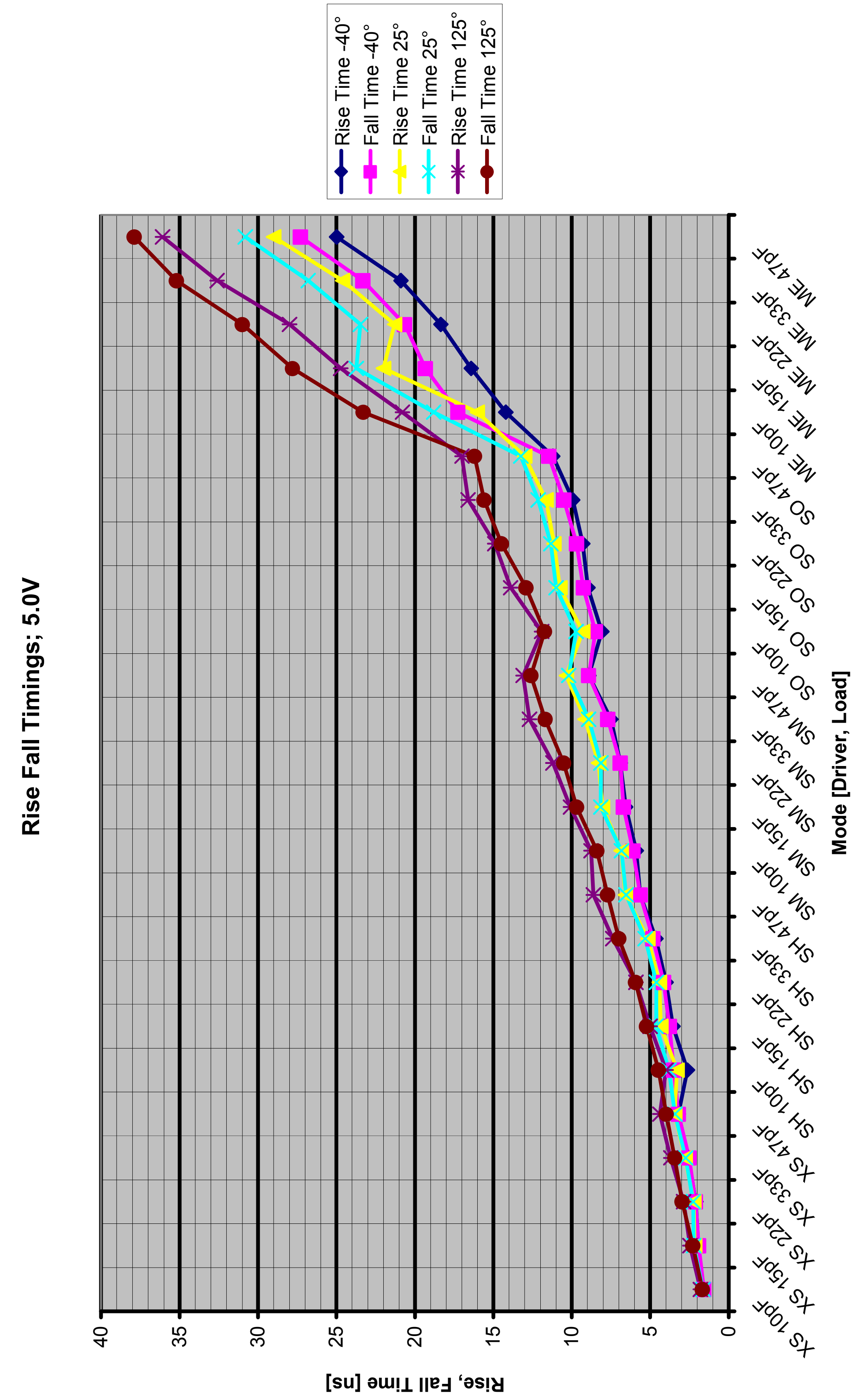

Figure 13: Rise/fall time values for all but weak driver settings at VDDP0=5.0V

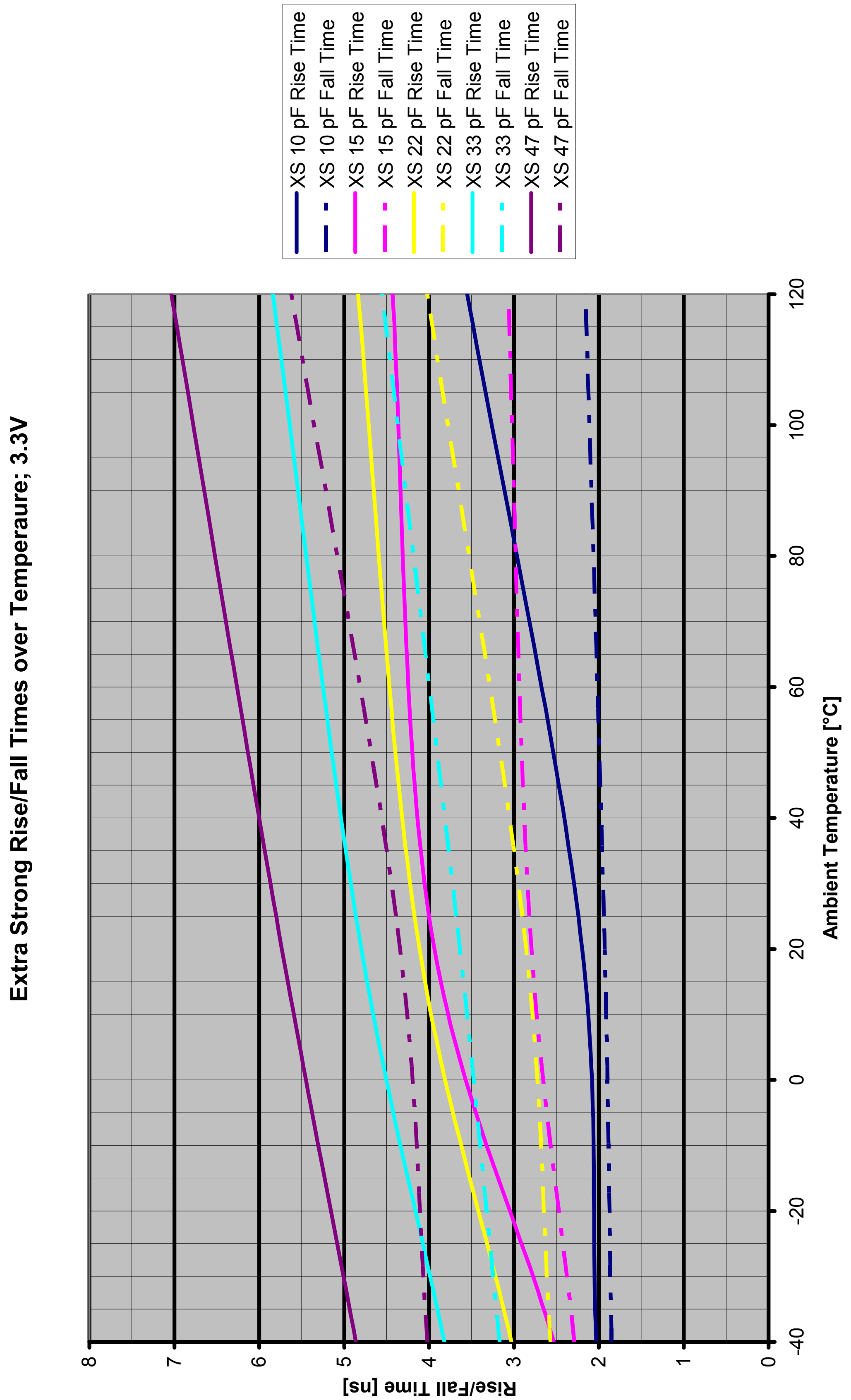

Figure 14: Rise/fall time values for extra-strong driver over temperature at VDDP0=3.3V

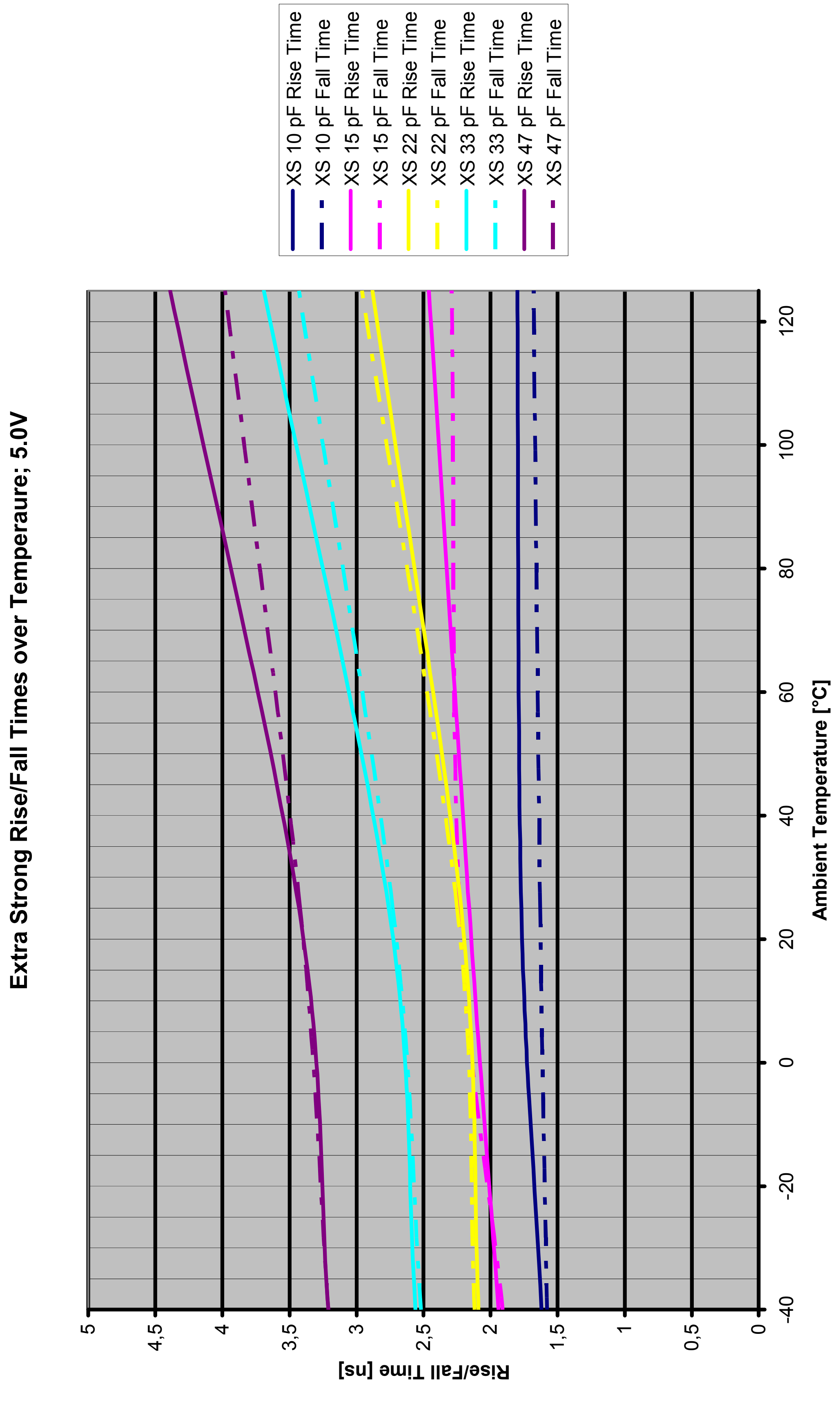

Figure 15: Rise/fall time values for extra-strong driver over temperature at VDDP0=5.0V

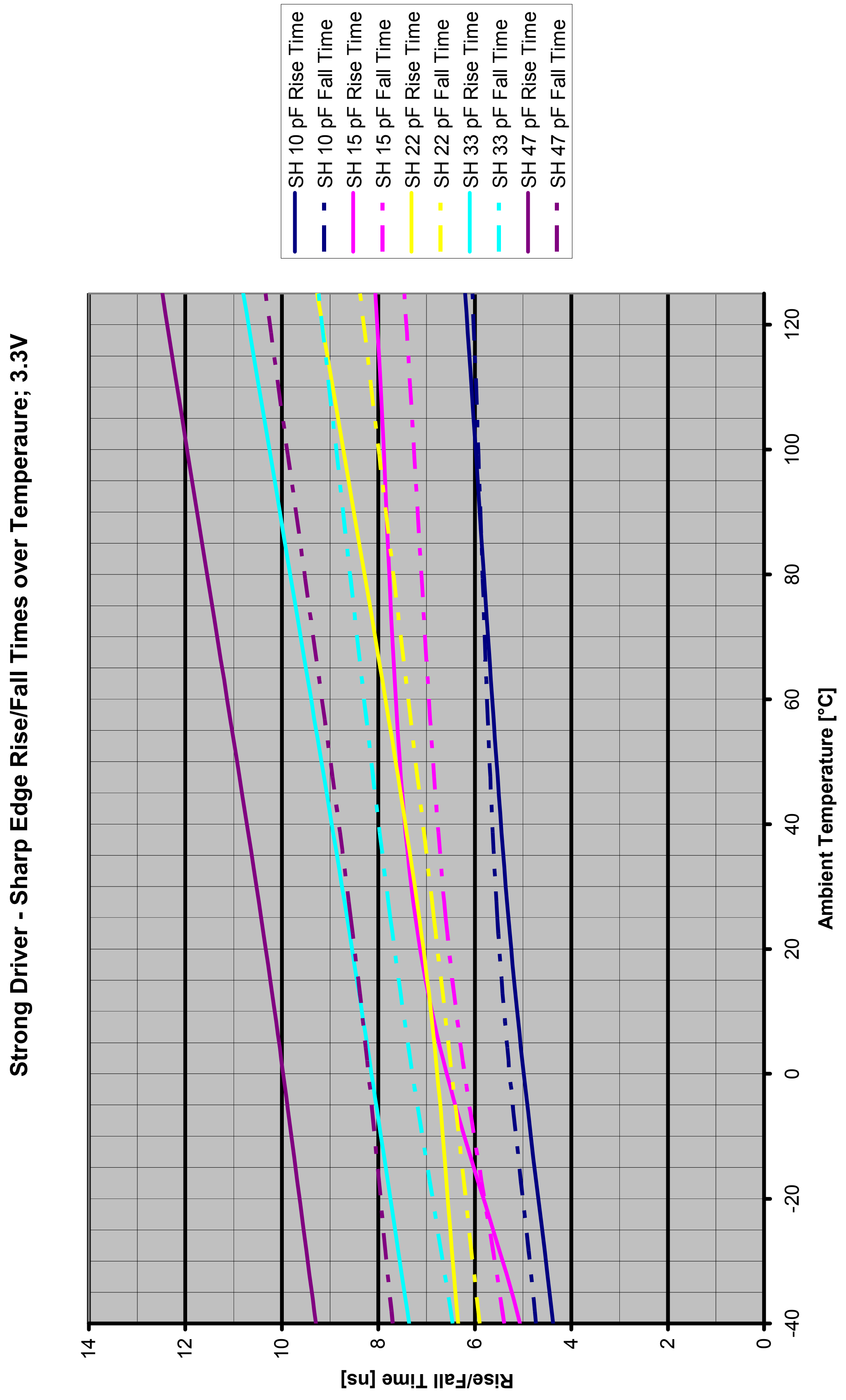

Figure 16: Rise/fall time values for strong-sharp driver over temperature at VDDP0=3.3V

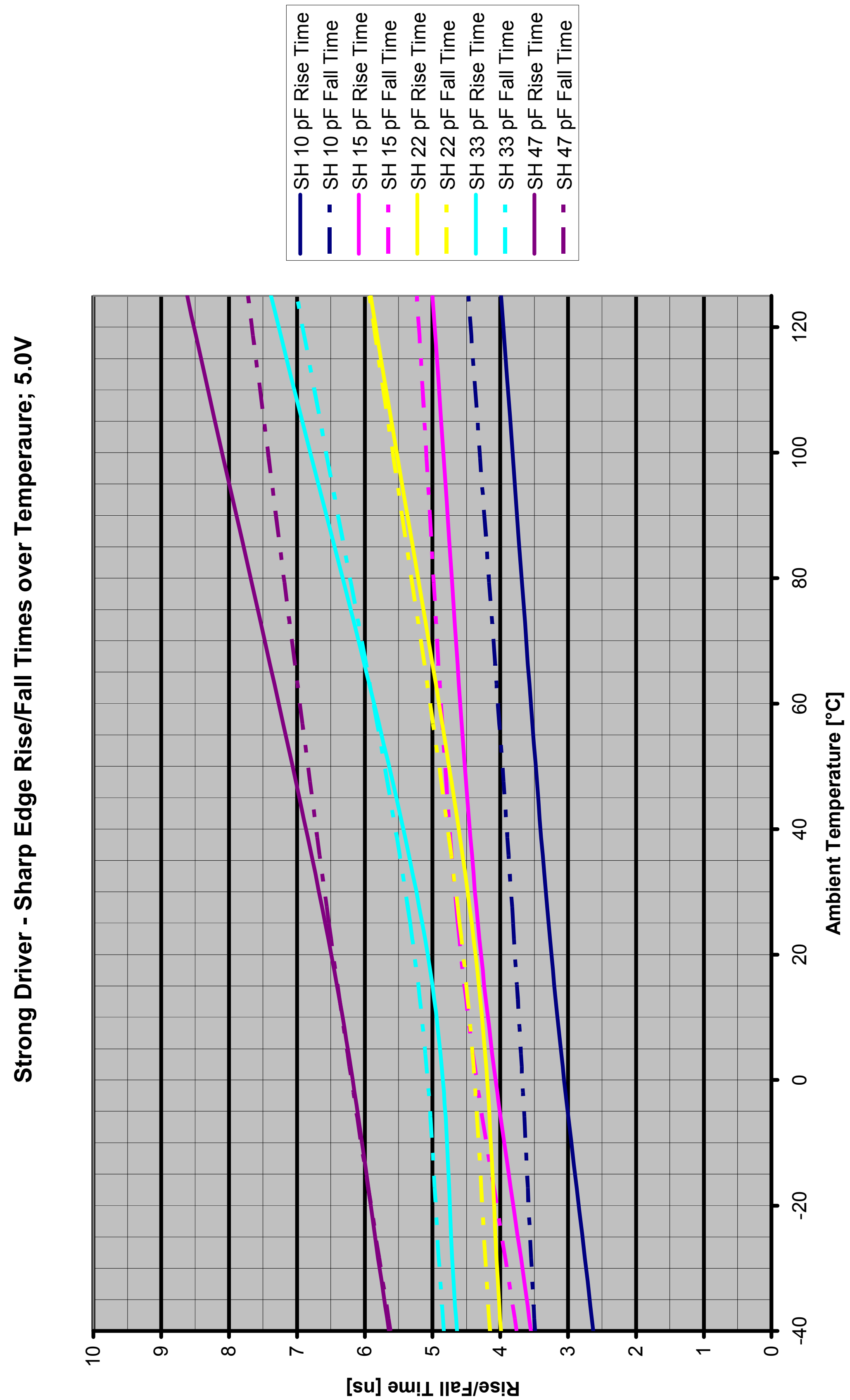

Figure 17: Rise/fall time values for strong-sharp driver over temperature at VDDP0=5.0V

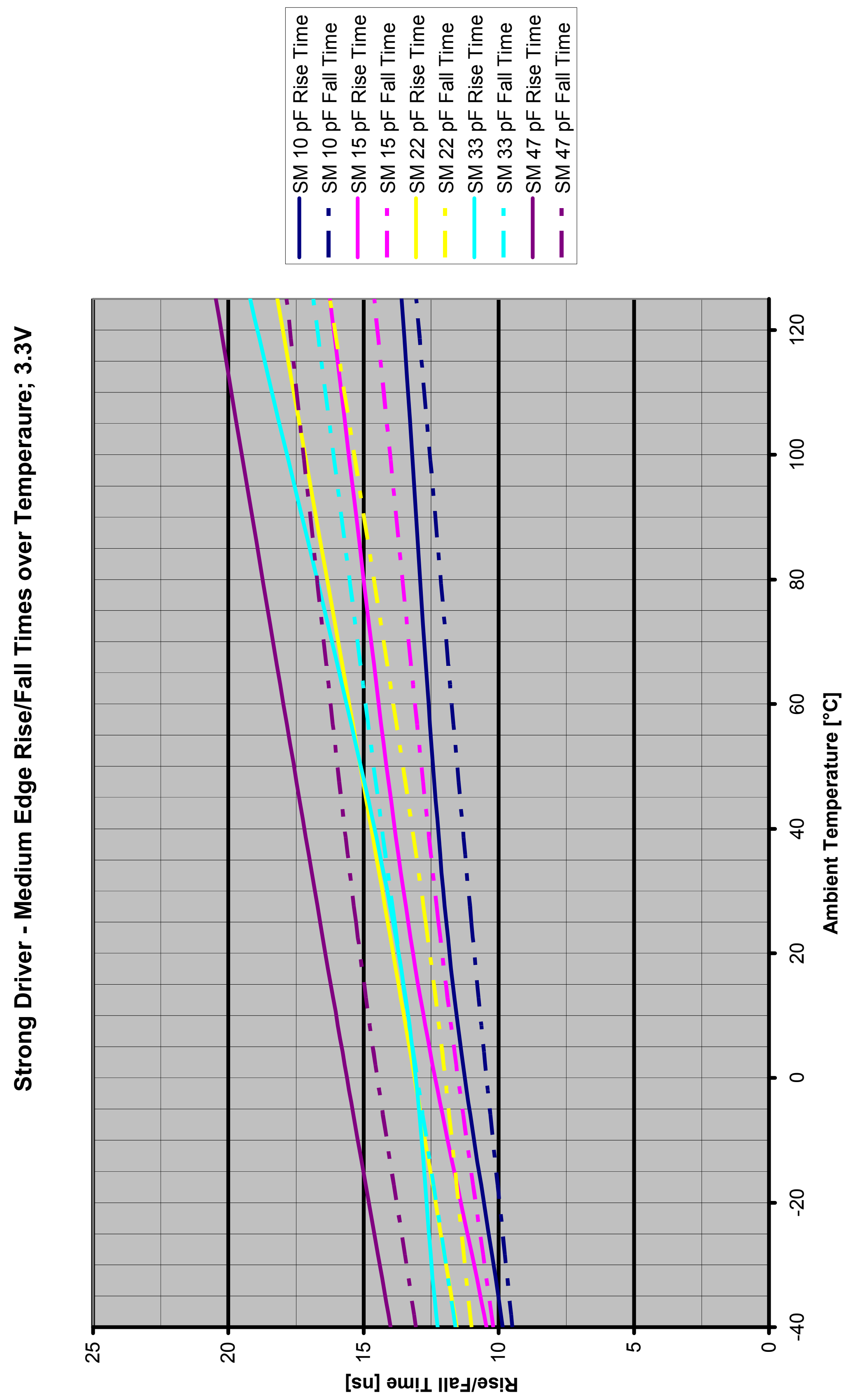

Figure 18: Rise/fall time values for strong-medium driver over temperature at VDDP0=3.3V

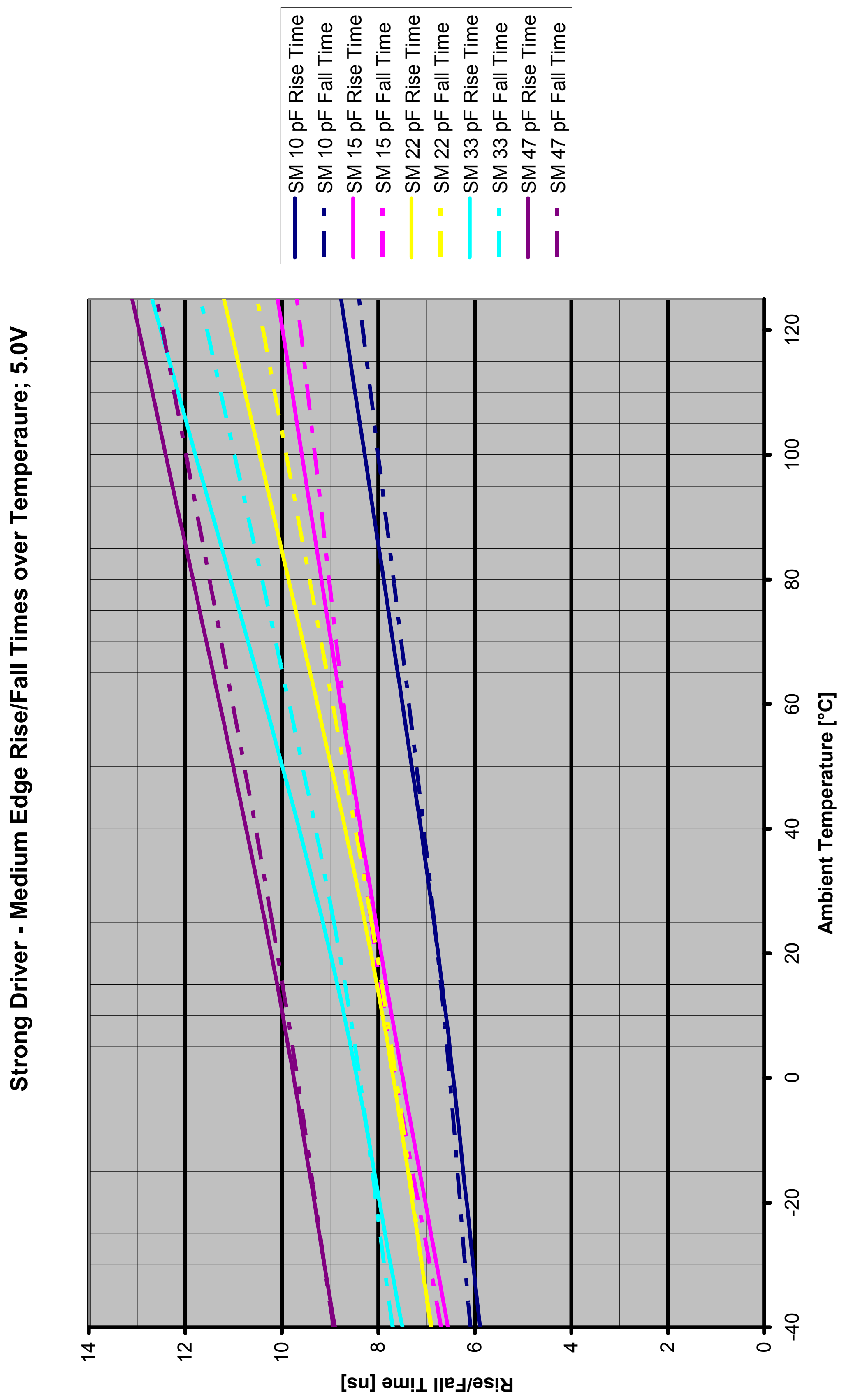

Figure 19: Rise/fall time values for strong-medium driver over temperature at VDDP0=5.0V

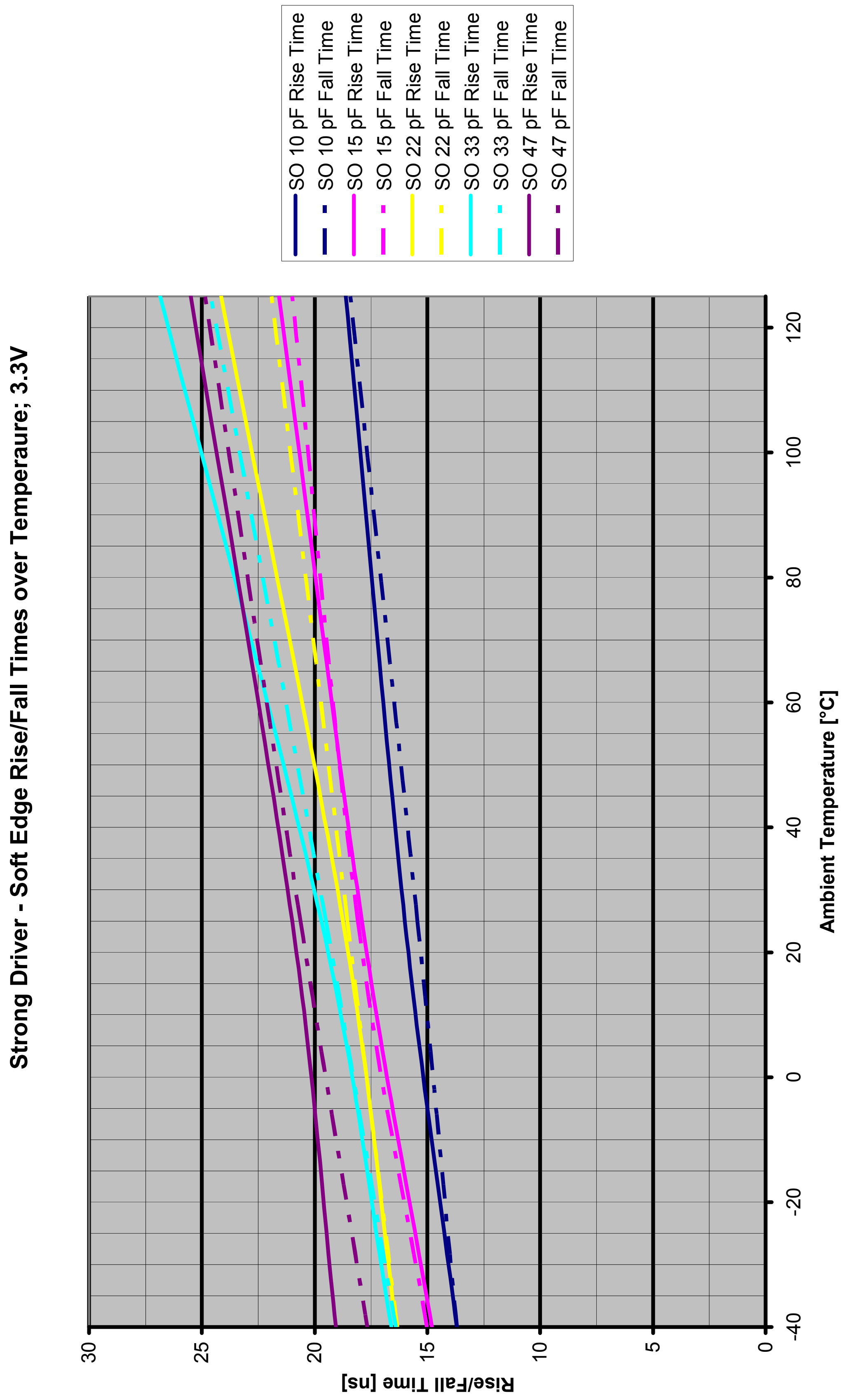

Figure 20: Rise/fall time values for strong-soft driver over temperature at VDDP0=3.3V

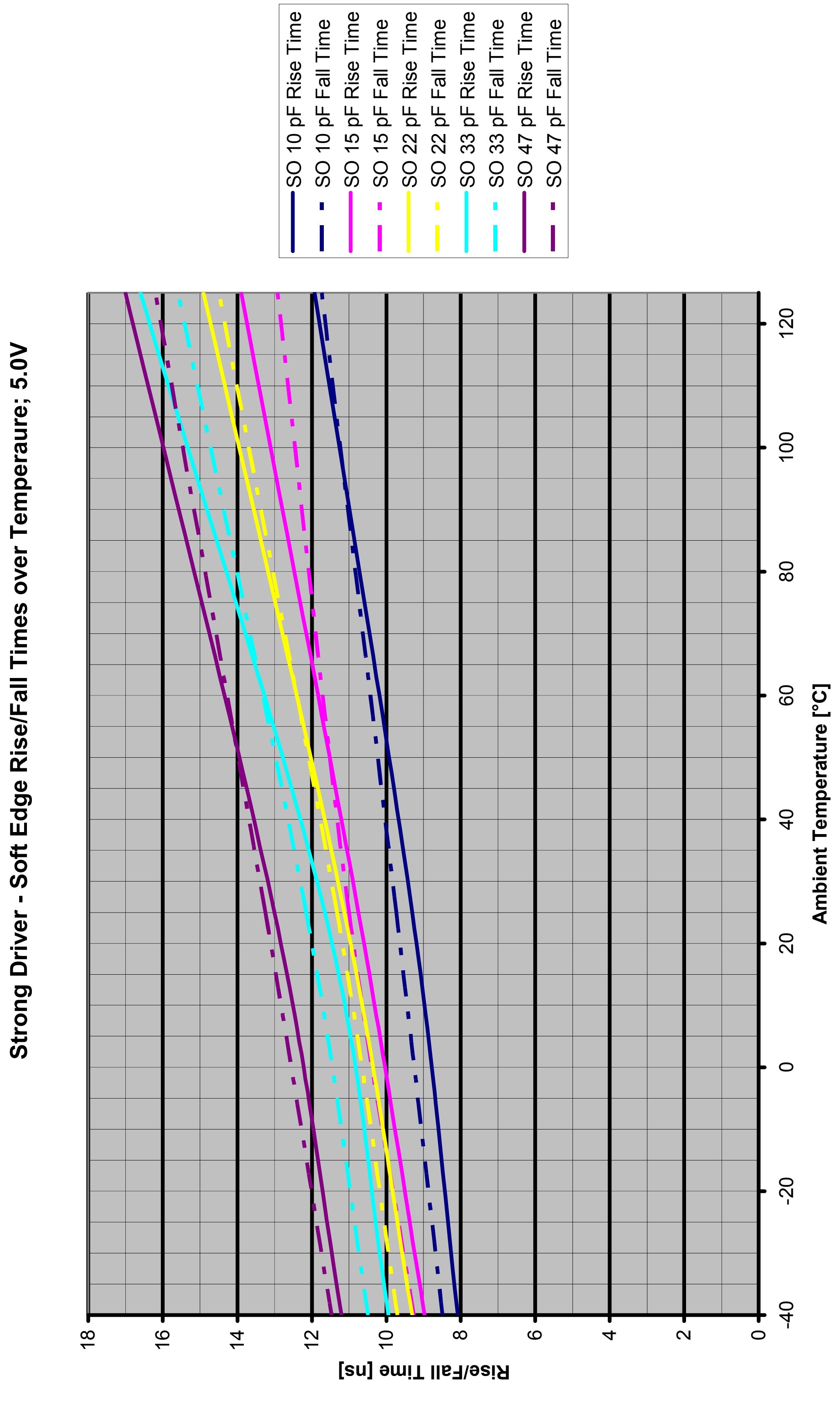

Figure 21: Rise/fall time values for strong-soft driver over temperature at VDDP0=5.0V

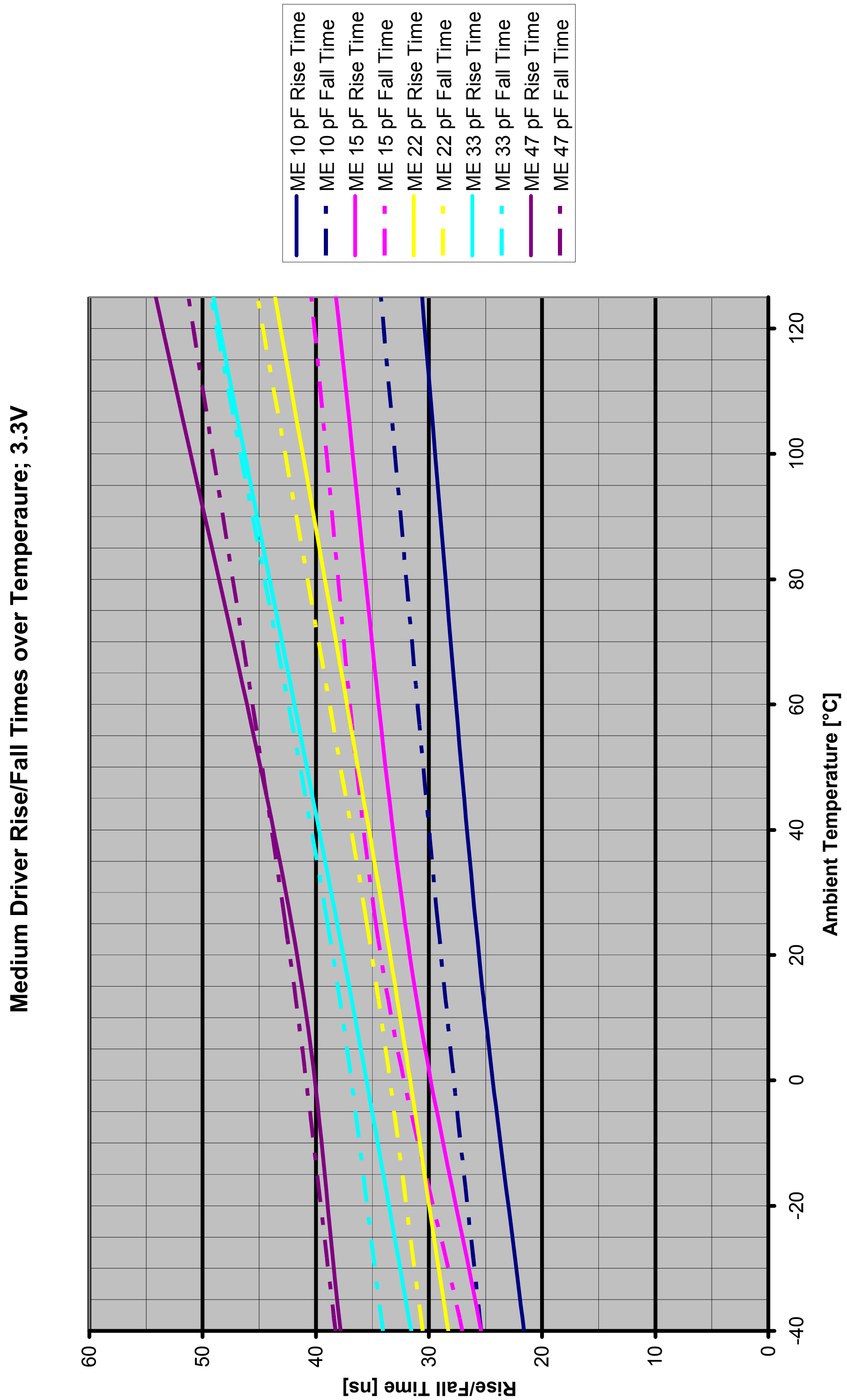

Figure 22: Rise/fall time values for medium driver over temperature at VDDP0=3.3V

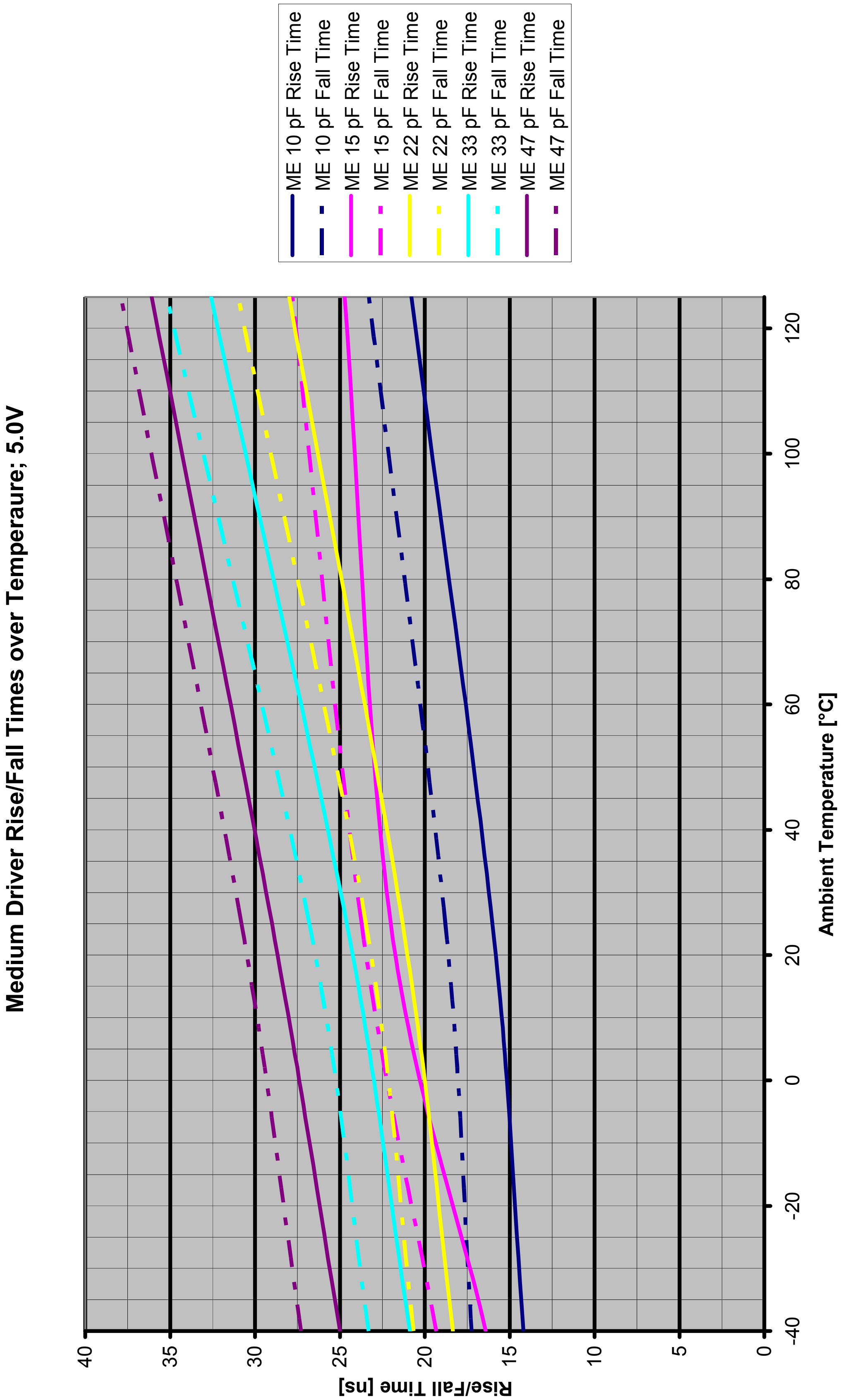

Figure 23: Rise/fall time values for medium driver over temperature at VDDP0=5.0V

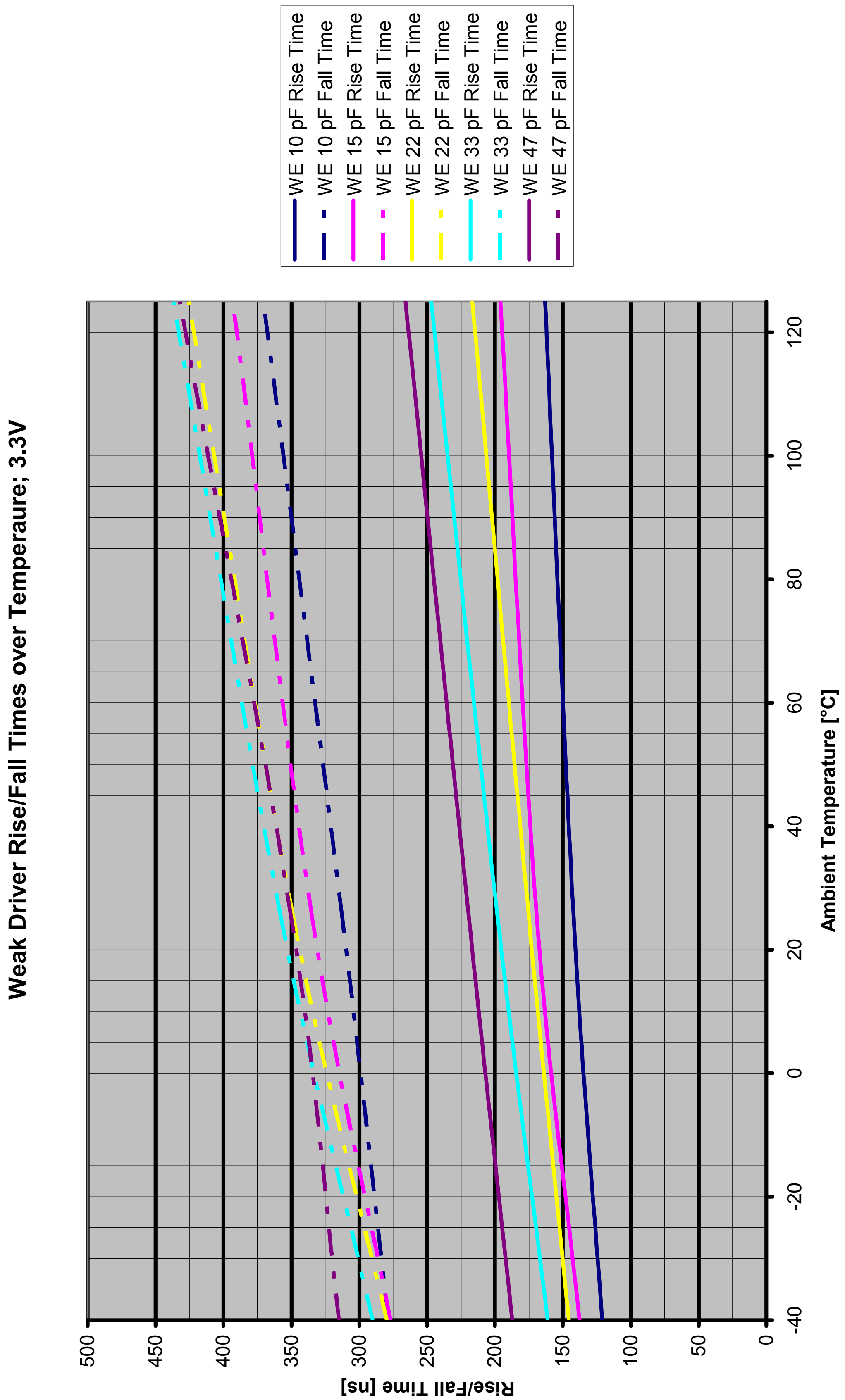

Figure 24: Rise/fall time values for weak driver over temperature at VDDP0=5.0V

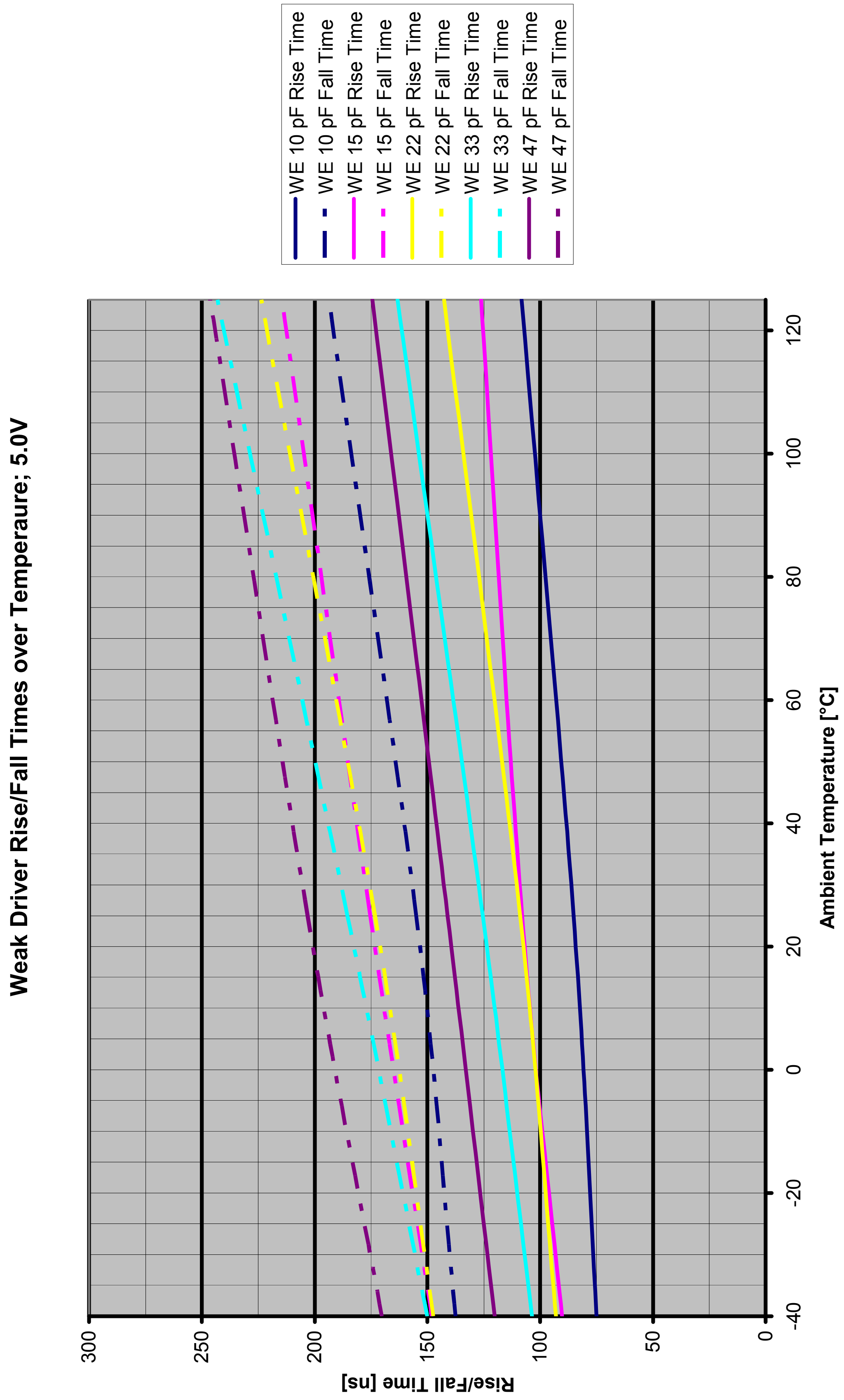

Figure 25: Rise/fall time values for weak driver over temperature at VDDP0=5.0V

5 Measured Electromagnetic Emission

In addition to signal integrity, the scaling of pad drivers helps to reduce electromagnetic emission (EME) caused by switching output pins. This is because slower signal edges produce less high frequency contents in the emission spectra.

The following rule should be obeyed when selecting pad driver strength:

Use the weakest/slowest driver setting which provides the required signal timing at worst-case operating conditions.

Worst-case operating conditions wrt. timing are:

- maximal ambient temperature (+125°C)
- minimal pad supply voltage (3.3V)
- realistic capacitive output load (consider trace length and structure, receiver input loads)
- weak driver settings

Worst-case operating conditions wrt. electromagnetic emission are:

- minimal ambient temperature (-40°C)
- maximal pad supply voltage (5.0V)
- extra-strong driver settings

To illustrate the benefits of driver scaling for low EME, some sample measurement results are provided.

The measurements have been performed under the following operating conditions:

EXTCLK (Port 2.8) is toggling at maximal possible data rate of selected driver with capacitive loads of 10pF and 47pF.

All other I/Os are inactive.

The core is running in idle loop.
Conducted emission is measured at pad supply (VDDP0) according to chapter 5.1.1.

Radiated emission is measured in mini-TEM cell according to chapter 5.1.2.

5.1 Description of test equipment

5.1.1 Conducted emission test configuration

Conducted emission is measured using the standardized 150Ω network, see Fig. 26. This network is used for both port and power supply emission measurements. The frequency range is from 150kHz to 1000MHz.

For reference purpose, only the emission measured on the supply domains VDDP0 is documented. Emission reduction can be observed in a similar way on other power supply domains and on passive (i.e. non-switching) pad pins.

150Ω networks are provided for conducted emission measurements according IEC 61967 part 4 and BISS emission test specification.

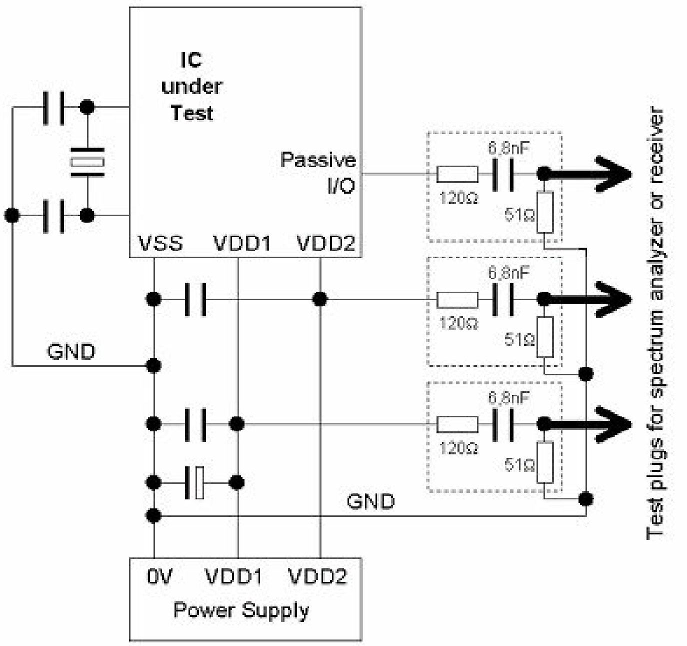

Figure 26: Conducted emission probing points

5.1.2 Radiated emission test configuration

Radiated emission is measured using the standard Mini TEM Cell according IEC 61967 part 2 and BISS emission test specification. The frequency range is from 150kHz to 1000MHz.

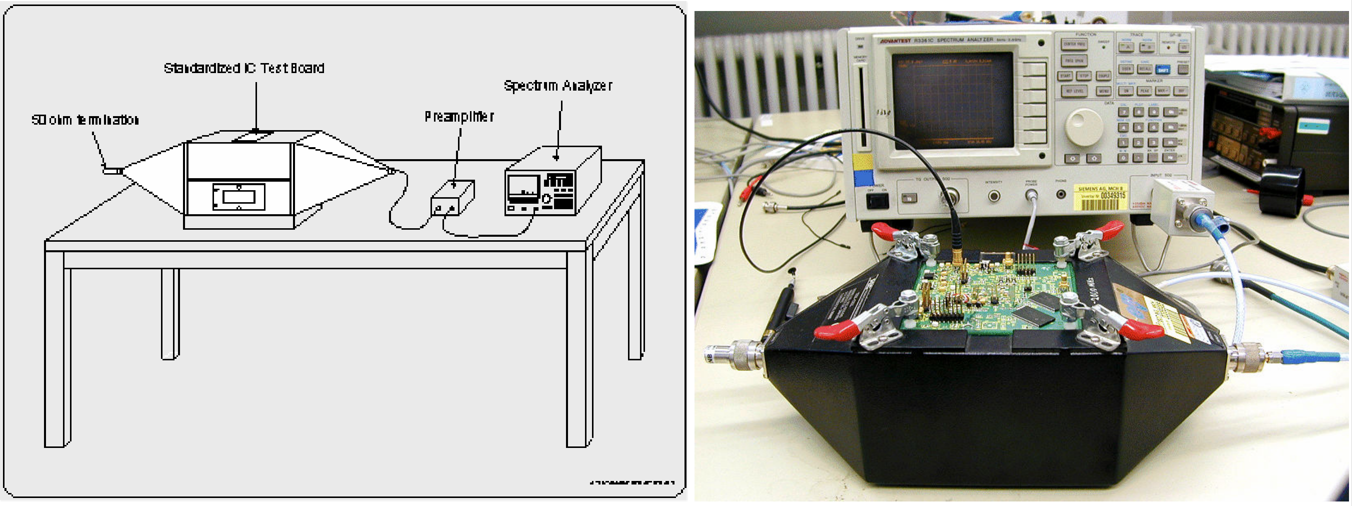

Figure 27: Radiated emission test setup

5.1.3 Instruments and software for emission data recognition

Spectrum analyzer:	Rohde & Schwarz FSP7
Detector type:	Peak detector
Pre-Amplifier:	internal
Measurement time:	For all measurements, the emission measurement time (10ms) at one frequency is longer than the test software loop duration.
Data generation software:	Rohde&Schwarz EMIPAK 9950
Environment:	temperature 23°C ±5°C
Supply:	nominal voltage ±5%

<table>
<tr><th colspan="5" rowspan="2">Frequency range</th><th colspan="2">Spectrum Analyzer</th></tr>
<tr><th>RBW</th><th>Sweep time*</th></tr>
<tr><td rowspan="3">150 Ω</td><td rowspan="3">TEM</td><td>150 kHz</td><td>to</td><td>30 MHz</td><td rowspan="3">10kHz</td><td rowspan="3">$t_s = \frac{NP \cdot LT \cdot FR}{RBW}$</td></tr>
<tr><td>30 MHz</td><td>to</td><td>200 MHz</td></tr>
<tr><td>200 MHz</td><td>to</td><td>1000 MHz</td></tr>
</table>

Table 5: Spectrum analyzer settings for EME measurements

*) NP=number of points; LT=loop time; FR=frequency range

5.2 Emission test result discussion

The detailled measured emission spectra are given in Annex B.

The comparison diagrams in Fig. 28 to 33 explain typical trends and benefits when using pad driver scaling. Pin EXTCLK (Port 2.8) is toggling at different data rates which have been selected according the driver capability wrt. to driver scaling, driver supply voltage VDDP0, external load and temperature. In all cases the external load was 10pF. All emission measurements have been performed on the XC2267/XC2287.

The system clock frequency has been selected to be identical to the EXTCLK clock rate in case the latter one is above or equal to 20MHz. For lower EXTCLK clk rates, the system clock frequency stays at 20MHz. The data rates vary from 66MHz (EXTRA-STRONG driver) down to 500kHz (WEAK driver). Emissions are measured either directly on VDDP0 (conducted. Shown are the peak envelope lines which connect all peak emission values of the clock rate harmonics.

Fig. 28 compares the conducted electromagnetic emission caused by all 6 driver settings which is visible on the VDDP0 net. The driver supply voltage VDDP0 is 5.0V.

Weak and medium driver settings cause no significant emission. All stronger settings need to be used with care and only where necessary because up to more than 30dB increased emission of the application must be anticipated when using strong driver settings.

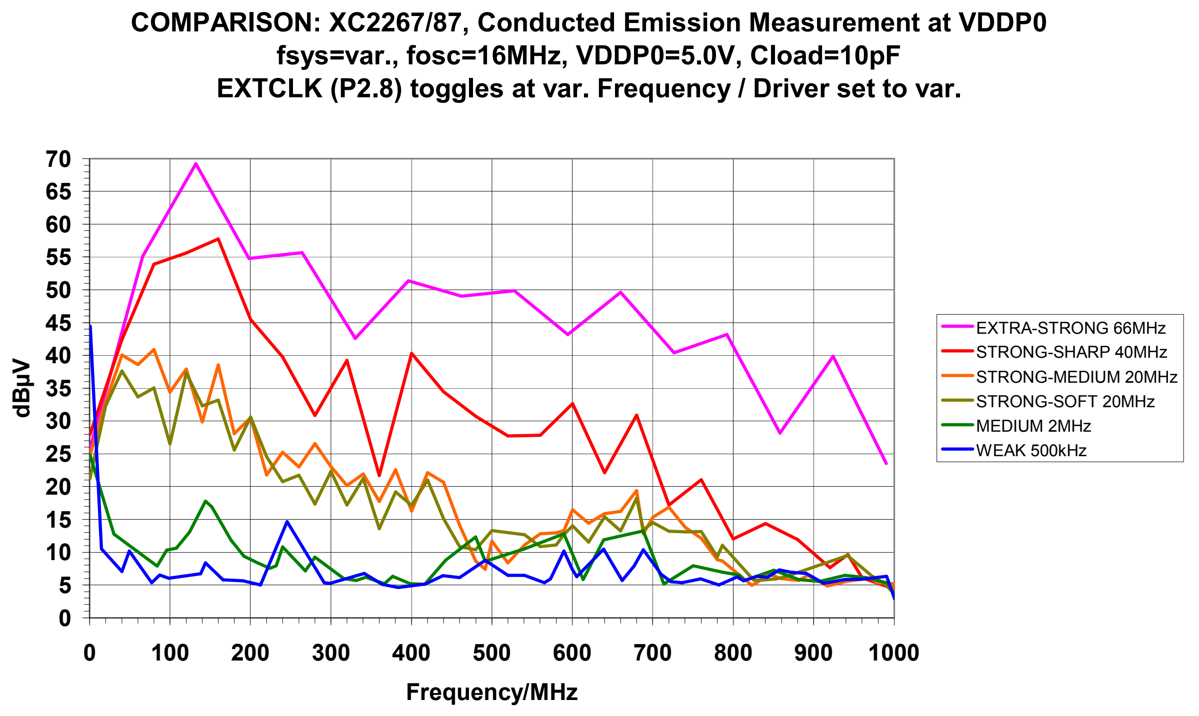

Figure 28: Conducted emission Spectra for different drivers at 10pF/5.0V

Fig. 29 compares the radiated electromagnetic emission caused by all 6 driver settings. The driver supply voltage VDDP0 is 5.0V.

Generally the radiated emission levels stay below the conducted emission levels by roughly 10dB in the base frequency range. From ca. 200MHz to 500MHz, the TEM cell radiation is slightly higher than the conducted one. Above 500MHz the two emission types arre comparable. Beside these facts, the same observations and recommendations as for conducted emission hold true. Weak and medium driver settings cause no significant emission. All stronger settings need to be used with care and only where necessary because up to more than 30dB increased emission of the application must be anticipated when using strong driver settings.

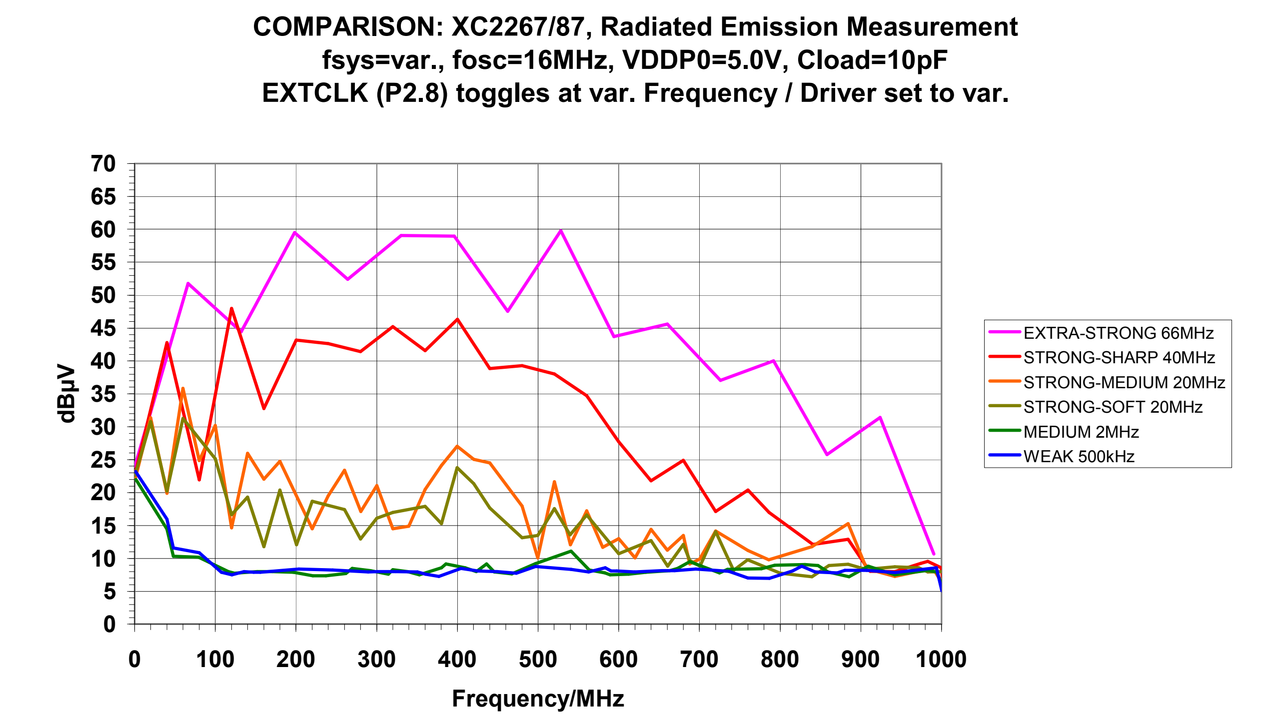

Figure 29: Radiated emission Spectra for different drivers at 10pF/5.0V

If the pad operating voltage VDDP0 is reduced from 5.0V to 3.3V, the conducted and radiated emissions drop down by roughly 6-10dB, as it is shown in Fig. 30 for conducted and in Fig. 31 for radiated emission.

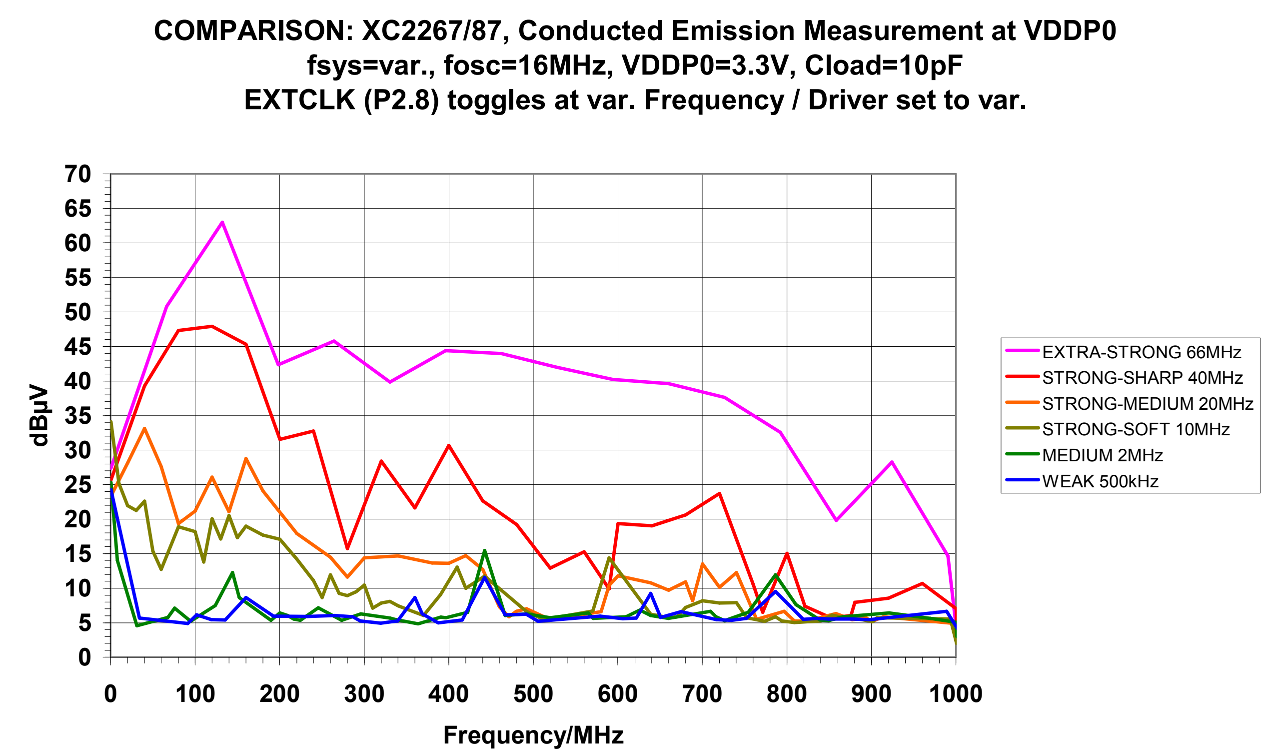

Figure 30: Conducted emission Spectra for different drivers at 10pF/3.3V

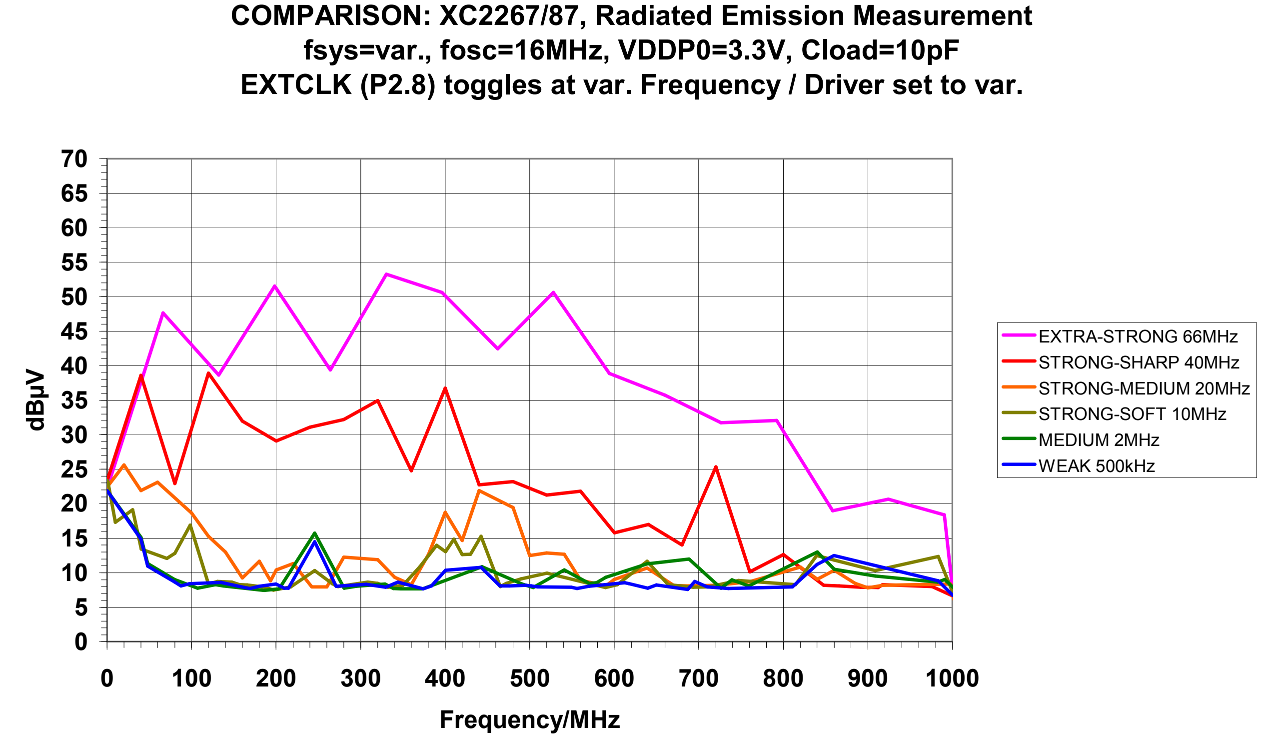

Figure 31: Radiated emission Spectra for different drivers at 10pF/3.3V

Fig. 32 and 33 compare the emission peaks of 5.0V and 3.3V driver operation, indicating a roughly 6-10dB benefit for the reduced VDDP0 voltage.

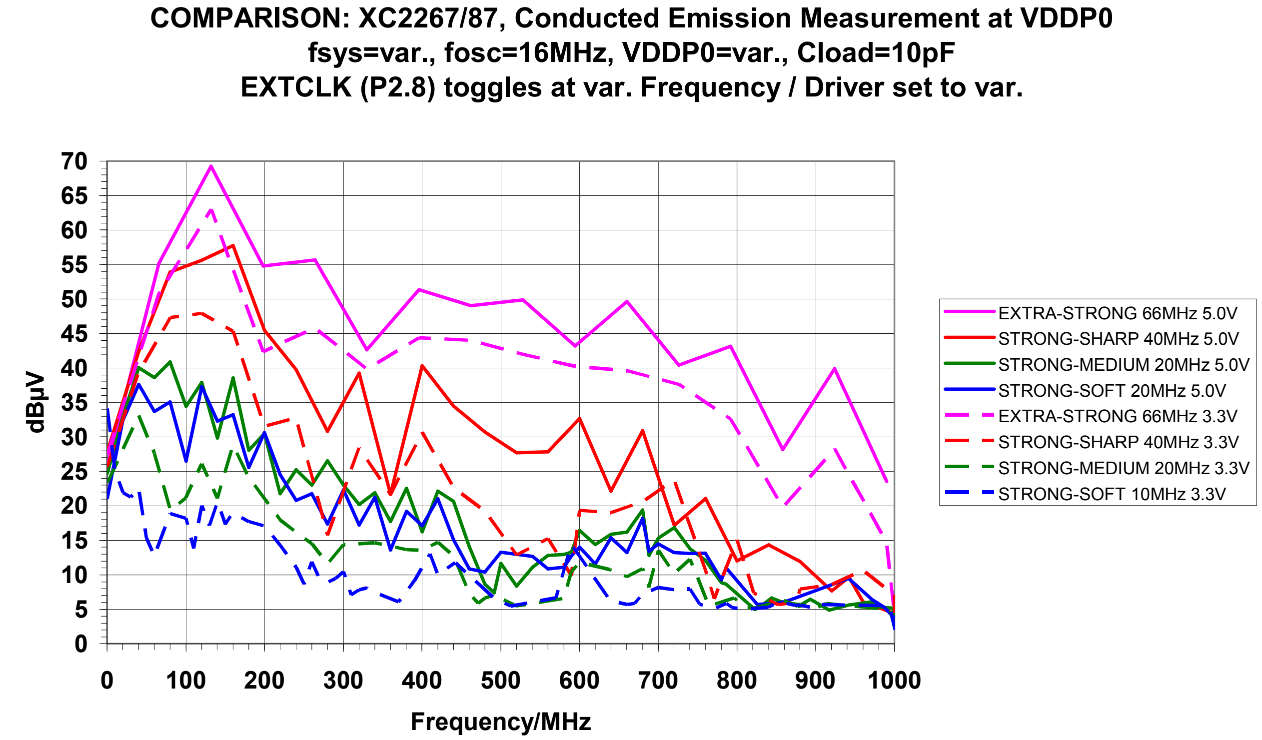

Figure 32: Conducted emission Spectra for different drivers at 10pF/3.3V and 5.0V

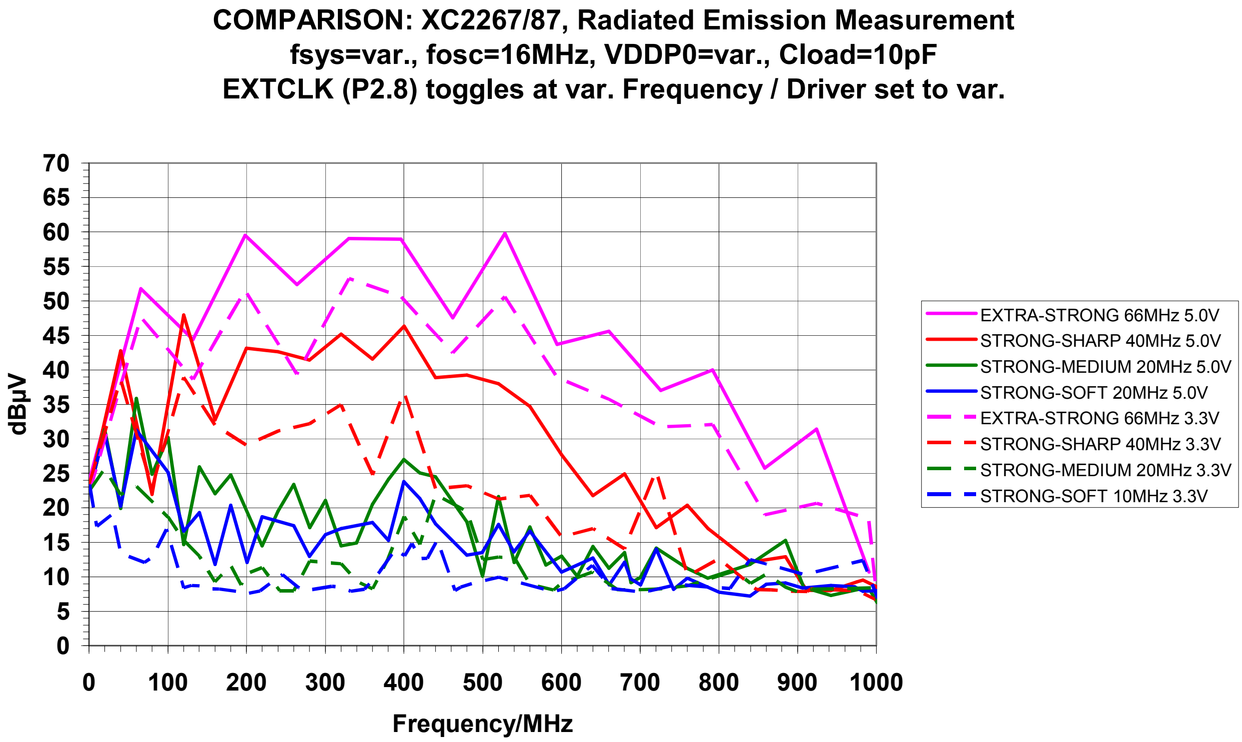

Figure 33: Radiated emission Spectra for different drivers at 10pF/3.3V and 5.0V

Conclusions:

Generally all strong driver settings (strong-soft, strong-medium, strong-sharp and extra-strong) lead to considerable emission. Consequently, all “low-rate” signals up to ca. 2MHz should be driven by medium or weak drivers. All “high-rate” signals above ca. 2MHz require strong driver settings in order to achieve good signal integrity. Nevertheless, the slowest slew rate which provides sufficient signal integrity should be selected. Up to ca. 10MHz, this is the strong-soft setting. Strong-medium and above settings should only be used in exceptional cases when a fast system clock needs to be driven across the system board or a high-speed memory bus is operated. Detailed selection diagrams for the recommended driver settings depending on given data rates are provided in Chapter 6.

6 Recommended Settings for Signal Categories

6.1 General

In the previous chapters, many detailed data was provided for the impact of driver settings and load capacitance on the resulting rise and fall times as well as on conducted and radiated emission.

Generally, the required signal integrity determines the selection of driver strength and slew rate for a given toggle rate and capacitive load. However, due to the simultaneous impact on electromagnetic emission, the weakest possible driver setting which still meets the signal integrity should be chosen.

To decide for the proper pad driver settings for a signal, its electrical characteristics should be considered. This leads to the definition of signal categories by means of clock or data transfer (AC view) or current driving capability (DC view). According to these views, any signal can be classified as shown in Table 6.

Signal category	Clock rate	Capacitive load	DC driving capability
System clock	>20MHz	10 … 50 pF	n/a
High-speed data line	5 … 20 MHz	10 … 50 pF	n/a
Low-speed data line	0.5 … 5 MHz	10 … 50 pF	n/a
Low-speed control line	<1 MHz	<20 pF	n/a
High-current control line	n/a	n/a	10 … 30 mA
Medium-current control line	n/a	n/a	1 … 10 mA
Low-current control line	n/a	n/a	<1 mA

Table 6: Signal categories

The following settings for pad output drivers are available, see also Table 7:

- extra-strong driver / no edge configuration available
- strong driver / sharp edge
- strong driver / medium edge
- strong driver / soft edge
- medium driver / no edge configuration available
- weak driver / no edge configuration available

Driver configuration	Edge configuration	Signal category	Capacitive Load	DC Current [1)]
EXTRA-STRONG	none	System clock >40MHz	High	n/a
STRONG	SHARP	System clock >20MHz	Medium	2.5 / 10 mA
STRONG	MEDIUM	System clock High-speed data lines	Low High	2.5 / 10 mA
STRONG	SOFT	High-speed data lines High-current control lines	Low All	2.5 / 10 mA
MEDIUM	none	Low-speed data lines Medium-current control lines	All All	1.0 / 4.0 mA
WEAK	none	Very low-speed control lines Low-current control line	All All	0.1 / 0.5 mA

Table 7: Recommended Output Driver Settings

Note 1) in Table 7: Two values are given for the DC current of GPIO pins in the format "nominal / max mA". The "max mA" value can only be drawn from a pin if maximal 2 other pins in the same 16-bit port group are also driving this maximum current. This restriction is due to danger of electromigration damage.

The following parameters determine the final selection of driver settings:

- signal performance category (AC and DC)
- maximal temperature
- maximal acceptable electromagnetic emission

6.2 Decision Tables and Graphs

Following the recommendations given above, the driver setting selection should be based on (1) proper signal integrity and (2) minimal electromagnetic emission. Since electromagnetic emission increases with stronger driver settings, the weakest driver and slew rate settings should be selected that are able to force the rise/fall times required for the desired signal integrity.

This chapter offers decision numbers in table and graphical format for proper driver settings at maximum clock or data rates expected to be driven. The rise/fall times occupy 1/6th of the clock period each, see Fig. 34 on top. Alternatively, the rise/fall times occupy 1/4th of the clock period each, see Fig. 34 on bottom.

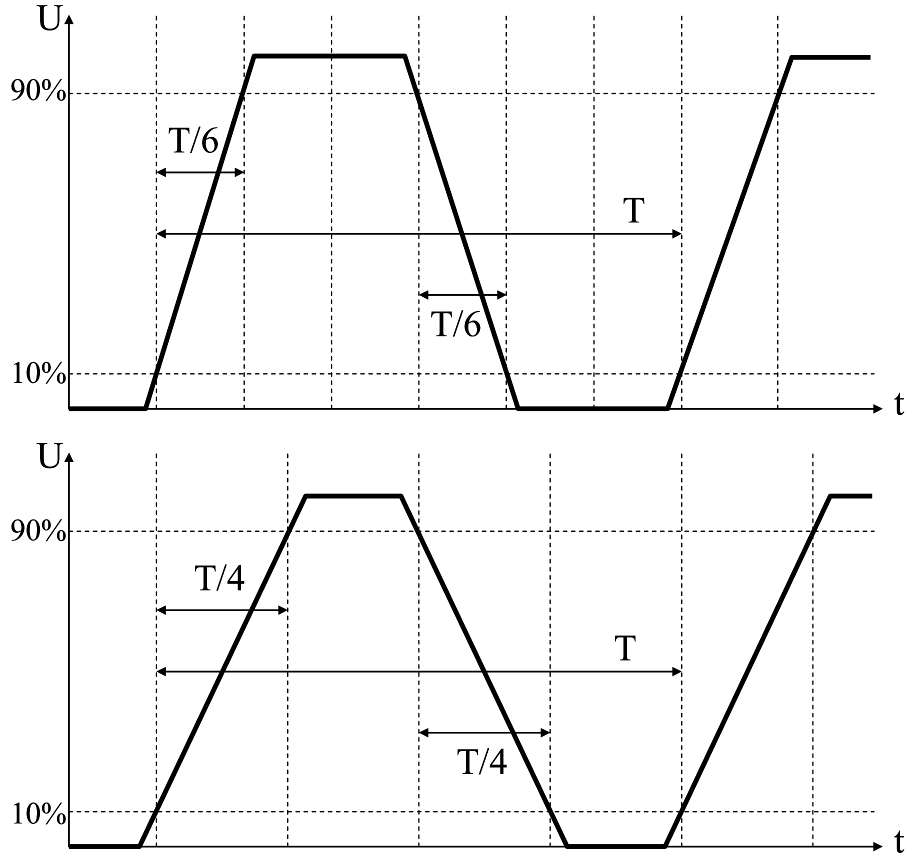

Figure 34: Assumed rise/fall timing conditions related to signal period

Please note that all values given in this chapter are proposals for system application designers using Infineon XC2200 microcontrollers in 0.13µm CMOS technology. They are based on timing measurements performed on center lot devices. Thus all values are subject to less than 10% offset depending according fabrication process variation. Additionally, pad supply voltages different from nominal conditions impact the resulting timing. The finally selected driver setting should consider these facts.

Fig. 35 shows an example of a decision graph.

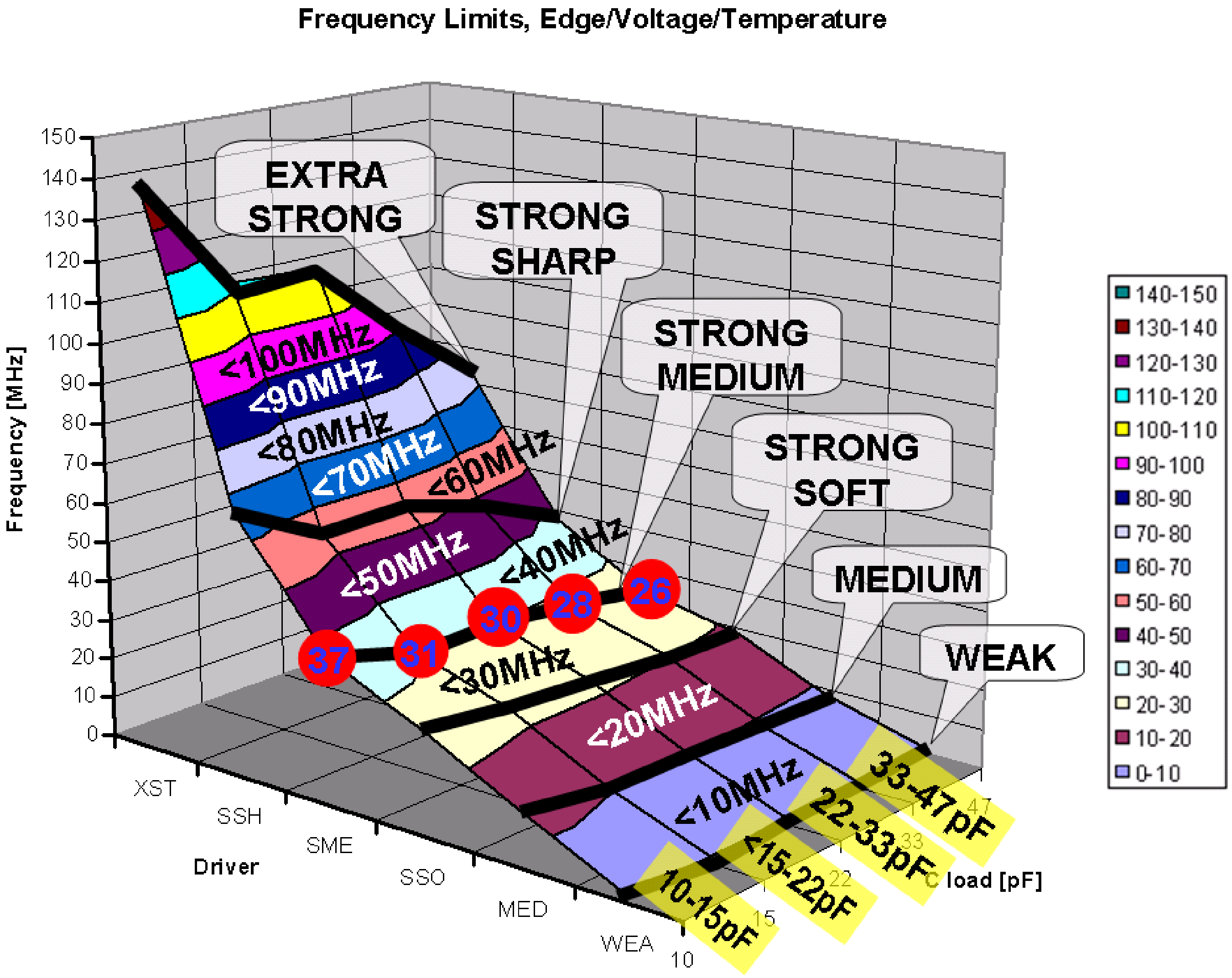

Figure 35: Assumed rise/fall timing conditions related to signal period

The title of each diagram indicates the conditions (Edge/Voltage/Temperature) for the shown values:

Edge is either “T/4” (meaning the rise time and the fall time take each 1/4 of the data rate period) or “T/6” (meaning the rise time and the fall time take each 1/6 of the data rate period).

Voltage indicates the I/O pad supply voltage VDDP0 and is either “3.3V” or “5.0V”.

Temperature indicates the ambient temperature and is either “125°C”, “110°C”, “85°C”, “70°C”, “25°C” or “-40°C”.

The maximal clock/data rate to meet good signal integrity is given in [MHz] for capacitive loads of 10, 15, 22, 33, 47 pF and driver selections of weak, medium, strong soft/medium/sharp/extra-strong. In Fig. 35, the resulting maximum data rates for the strong-medium driver are marked with red circles:

If the strong-medium driver is loaded with 10pF (which means actually 13pF including the oscilloscope probe load) it is capable to drive a clean 37MHz signal (under the above mentioned edge/voltage/temperature conditions).

An 18pF load (15+3pF) can be driven at 31MHz.

A 25pF load (22+3pF) can be driven at 30MHz.

A 36pF load (33+3pF) can be driven at 28MHz.

A 50pF load (47+3pF) can be driven at 26MHz.

Other examples from Fig. 35:

A 20MHz signal can be driven up to ca. 30pF load by a strong-soft driver. At 50pF, a strong-medium driver is required. Of course a strong-medium or even a stronger driver can be selected for 20MHz at 20pF, but this causes unnecessarily high electromagnetic emission and should be avoided.

General rule: Select always the weakest possible driver which is able to toggle the maximal desired data rate at the given external load, supply voltage and temperature.

The capability of the weak driver stays below 1MHz for all loads. Exact values are not resolved sufficiently in the diagrams; the exact values must be taken from Tables 8 and 9, as described below.

The rise/fall times occupy 1/6th of the clock period each, see Fig. 34 on top. This relation should be acceptable for most interface signals and protocols.

Tables 8 and 9 give an overview of the maximal toggle rates in [MHz] for all driver settings (WEA = weak, MED = medium, SSO = strong-soft, SME = strong-medium, SSH =strong-sharp, XST = extra-strong) connected to capacitive loads of 10, 15, 22, 33, and 47 pF. Each ambient temperature is marked by its own color. According to the microcontroller specification or marking, one of the following maximum temperatures should apply: 125°C, 110°C, 85°C, 70°C. The other temperatures, 25°C and -40°C, are given for reference only.

In Table 8, the rise/fall times are assumed to occupy 1/6th of the clock period, see Fig. 34 on top. In Table 9, the rise/fall times are assumed to occupy 1/4th of the clock period, see Fig. 34 on bottom.

Fig. 36-59 show the values of Tables 9 and 10 in the graphical representation explained in Fig. 35, separated by ambient temperatures and driver types. In the respective titles, “16% Edges” stands for rise/fall times occupying 1/6th of the clock period; “25% Edges” stands for rise/fall times occupying 1/4th of the clock period.

If other than 1/4 or 1/6 rise/fall times are intended, the values of either Table 9 or Table 10 must be taken and extrapolated. Example: Rise and fall time should be each 1/10 of the data rate. We are interested in a data rate of 10MHz at 15pF with VDDP0=3.3V, T_A=85°C. Fetch the values from Table 8 and multiply them by 6/10=0.6 or fetch the values from Table 9 and multiply them by 4/10=0.4. The resulting values for 1/10 edge are shown in Table 8.

DRIVER	1/4 EDGE	1/6 EDGE	1/10 EDGE
XST	58,71	39,14	23,484
SSH	32,44	21,23	12,976
SME	16,73	11,15	6,692
SSO	12,48	8,32	4,992
MED	6,59	4,4	2,636
WEA	0,681	0,454	0,2724

Table 8: Calculated max. data rate [MHz] for 1/10 edges

	3,3V						5V					
125°C		10	15	22	33	47		10	15	22	33	47
	XST	46,04	37,45	34,22	28,3	23,47	XST	92,59	67,75	56,31	45,17	37,97
	SSH	26,88	20,68	17,98	15,43	13,35	SSH	37,29	31,87	28,11	22,58	19,33
	SME	12,25	10,26	9,16	8,68	8,15	SME	19	16,52	14,88	13,13	12,72
	SSO	8,95	7,72	6,9	6,21	6,54	SSO	13,98	11,99	11,18	10,04	9,8
	MED	4,87	4,13	3,69	3,38	3,08	MED	7,16	6	5,38	4,74	4,4
	WEA	0,5	0,424	0,392	0,381	0,385	WEA	0,86	0,777	0,745	0,686	0,677
110°C		10	15	22	33	47		10	15	22	33	47
	XST	50,29	38,08	35,08	29,2	24,26	XST	92,83	68,8	58,97	47,45	39,56
	SSH	27,37	21,03	18,78	16,01	13,75	SSH	38,25	32,49	29,32	23,89	20,23
	SME	12,51	10,6	9,56	9,18	8,43	SME	19,8	17,11	15,67	13,9	13,23
	SSO	9,17	7,95	7,2	6,55	6,75	SSO	14,45	12,46	11,71	10,59	10,22
	MED	4,99	4,23	3,84	3,52	3,2	MED	7,41	6,15	5,64	4,96	4,55
	WEA	0,462	0,435	0,405	0,364	0,399	WEA	0,893	0,803	0,778	0,786	0,698
85°C		10	15	22	33	47		10	15	22	33	47
	XST	57,38	39,14	36,52	30,7	25,58	XST	93,22	70,55	63,41	51,25	42,22
	SSH	28,18	21,23	20,11	16,97	14,4	SSH	39,87	33,52	31,36	26,06	21,73
	SME	12,94	11,15	10,23	10	8,9	SME	21,13	18,09	16,98	15,17	14,07
	SSO	9,54	8,32	7,7	7,11	7,1	SSO	15,24	13,25	12,6	11,51	10,91
	MED	5,2	4,4	4,09	3,74	3,41	MED	7,84	6,41	6,07	5,33	4,8
	WEA	0,483	0,454	0,426	0,335	0,422	WEA	0,947	0,846	0,832	0,953	0,734
70°C		10	15	22	33	47		10	15	22	33	47
	XST	61,64	39,77	37,38	31,59	26,37	XST	93,46	71,59	66,08	53,54	43,81
	SSH	28,67	21,98	20,91	17,54	14,8	SSH	40,84	34,14	32,58	27,36	22,63
	SME	13,19	11,48	10,62	10,5	9,19	SME	21,93	18,68	17,77	15,93	14,58
	SSO	9,76	8,55	7,99	7,45	7,31	SSO	15,71	13,73	13,13	12,06	11,33
	MED	5,33	4,5	4,24	3,88	3,53	MED	8,1	6,56	6,33	5,55	4,96
	WEA	0,496	0,465	0,439	0,428	0,436	WEA	0,979	0,872	0,865	0,803	0,756
25°C		10	15	22	33	47		10	15	22	33	47
	XST	74,4	41,67	39,97	34,29	28,74	XST	94,16	74,74	74,07	60,39	48,59
	SSH	30,14	23,05	23,31	19,27	15,98	SSH	43,74	36	36,23	31,27	25,33
	SME	13,96	12,48	11,82	11,99	10,04	SME	24,33	20,45	20,13	18,21	16,1
	SSO	10,42	9,22	8,89	8,46	7,94	SSO	17,13	15,15	14,72	13,72	12,58
	MED	5,71	4,8	4,69	4,28	3,91	MED	8,87	7,02	7,1	6,22	5,41
	WEA	0,533	0,498	0,478	0,466	0,476	WEA	1,076	0,95	0,962	0,899	0,821
-40°C		10	15	22	33	47		10	15	22	33	47
	XST	82,1	65,88	55,01	43,63	34,29	XST	102,88	82,91	78,62	65,1	51,92
	SSH	35,24	30,92	26,29	22,64	17,94	SSH	47,76	44,33	40,16	34,51	29,55
	SME	16,92	15,95	14,43	13,59	11,9	SME	27,67	24,88	24,12	21,65	18,66
	SSO	12,17	11,1	10,18	10,04	8,74	SSO	19,63	18	17,18	15,89	14,53
	MED	6,56	6,16	5,46	4,89	4,36	MED	9,66	8,63	8,07	7.15	6,11
	WEA	0,598	0,601	0,596	0,574	0,529	WEA	1,211	1,126	1,131	1,11	0,979

Table 9: Maximum toggle rates [MHz] for all driver settings at loads 10..47 pF; 16% Edges

	3,3V						5V					
125°C		10	15	22	33	47		10	15	22	33	47
	XST	69,06	56,18	51,33	52,44	35,21	XST	138,89	101,61	84,46	67,75	56,95
	SSH	40,32	31,02	26,07	23,15	20,03	SSH	55,93	47,8	42,16	33,88	29
	SME	18,28	15,39	13,74	13,02	12,22	SME	28,51	24,78	22,32	19,7	19,08
	SSO	13,43	11,58	10,35	9,31	9,81	SSO	20,97	17,99	16,77	15,06	14,71
	MED	7,3	6,19	5,54	5,08	4,62	MED	10,73	8,99	8,06	7,1	6,6
	WEA	0,675	0,636	0,587	0,572	0,578	WEA	1,291	1,165	1,118	1,028	1,015
110°C		10	15	22	33	47		10	15	22	33	47
	XST	75,44	57,13	52,63	43,79	36,4	XST	139,24	103,2	88,46	71,18	59,34
	SSH	41,06	31,55	28,17	24,01	20,62	SSH	57,48	48,73	43,99	35,83	30,35
	SME	18,77	15,89	14,34	13,77	12,65	SME	29,7	25,66	23,5	20,84	19,84
	SSO	13,76	11,92	10,8	9,82	10,12	SSO	21,68	18,7	17,56	15,89	15,33
	MED	7,49	6,34	5,76	5,28	4,81	MED	11,12	9,22	8,45	7,44	6,83
	WEA	0,694	0,653	0,607	0,546	0,599	WEA	1,339	1,204	1,167	1,191	1,048
85°C		10	15	22	33	47		10	15	22	33	47
	XST	86,08	58,71	54,78	46,04	38,37	XST	139,83	105,82	95,12	76,88	63,32
	SSH	42,28	32,44	30,17	25,45	21,61	SSH	59,8	50,28	47,03	39,09	32,6
	SME	19,4	16,73	15,34	15,01	13,36	SME	31,7	27,14	25,47	22,75	21,11
	SSO	14,31	12,48	11,54	10,66	10,65	SSO	22,86	19,88	18,89	17,27	16,37
	MED	7,81	6,59	6,14	5,61	5,11	MED	11,76	9,61	9,1	7,99	7,21
	WEA	0,725	0,681	0,64	0,503	0,633	WEA	1,42	1,269	1,248	1,462	1,102
70°C		10	15	22	33	47		10	15	22	33	47
	XST	92,46	59,66	56,07	47,39	39,55	XST	140,18	107,39	99,12	80,31	65,71
	SSH	43,01	32,98	31,37	26,31	22,2	SSH	61,26	51,21	48,86	41,04	33,95
	SME	19,79	17,23	15,94	15,75	13,78	SME	32,9	28,02	26,65	23,89	21,87
	SSO	14,64	12,82	11,99	11,17	10,96	SSO	23,57	20,59	19,69	18,09	17
	MED	7,99	6,75	6,36	5,81	5,3	MED	12,14	9,84	9,49	8,33	7,43
	WEA	0,744	0,697	0,659	0,642	0,653	WEA	1,468	1,308	1,297	1,204	1,134
25°C		10	15	22	33	47		10	15	22	33	47
	XST	111,61	62,5	59,95	51,44	43,1	XST	141,24	112,11	111,11	90,58	72,89
	SSH	45,21	34,58	34,97	28,9	23,97	SSH	65,62	54	54,35	46,9	37,99
	SME	20,94	18,73	17,73	17,99	15,06	SME	36,5	30,67	30,19	27,32	24,15
	SSO	15,63	13,83	13,33	12,69	11,9	SSO	25,63	22,73	22,08	20,58	18,87
	MED	8,56	7,2	7,04	6,42	5,86	MED	13,3	10,54	10,65	9,33	8,12
	WEA	0,8	0,747	0,718	0,699	0,715	WEA	1,614	1,425	1,443	1,348	1,231
-40°C		10	15	22	33	47		10	15	22	33	47
	XST	123,15	98,81	82,51	65,45	51,44	XST	154,32	128,87	117,92	97,66	77,88
	SSH	52,85	46,38	39,43	33,97	26,19	SSH	71,63	66,49	60,24	51,76	44,33
	SME	25,38	23,92	21,64	20,39	17,86	SME	41,05	37,31	36,18	32,47	28
	SSO	18,25	16,64	15,26	15,06	13,12	SSO	29,45	27	25,77	23,83	21,8
	MED	9,84	9,24	8,18	7,34	6,54	MED	14,49	12,94	12,1	10,73	9,16
	WEA	0,897	0,903	0,894	0,862	0,794	WEA	1,867	1,689	1,656	1,666	1,469

Table 10: Maximum toggle rates [MHz] for all driver settings at loads 10..47pF; 25% edges

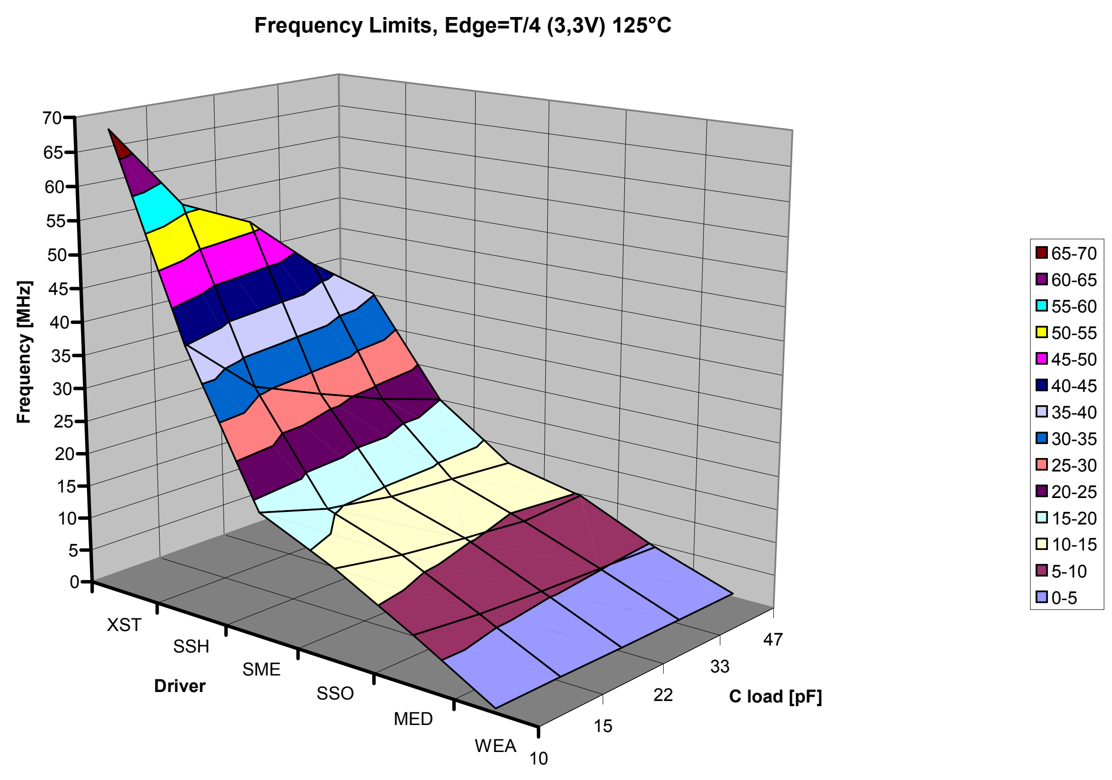

Figure 36: Selection decision graph for driver at T_A=125°C; 3.3V; edges occupy 1/4 period

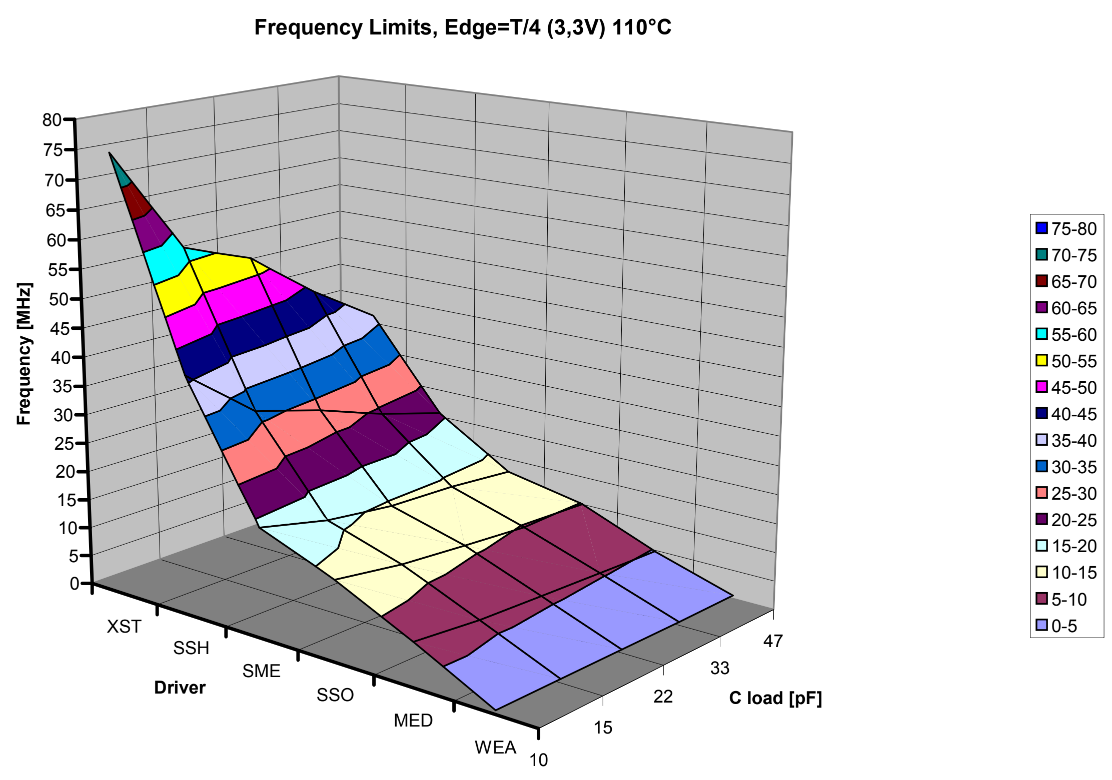

Figure 37: Selection decision graph for driver at T_A=110°C; 3.3V; edges occupy 1/4 period

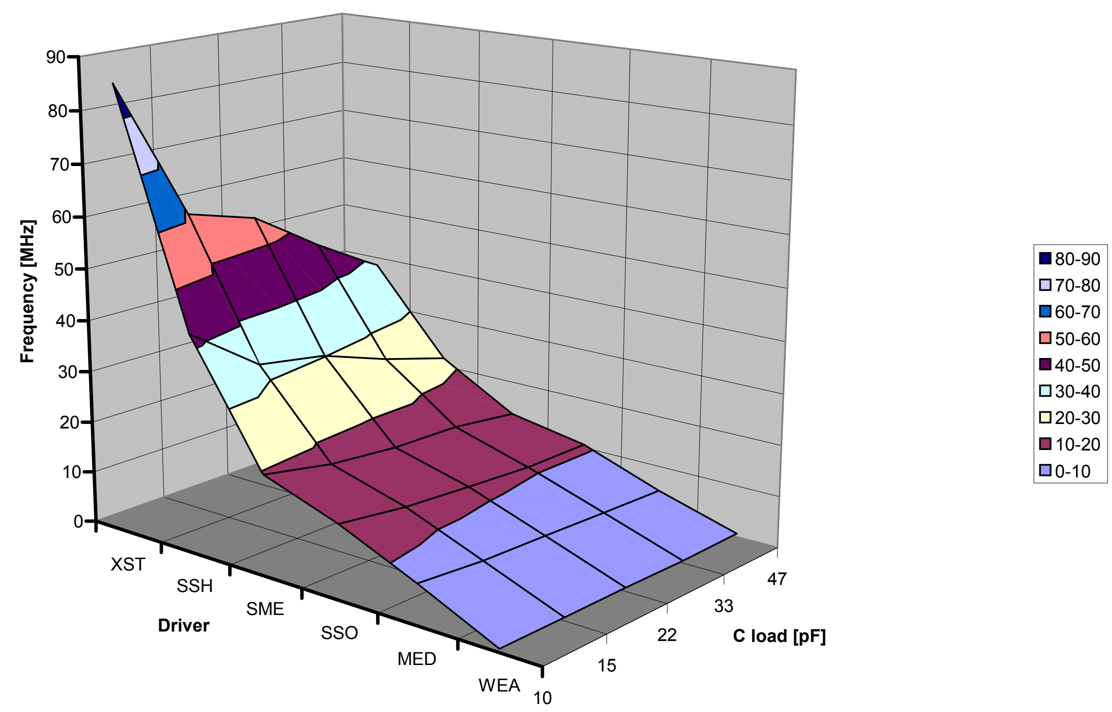

Figure 38: Selection decision graph for driver at T_A=85°C; 3.3V; edges occupy 1/4 period

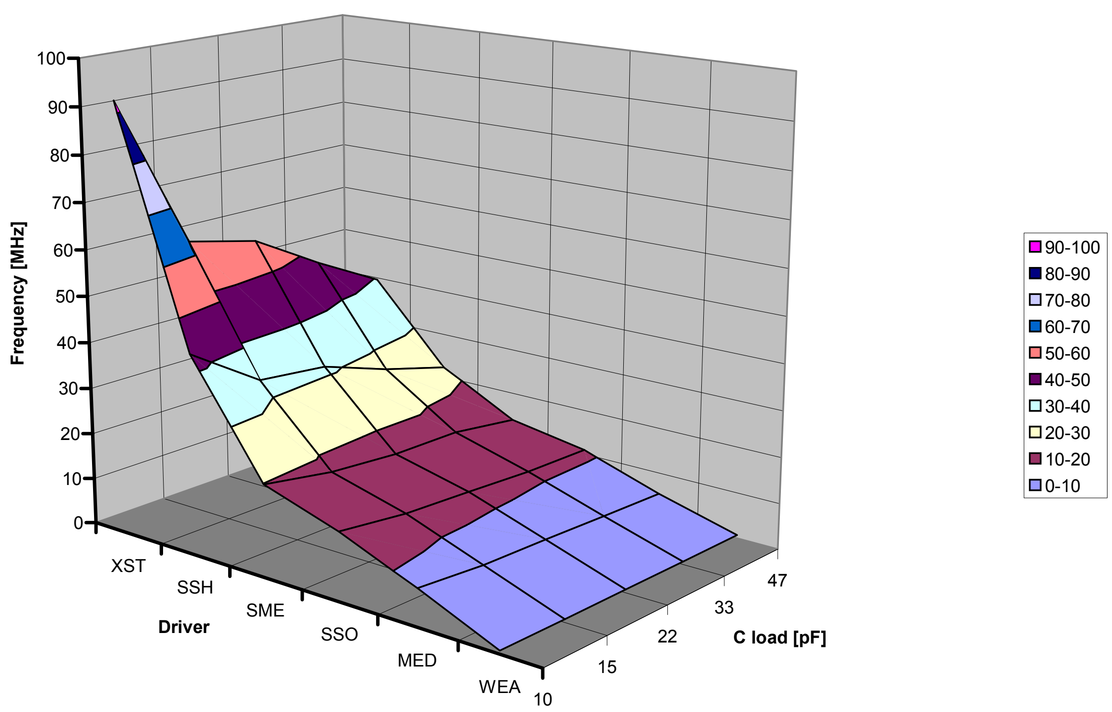

Figure 39: Selection decision graph for driver at T_A=70°C; 3.3V; edges occupy 1/4 period

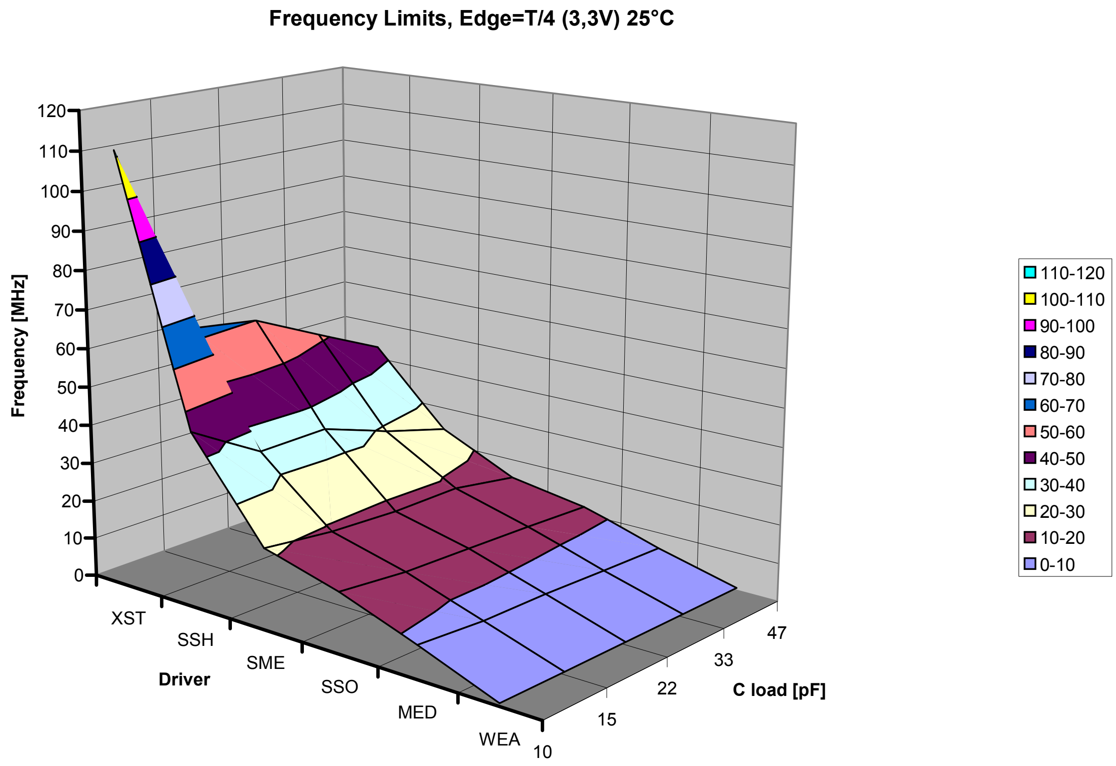

Figure 40: Selection decision graph for driver at T_A=25°C; 3.3V; edges occupy 1/4 period

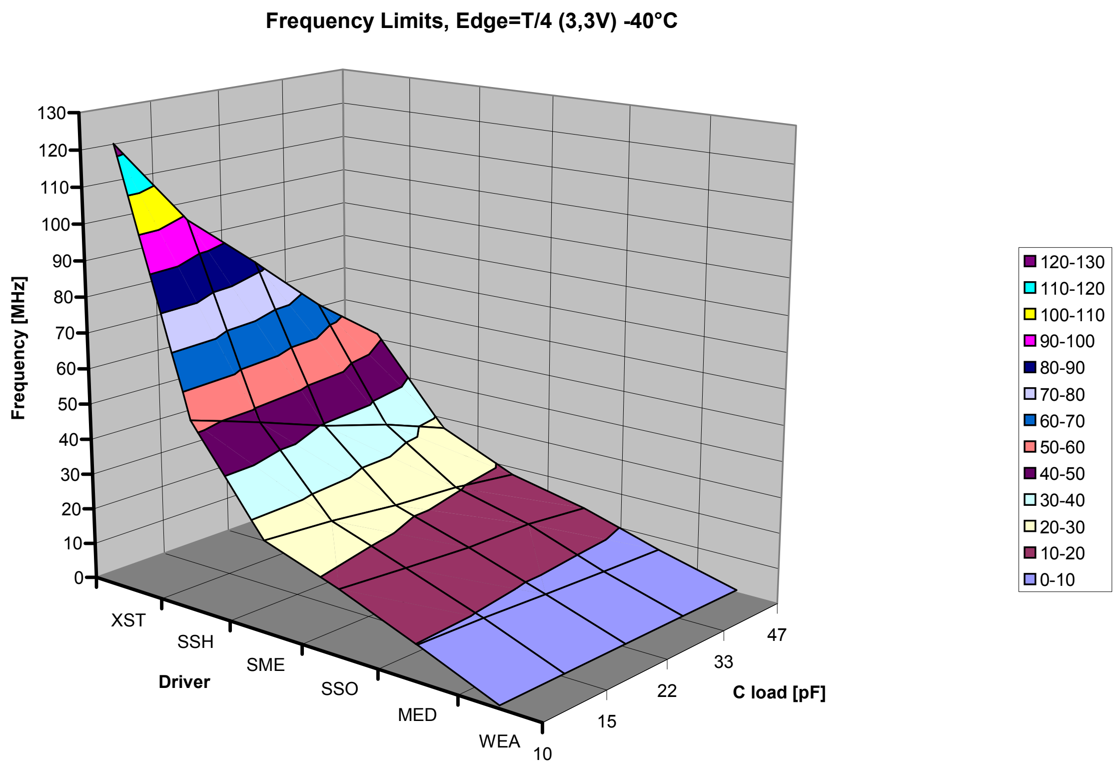

Figure 41: Selection decision graph for driver at T_A=-40°C; 3.3V; edges occupy 1/4 period

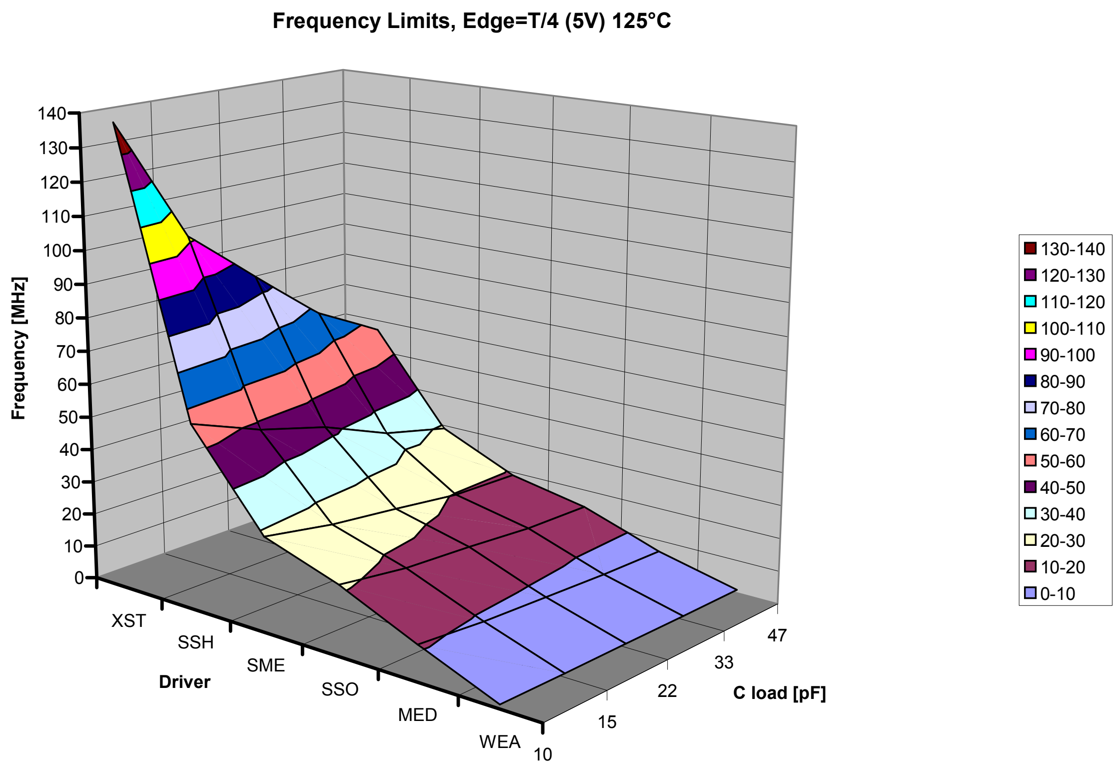

Figure 42: Selection decision graph for driver at T_A=125°C; 5.0V; edges occupy 1/4 period

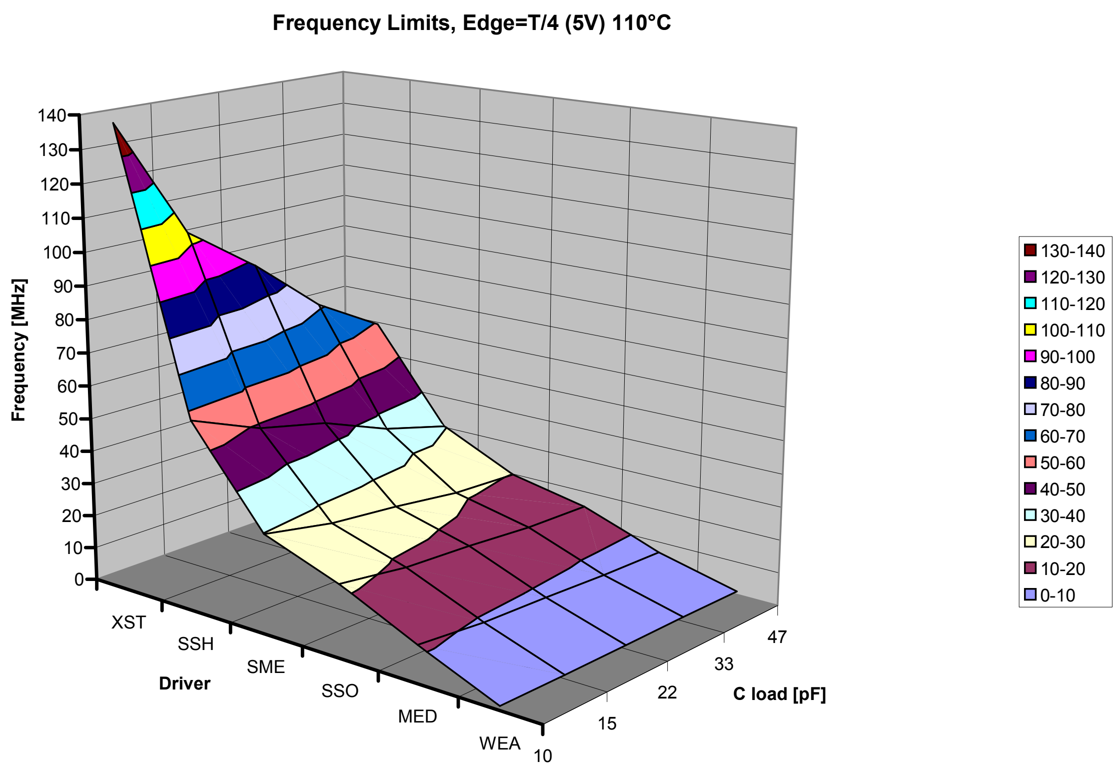

Figure 43: Selection decision graph for driver at T_A=110°C; 5.0V; edges occupy 1/4 period

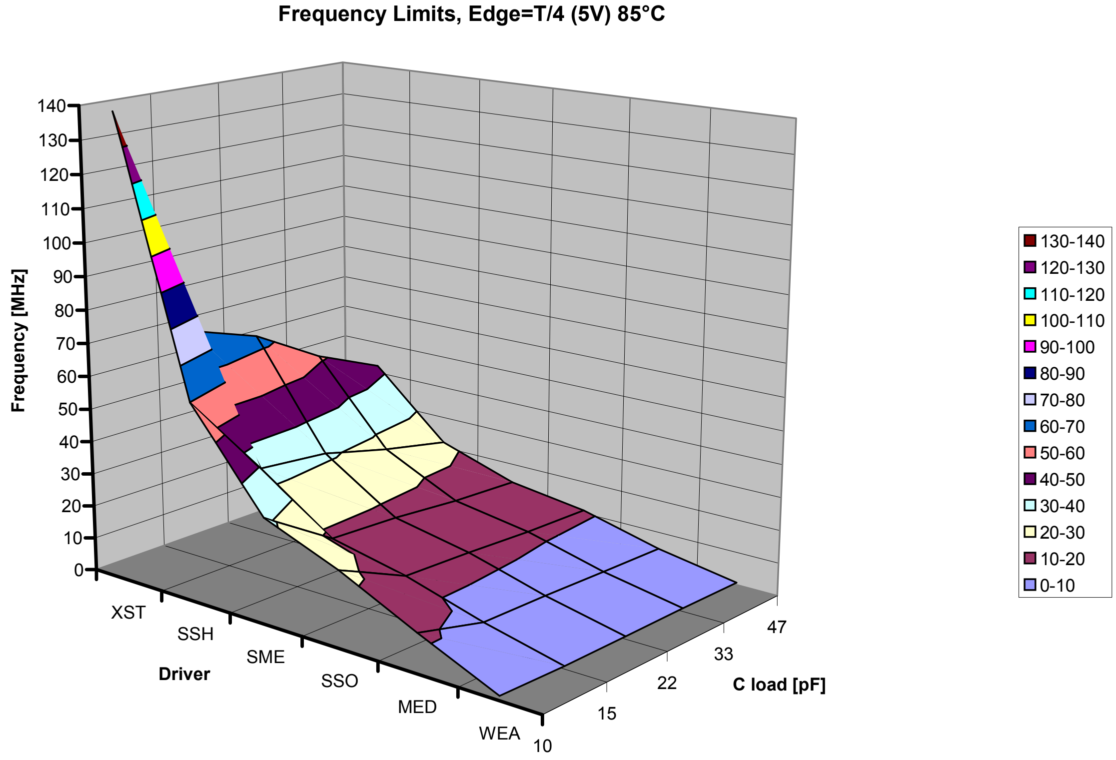

Figure 44: Selection decision graph for driver at T_A=85°C; 5.0V; edges occupy 1/4 period

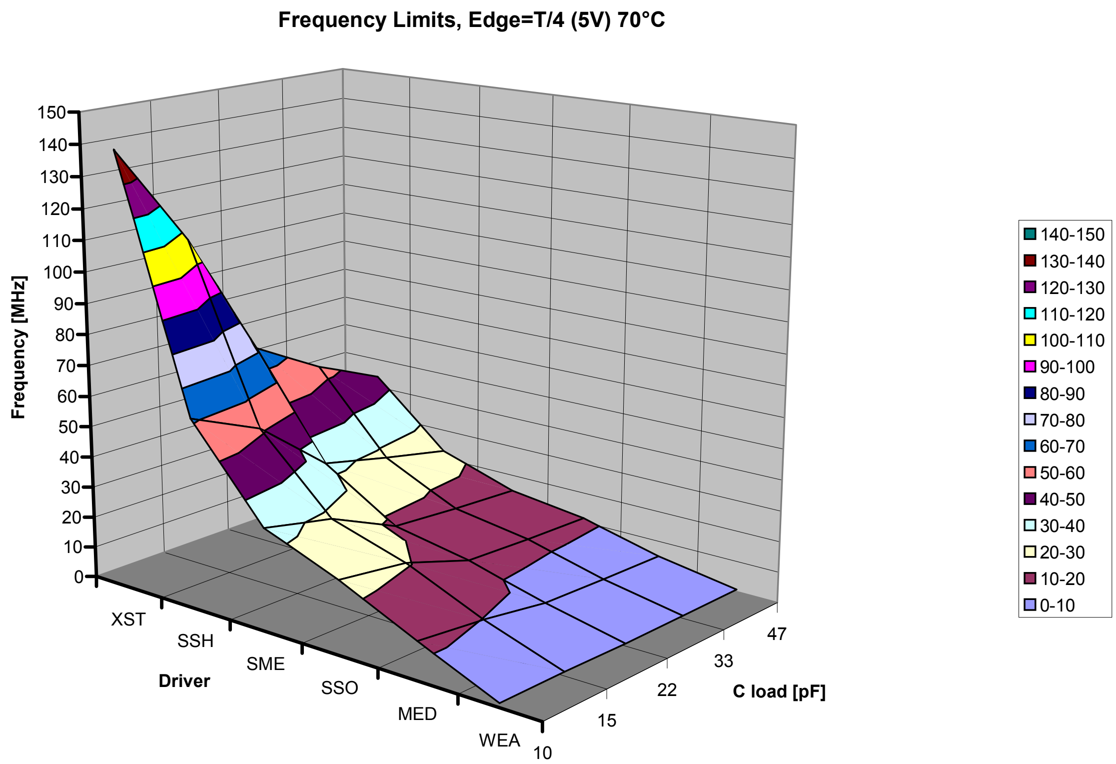

Figure 45: Selection decision graph for driver at T_A=70°C; 5.0V; edges occupy 1/4 period

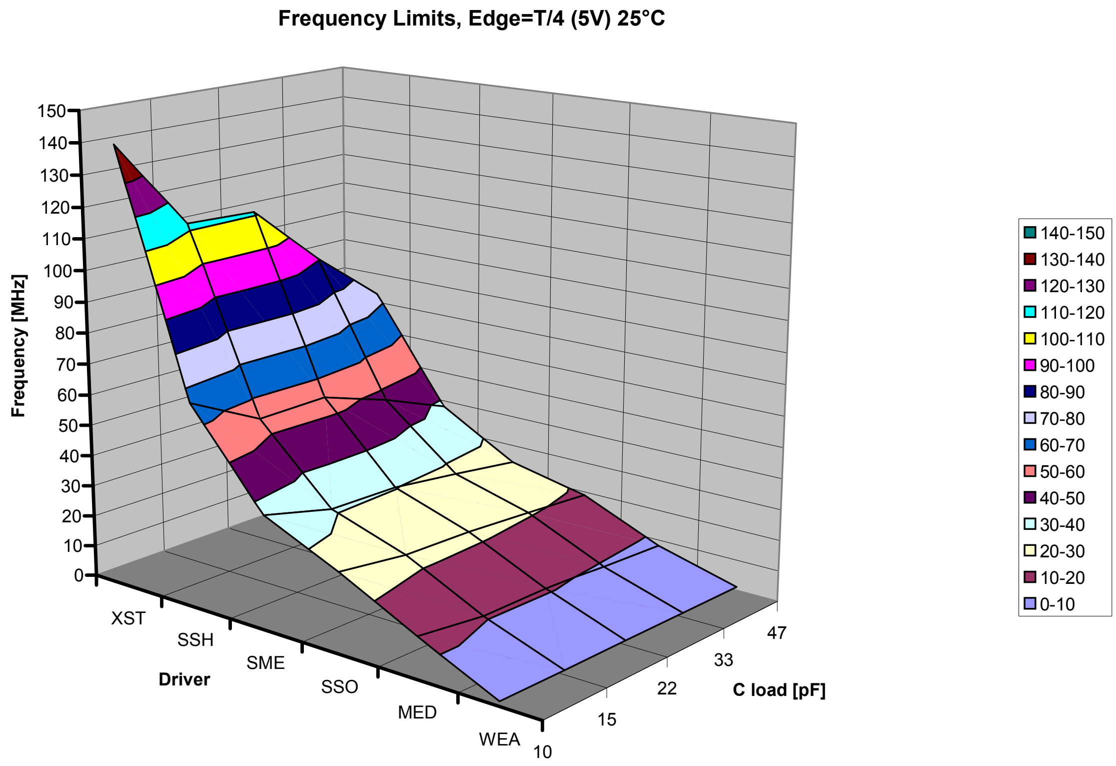

Figure 46: Selection decision graph for driver at T_A=25°C; 5.0V; edges occupy 1/4 period

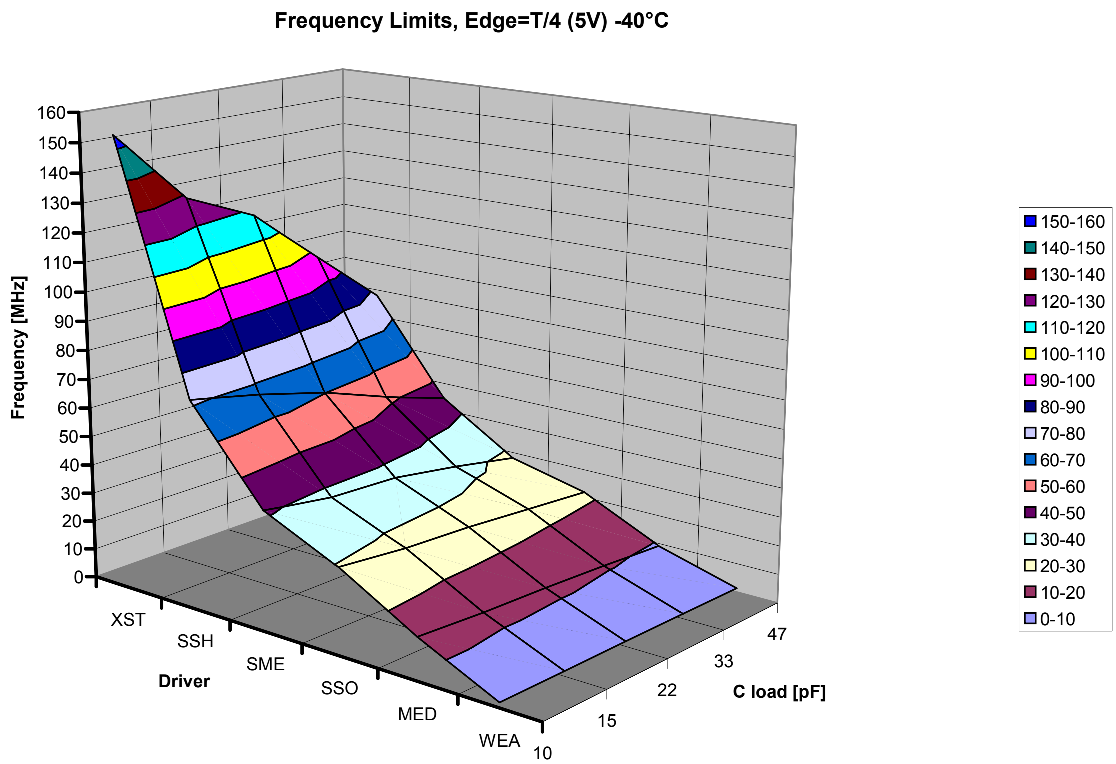

Figure 47: Selection decision graph for driver at T_A=-40°C; 5.0V; edges occupy 1/4 period

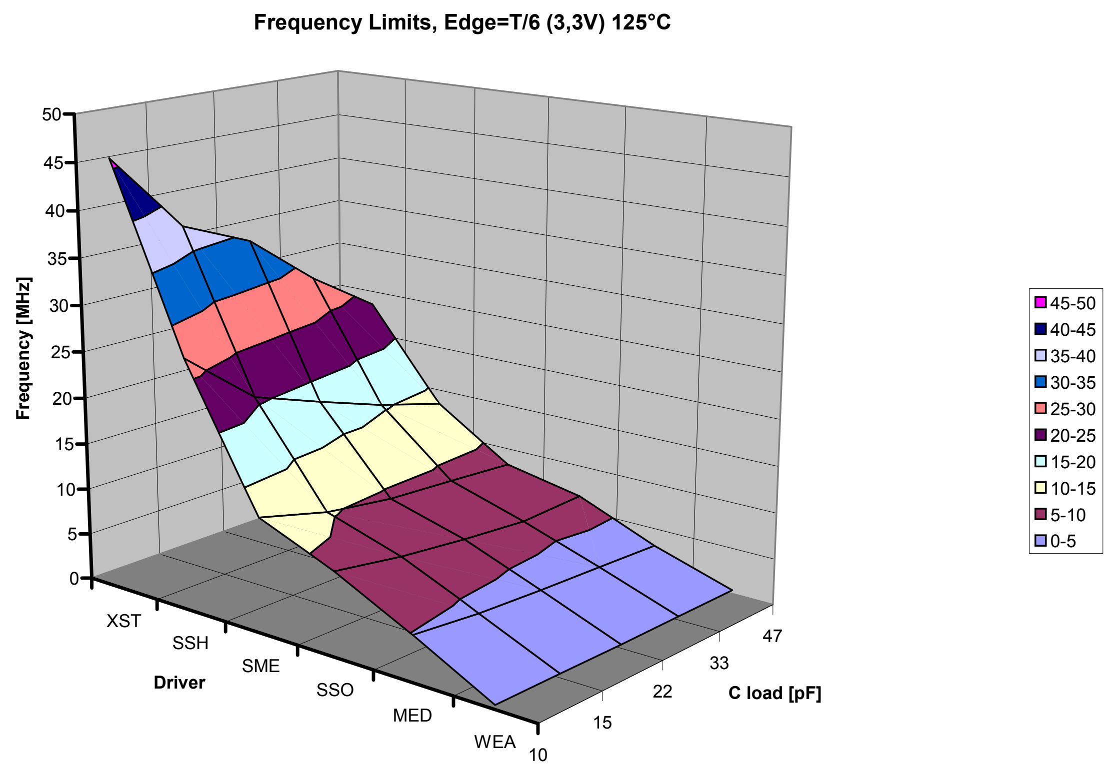

Figure 48: Selection decision graph for driver at T_A=125°C; 3.3V; edges occupy 1/6 period

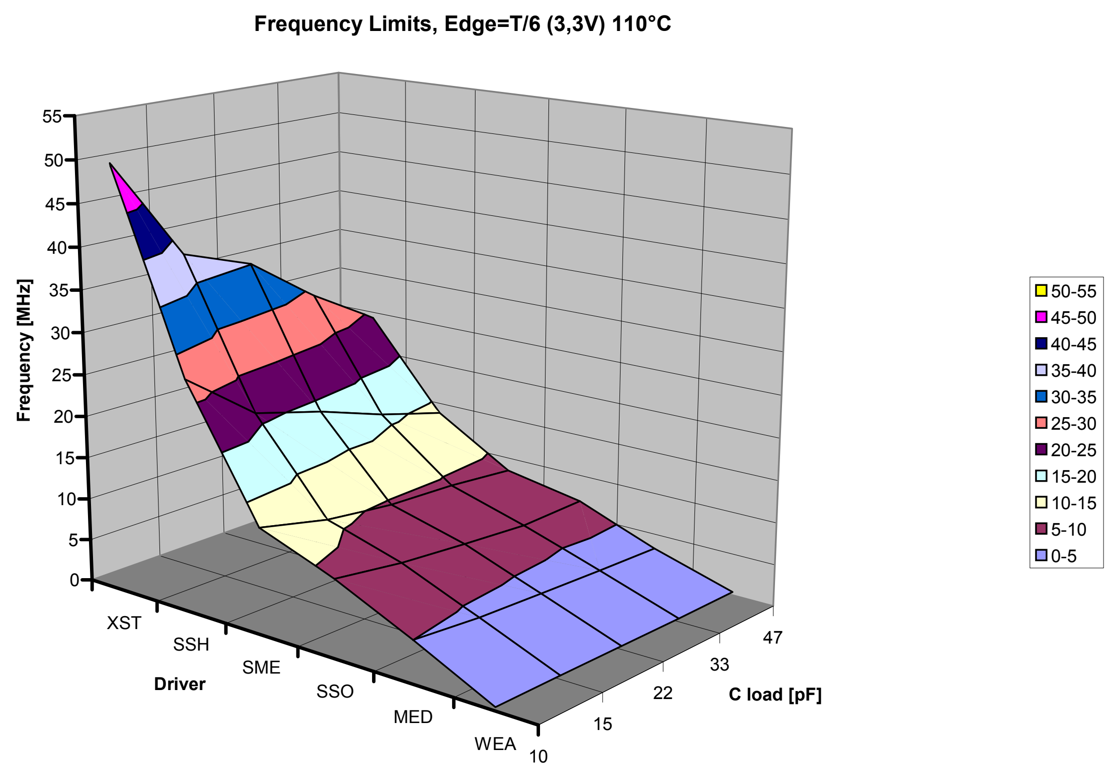

Figure 49: Selection decision graph for driver at T_A=110°C; 3.3V; edges occupy 1/6 period

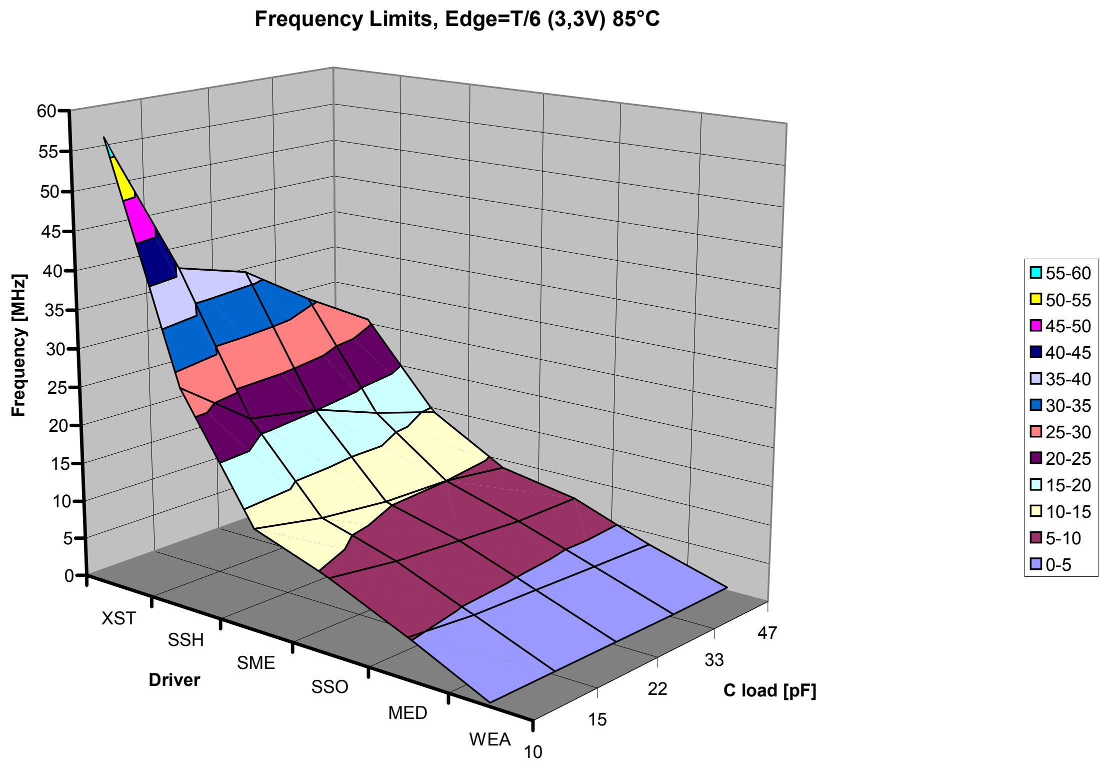

Figure 50: Selection decision graph for driver at T_A=85°C; 3.3V; edges occupy 1/6 period

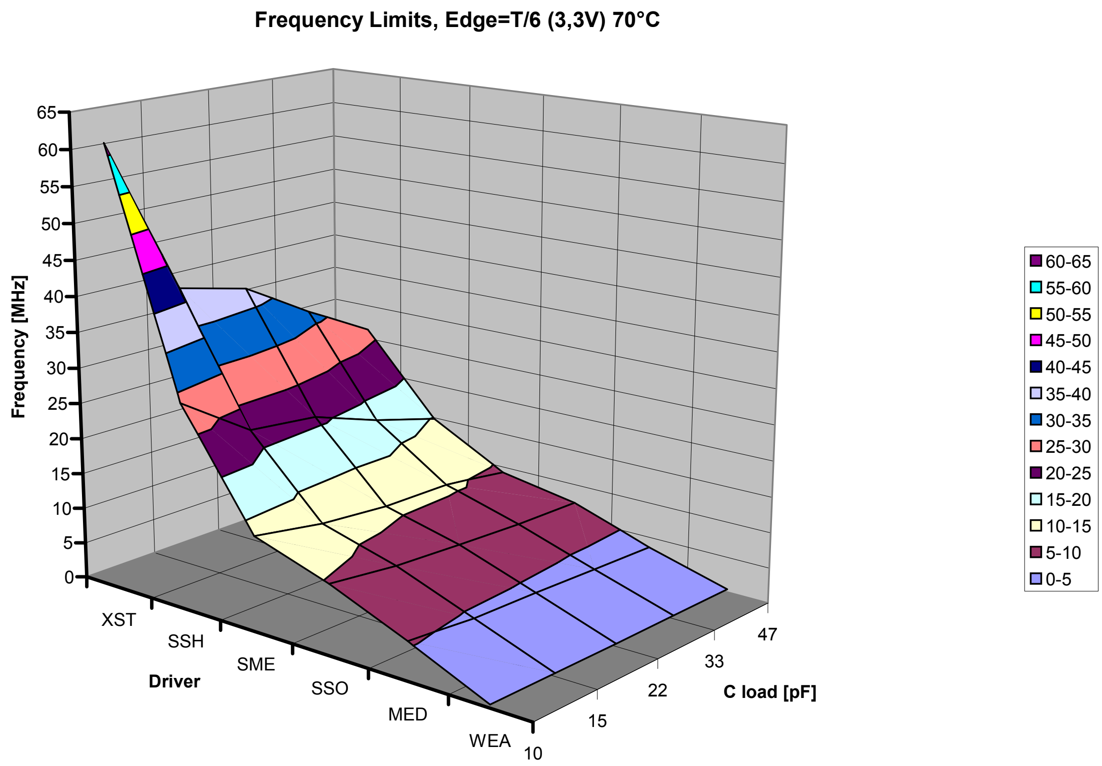

Figure 51: Selection decision graph for driver at T_A=70°C; 3.3V; edges occupy 1/6 period

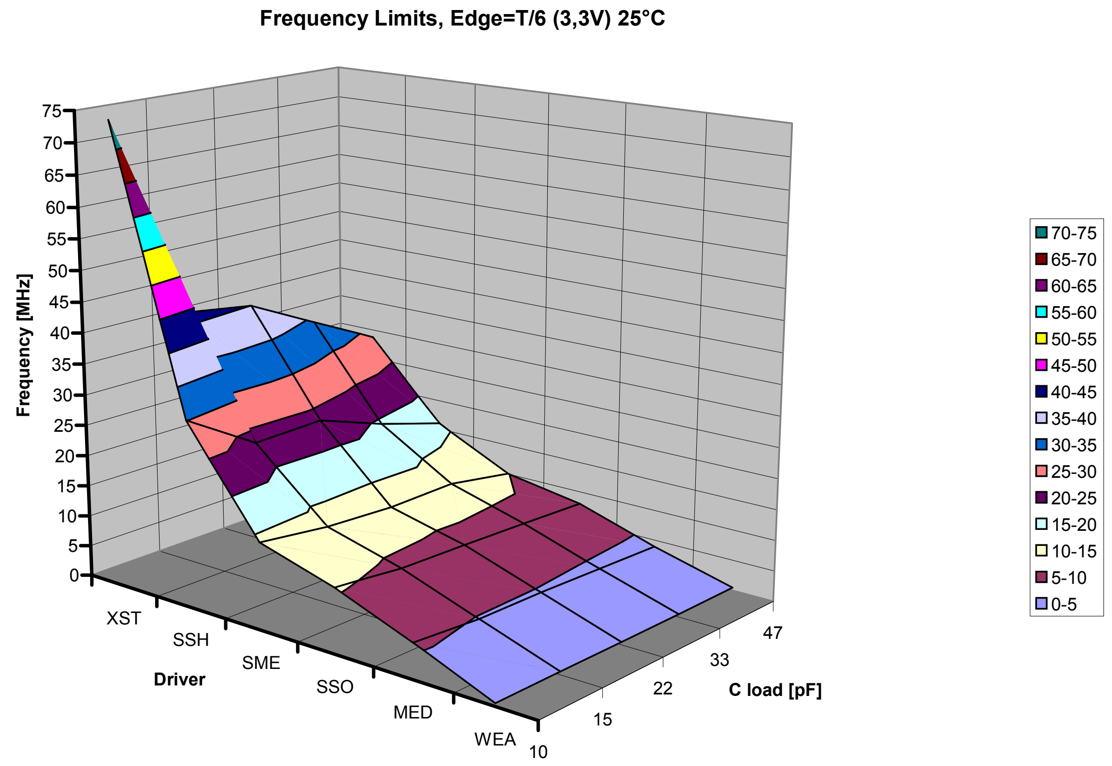

Figure 52: Selection decision graph for driver at T_A=25°C; 3.3V; edges occupy 1/6 period

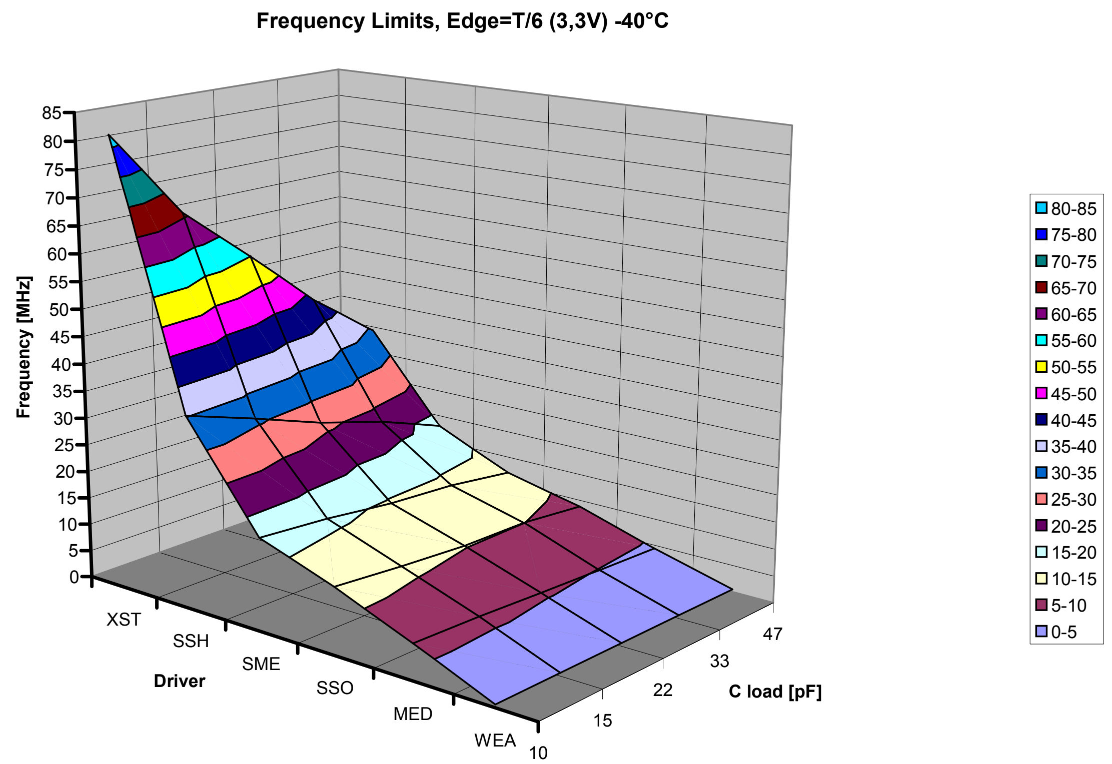

Figure 53: Selection decision graph for driver at T_A=-40°C; 3.3V; edges occupy 1/6 period

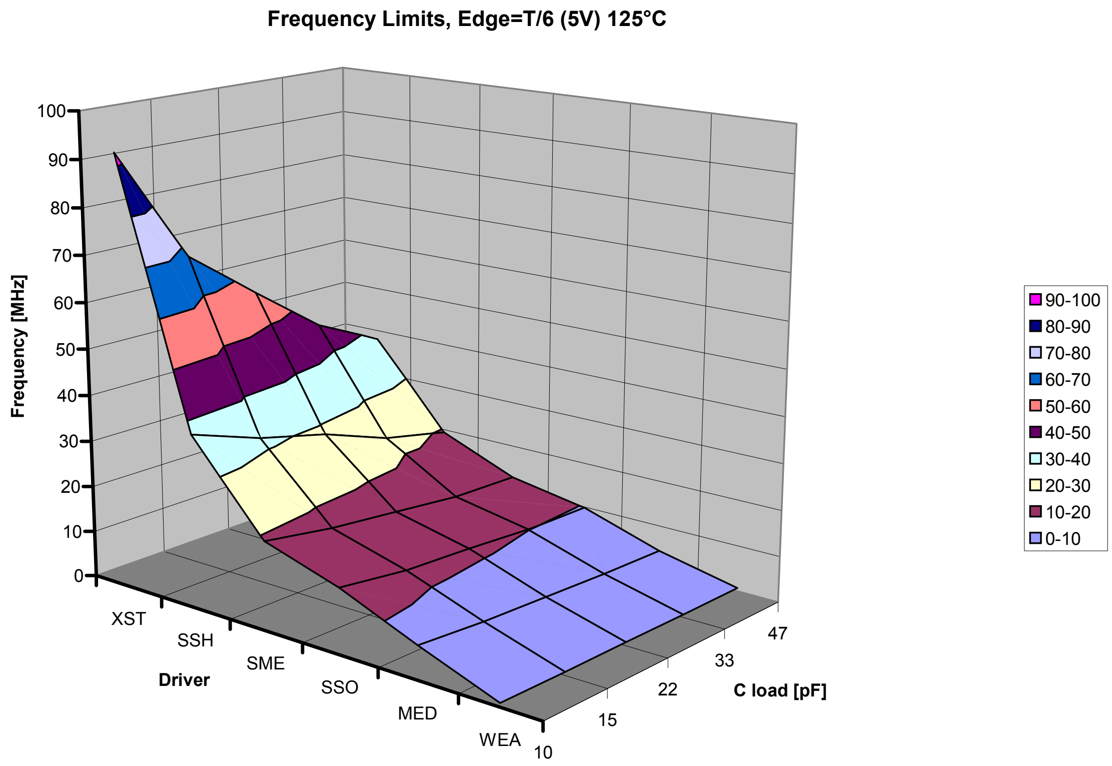

Figure 54: Selection decision graph for driver at T_A=125°C; 5.0V; edges occupy 1/6 period

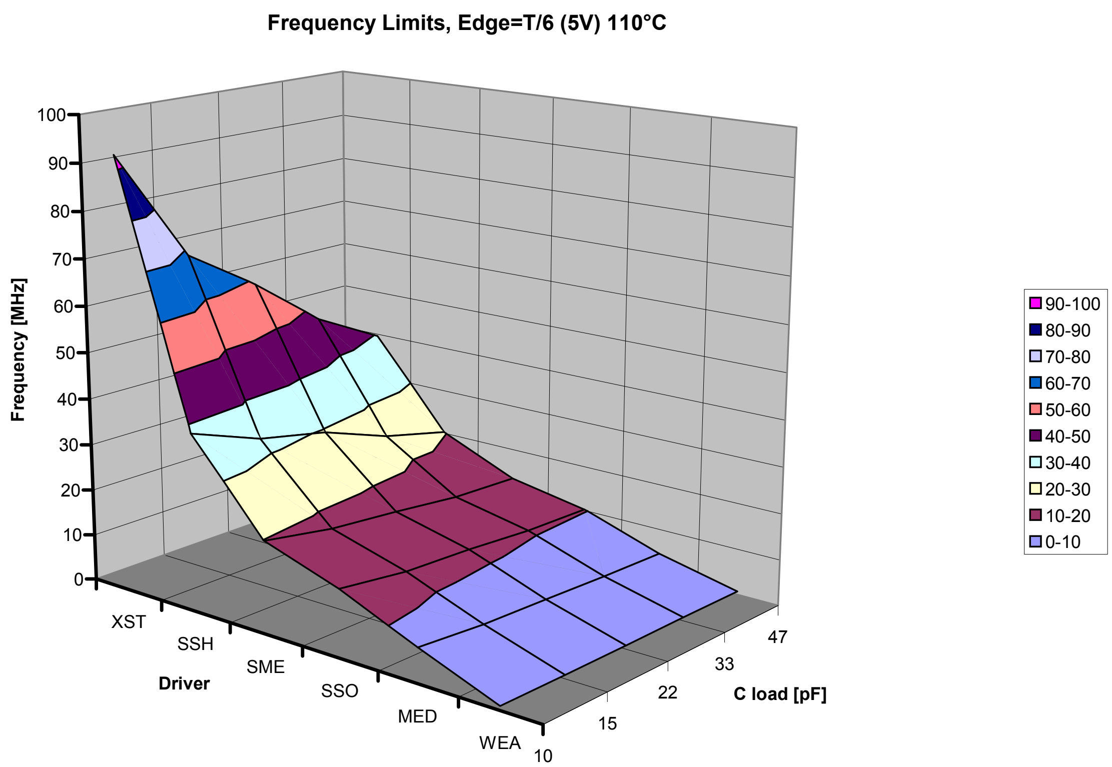

Figure 55: Selection decision graph for driver at T_A=110°C; 5.0V; edges occupy 1/6 period

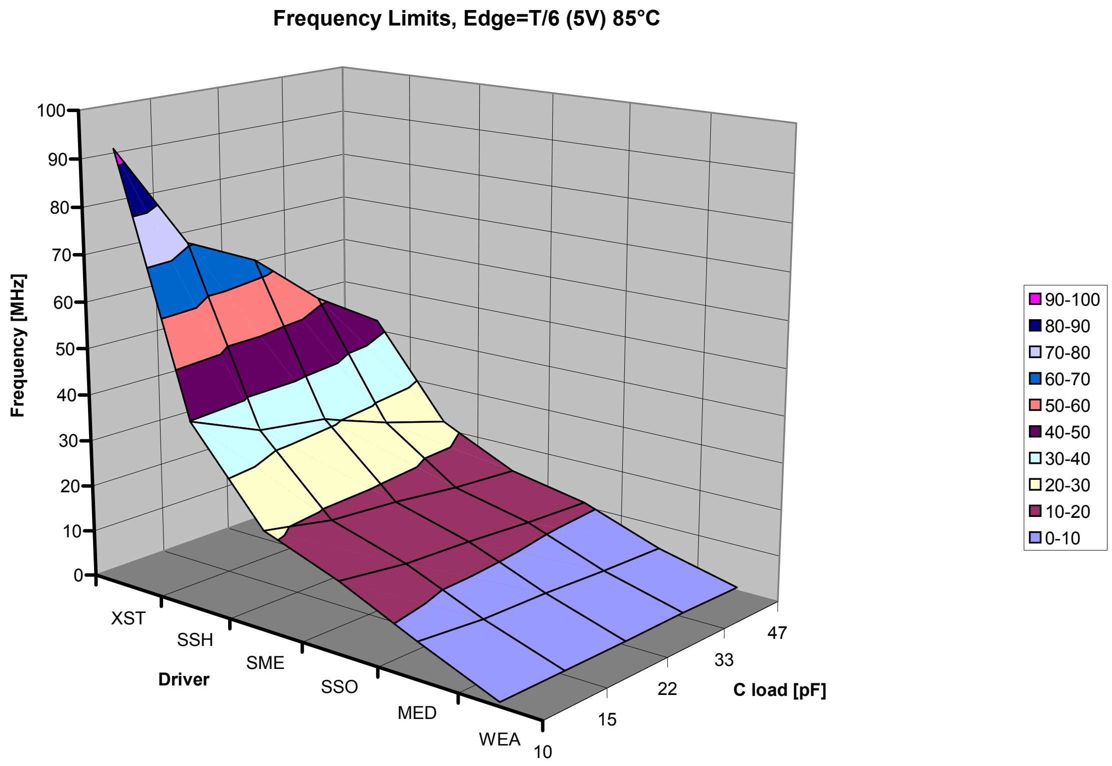

Figure 56: Selection decision graph for driver at T_A=85°C; 5.0V; edges occupy 1/6 period

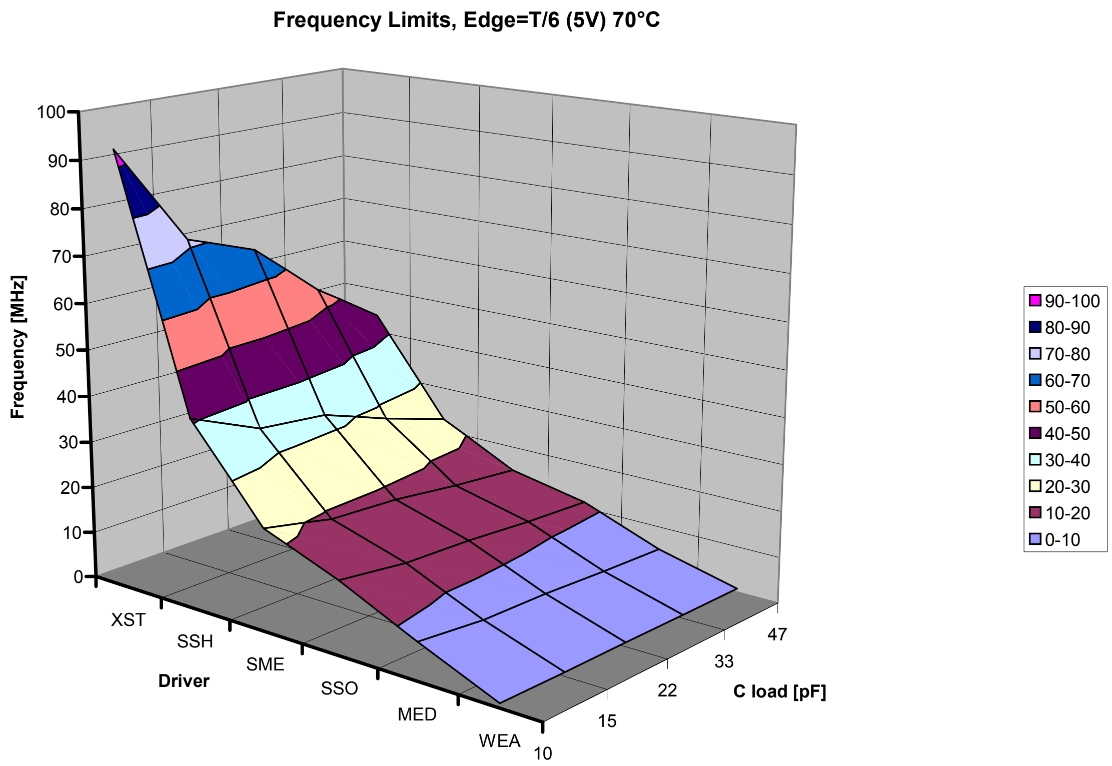

Figure 57: Selection decision graph for driver at T_A=70°C; 5.0V; edges occupy 1/6 period

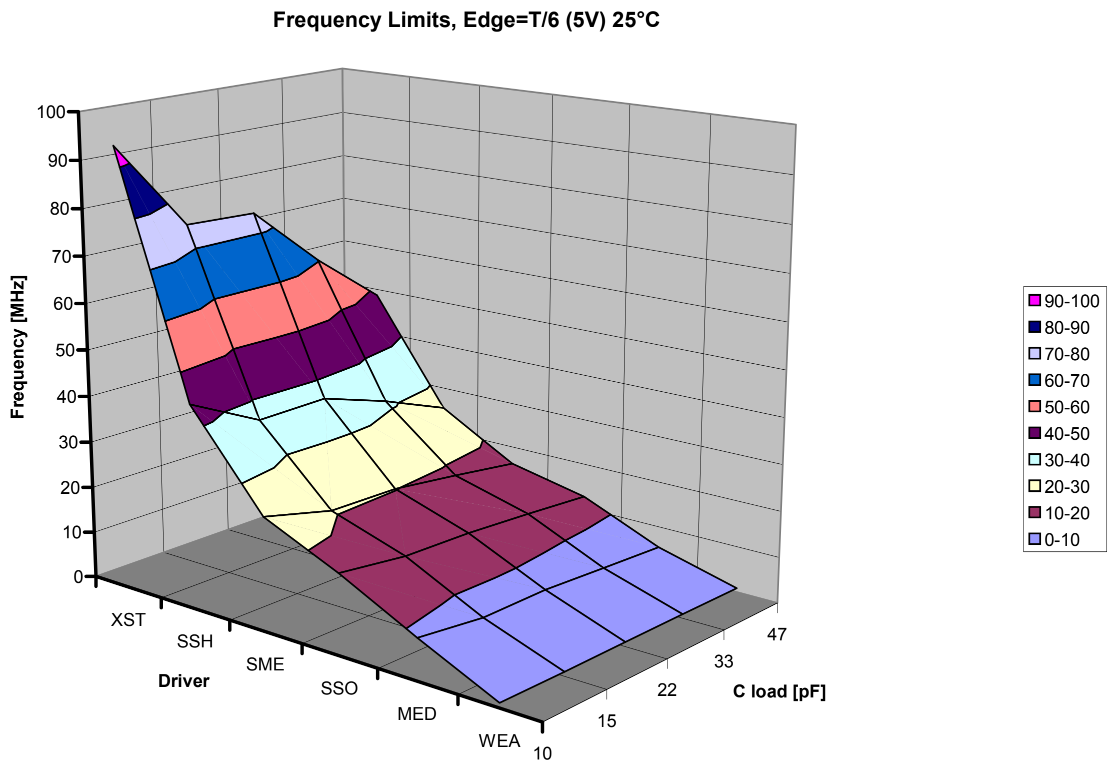

Figure 58: Selection decision graph for driver at T_A=25°C; 5.0V; edges occupy 1/6 period

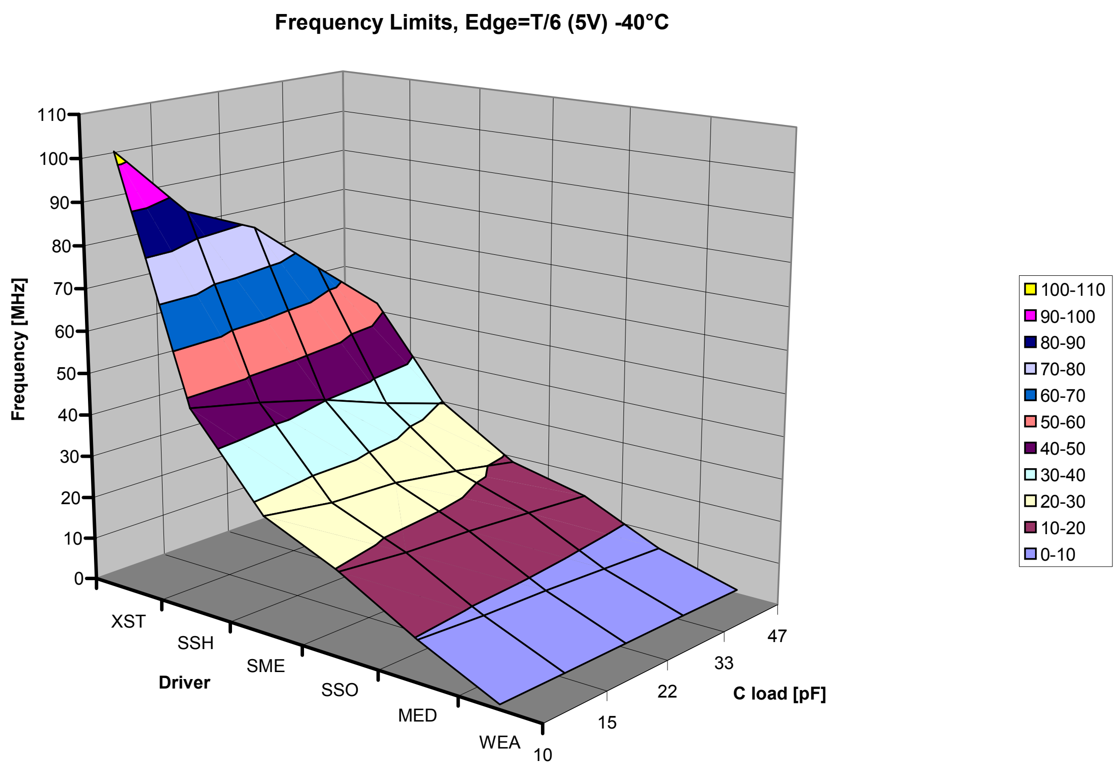

Figure 59: Selection decision graph for driver at T_A=-40°C; 5.0V; edges occupy 1/6 period

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Annex A: Measured rise/fall waveforms

Rise/fall timing diagrams are provided for selected EXTCLK driver settings and capacitive loads, as listed in Table 11. These results have been summarized in Chapter 4. This Annex B shows all measured timing diagrams for reference puposes.

Driver strength	Connected physical capacitor	Resulting load capacitance	VDDP0 supply voltages	Ambient temperatures
Extra-strong	10pF	13 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Extra-strong	15 pF	18 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Extra-strong	22 pF	25 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Extra-strong	33 pF	36 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Extra-strong	47 pF	50 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-sharp	10pF	13 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-sharp	15 pF	18 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-sharp	22 pF	25 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-sharp	33 pF	36 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-sharp	47 pF	50 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-medium	10pF	13 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-medium	15 pF	18 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-medium	22 pF	25 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-medium	33 pF	36 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-medium	47 pF	50 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-soft	10pF	13 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-soft	15 pF	18 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-soft	22 pF	25 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-soft	33 pF	36 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Strong-soft	47 pF	50 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Medium	10pF	13 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Medium	15 pF	18 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Medium	22 pF	25 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Medium	33 pF	36 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Medium	47 pF	50 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Weak	10pF	13 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Weak	15 pF	18 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Weak	22 pF	25 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Weak	33 pF	36 pF	3.3V / 5.0V	-40°C / 25°C / 125°C
Weak	47 pF	50 pF	3.3V / 5.0V	-40°C / 25°C / 125°C

Table 11: List of all timing measurement conditions

Each of Fig. 61-96 contains 5 waveforms for a given driver strength, a given VDDP0 supply voltage (3.3V, 5.0V) and a given ambient temperature (-40°C, 25°C, 125°C). Depending on these settings, certain clock frequencies can be driven or not. The waveforms are measured at a data rate of 500kHz, which allows all driver settings to provide a good signal integrity at loads op to 50pF.

The 5 configurations shown in one figure are distributed as follows:

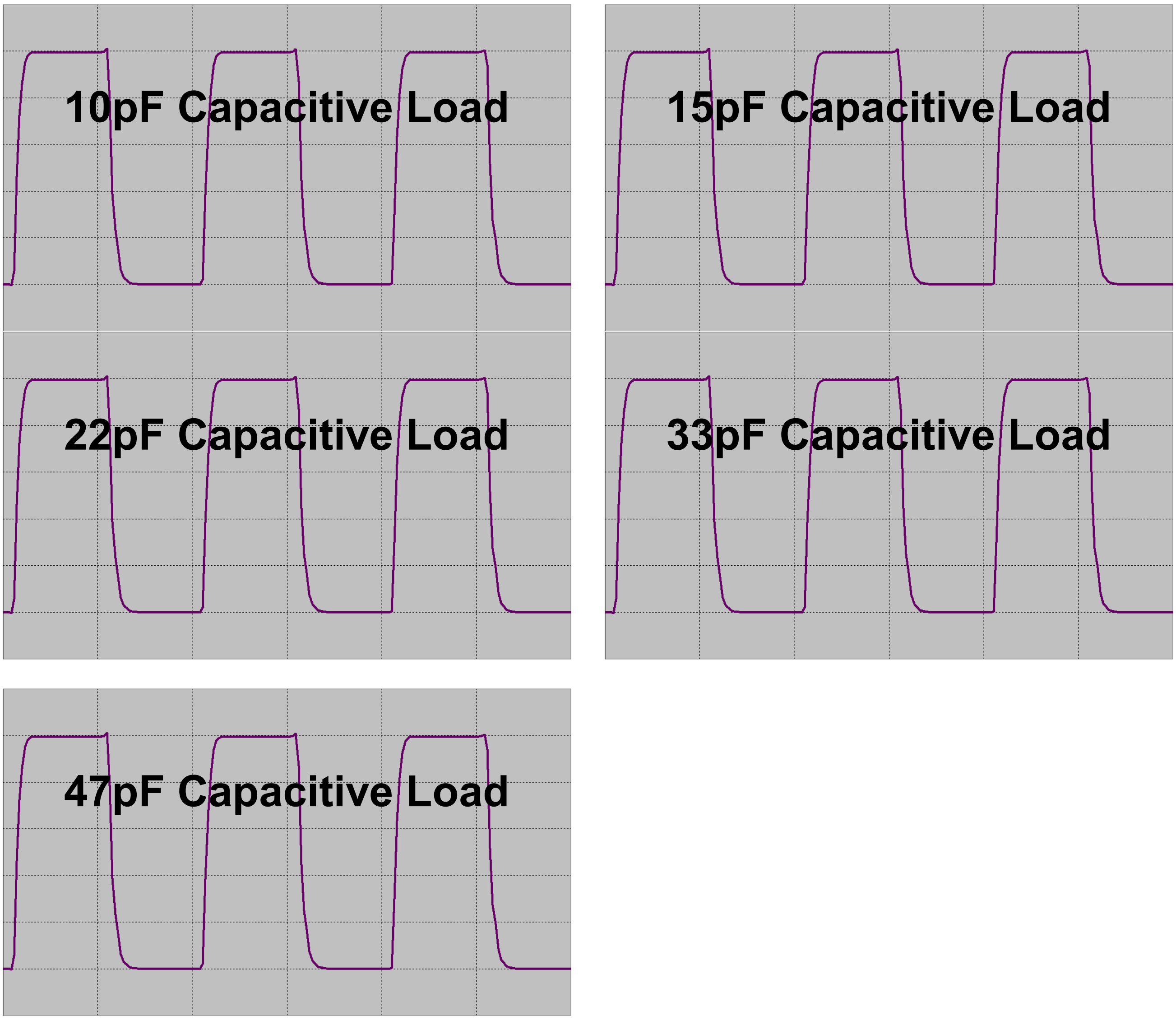

Figure 60: General grouping of waveform configurations

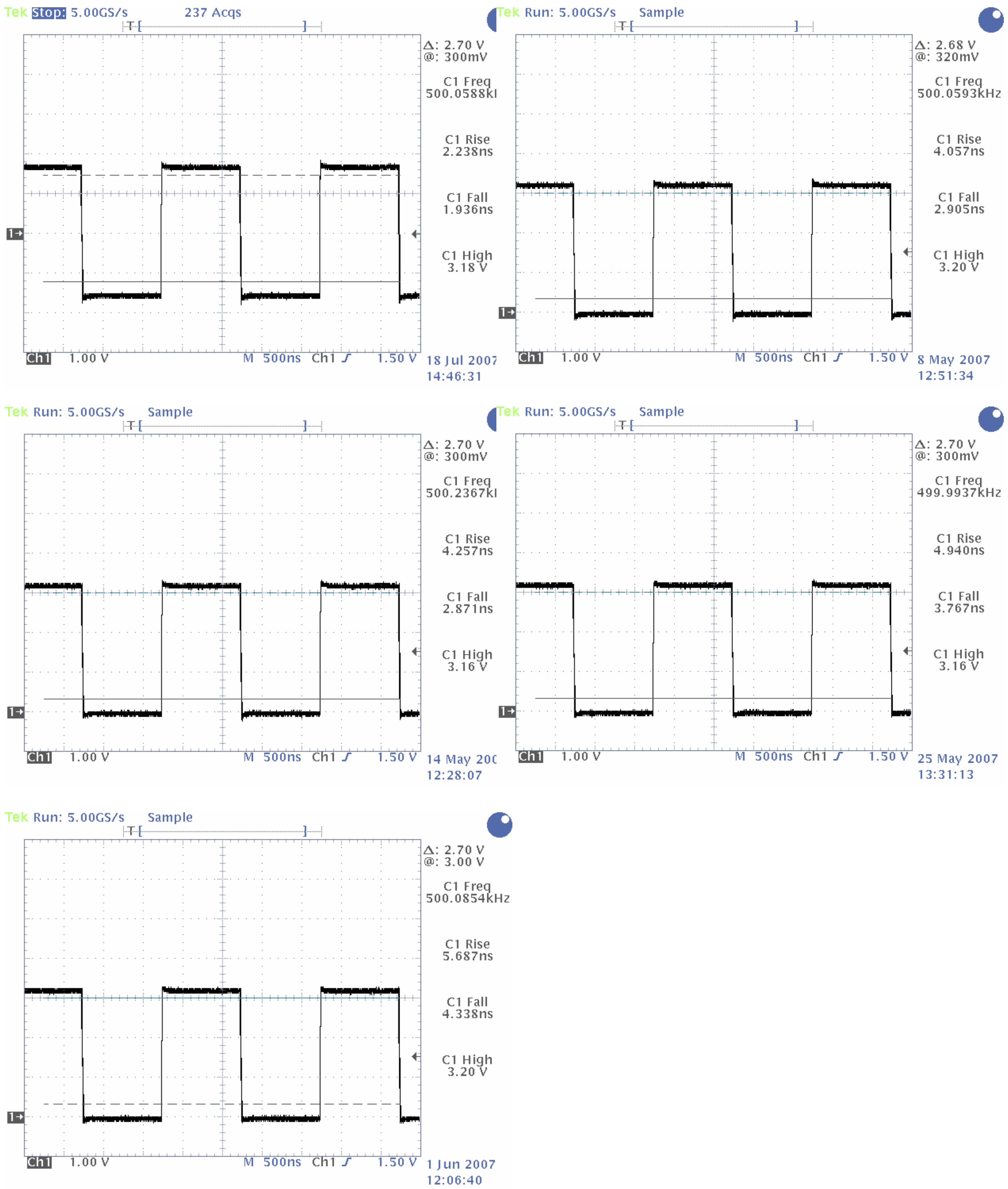

Figure 61: Waveforms EXTCLK 500 kHz "Extra Strong" at 3.3V and at 25°C ambient temperature

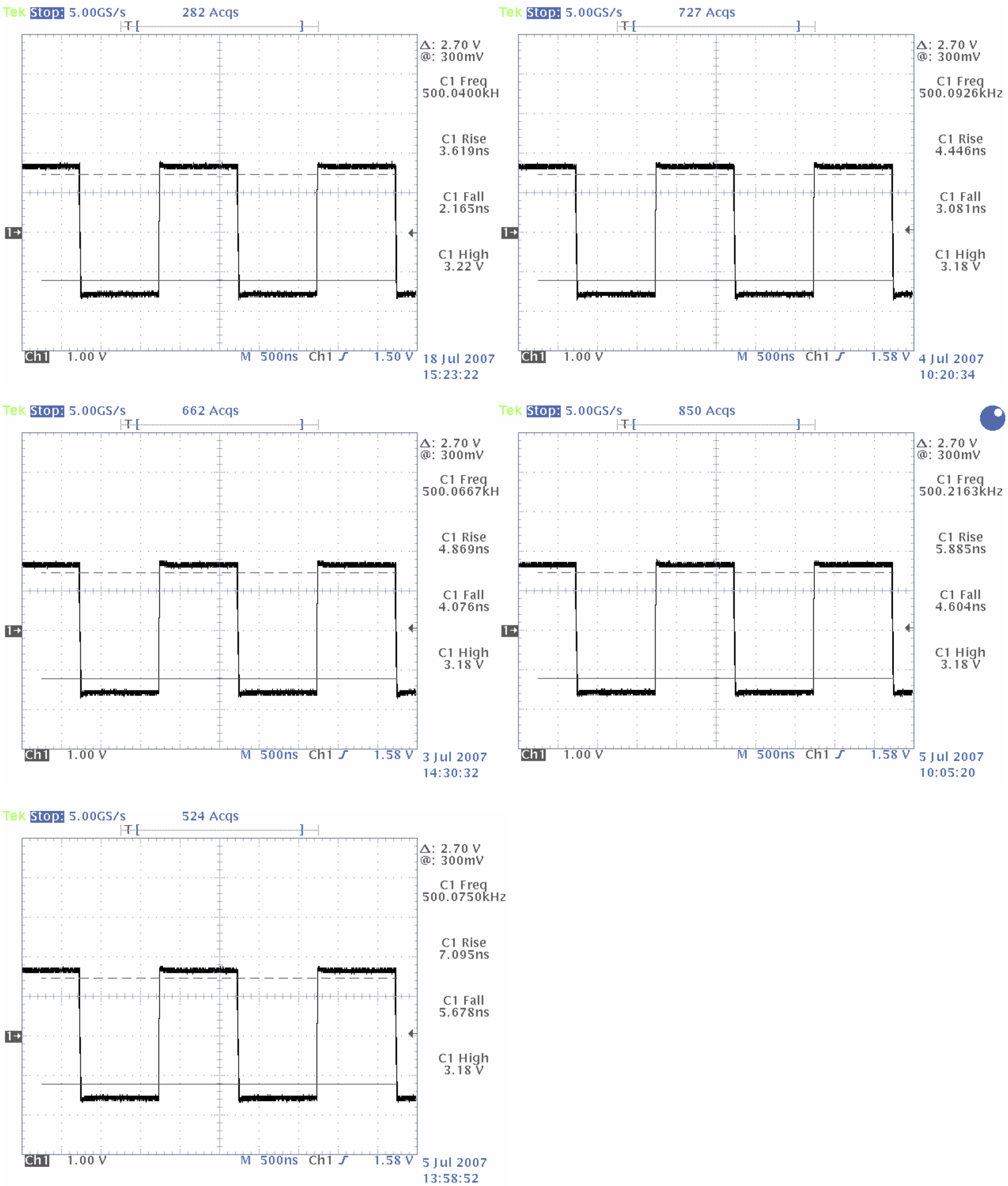

Figure 62: Waveforms EXTCLK 500 kHz “Extra Strong” at 3.3V and at 125°C ambient temperature

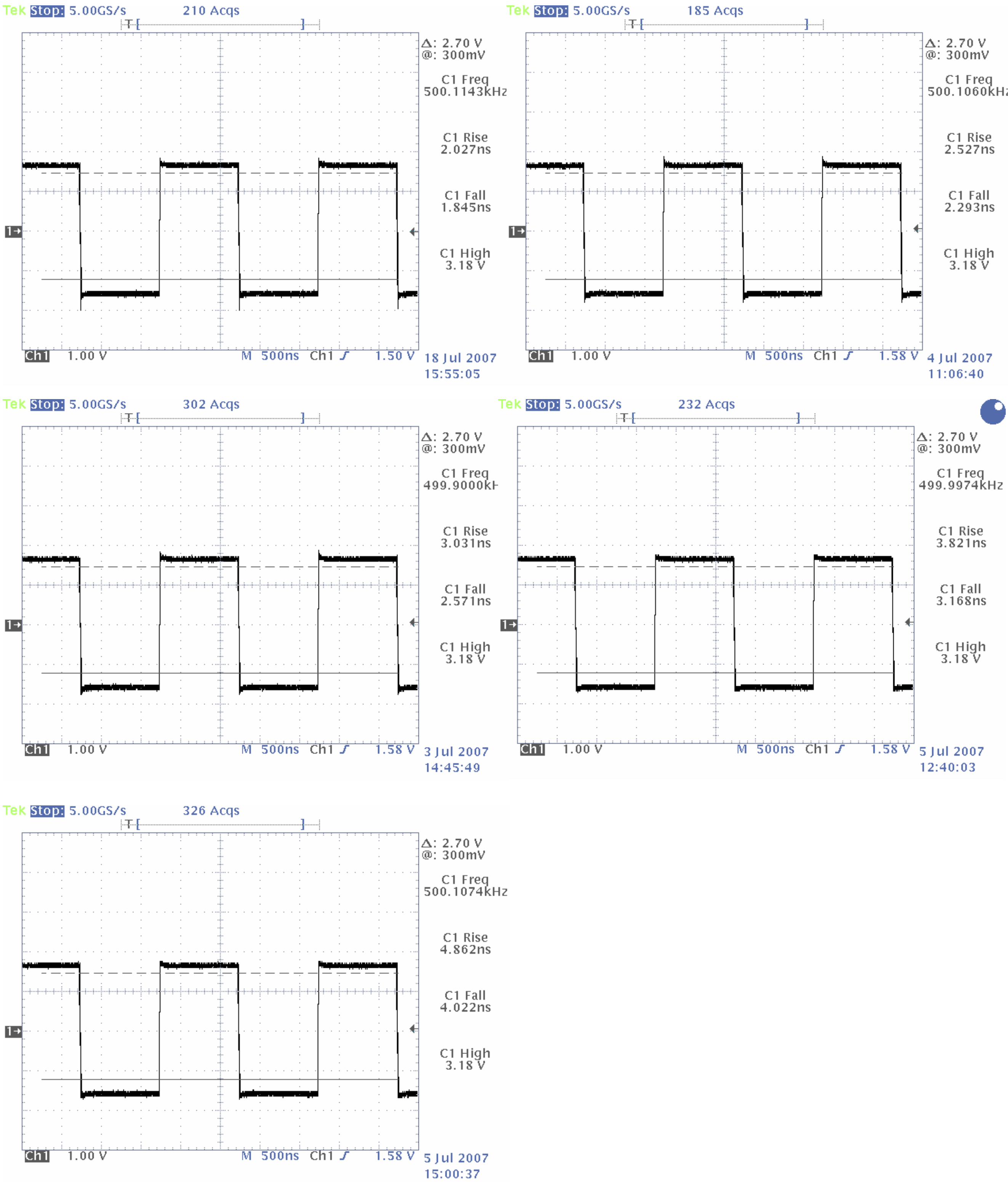

Figure 63: Waveforms EXTCLK 500 kHz "Extra Strong" at 3.3V and at -40°C ambient temperature

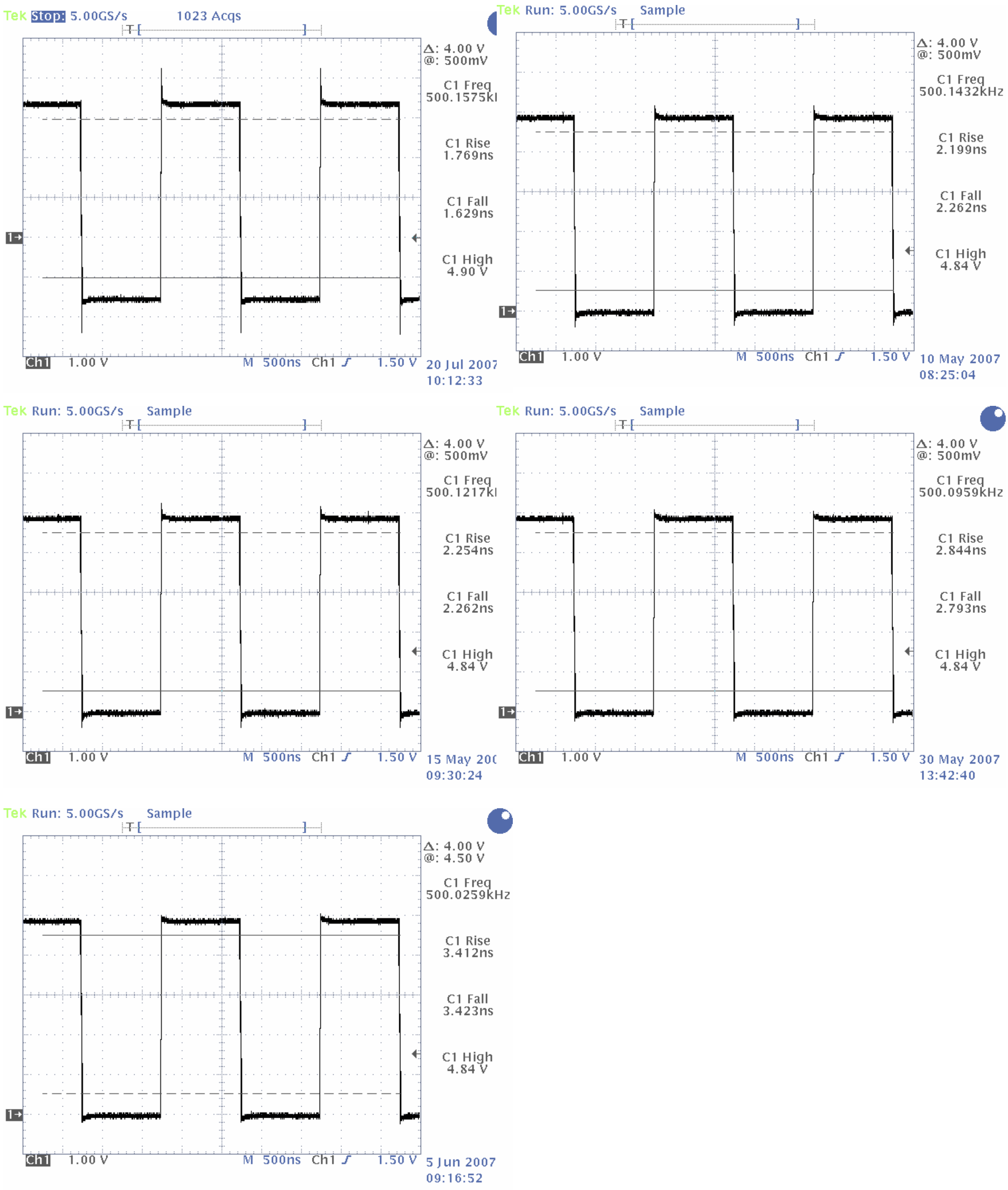

Figure 64: Waveforms EXTCLK 500 kHz "Extra Strong" at 5.0V and at 25°C ambient temperature

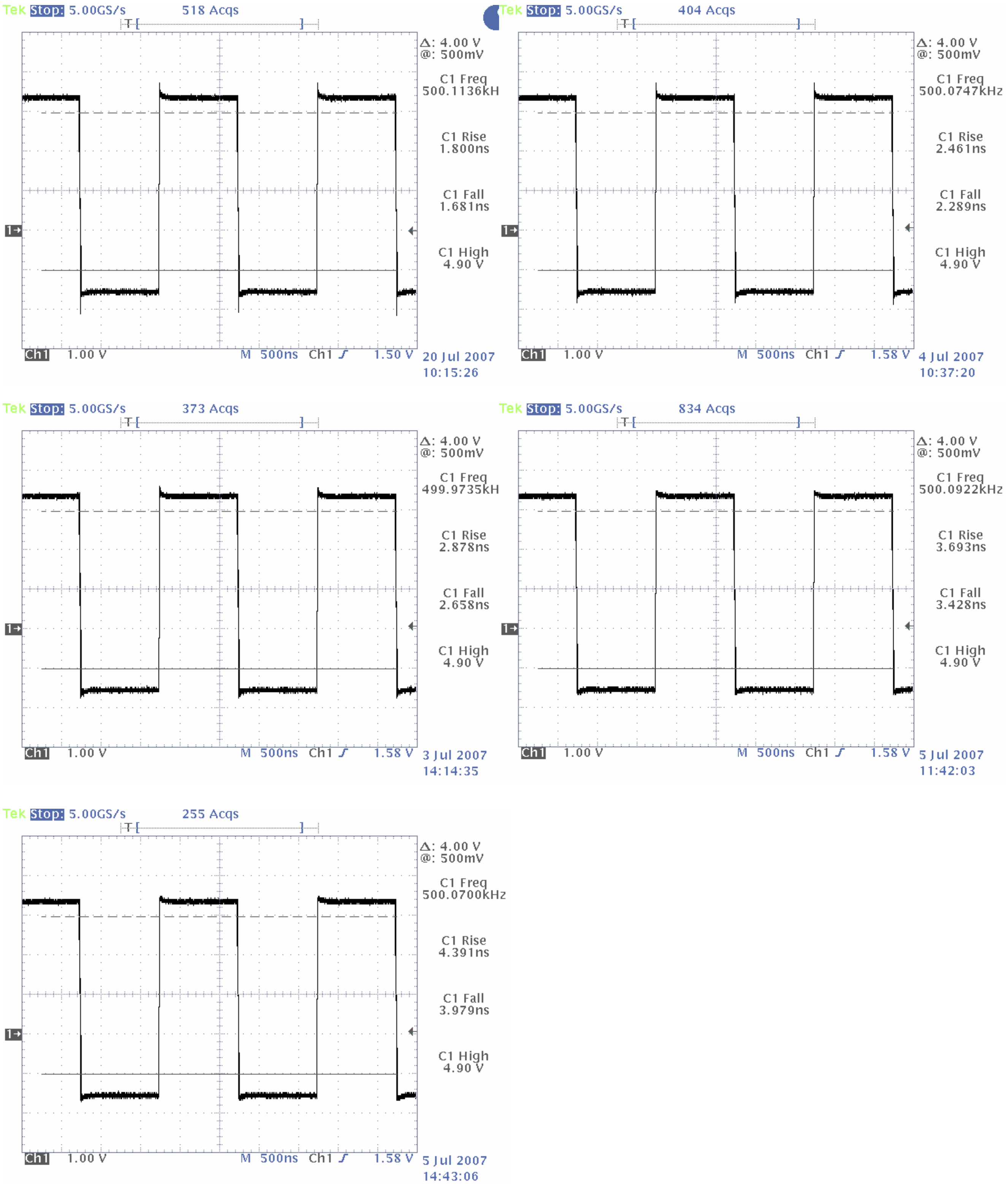

Figure 65: Waveforms EXTCLK 500 kHz "Extra Strong" at 5.0V and at 125°C ambient temperature

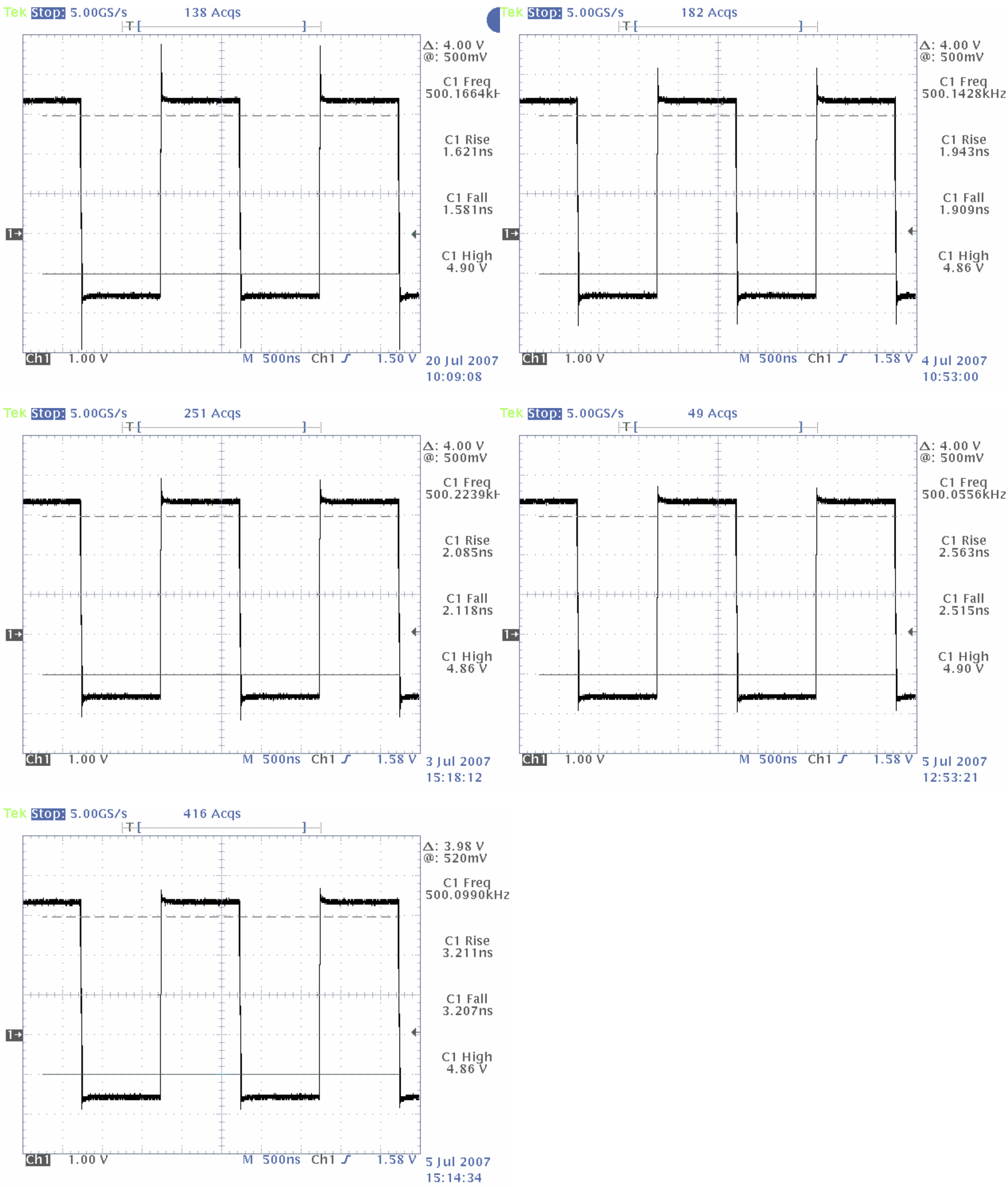

Figure 66: Waveforms EXTCLK 500 kHz “Extra Strong” at 5.0V and at -40°C ambient temperature

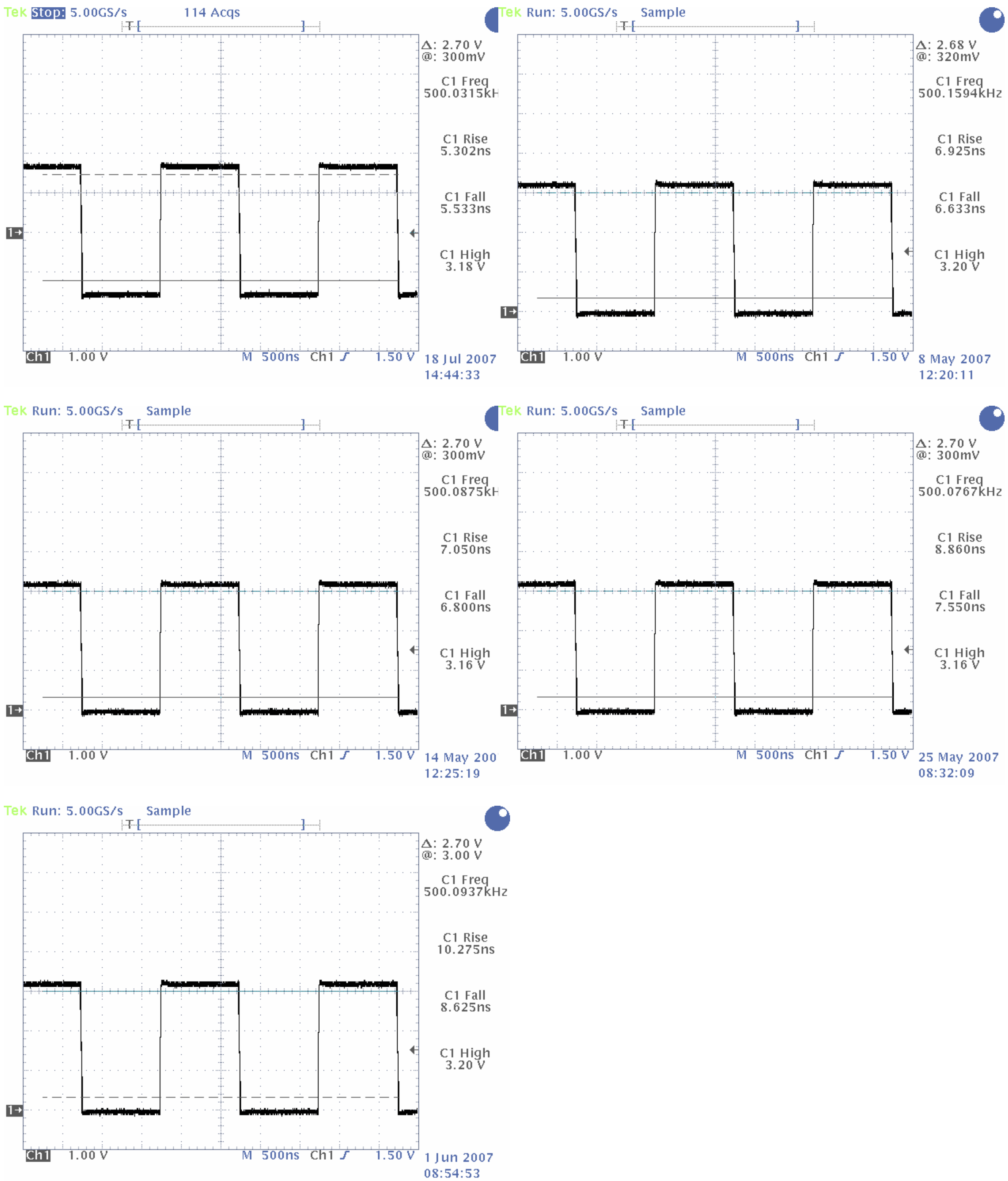

Figure 67: Waveforms EXTCLK 500 kHz “Strong-Sharp” at 3.3V and at 25°C ambient temperature

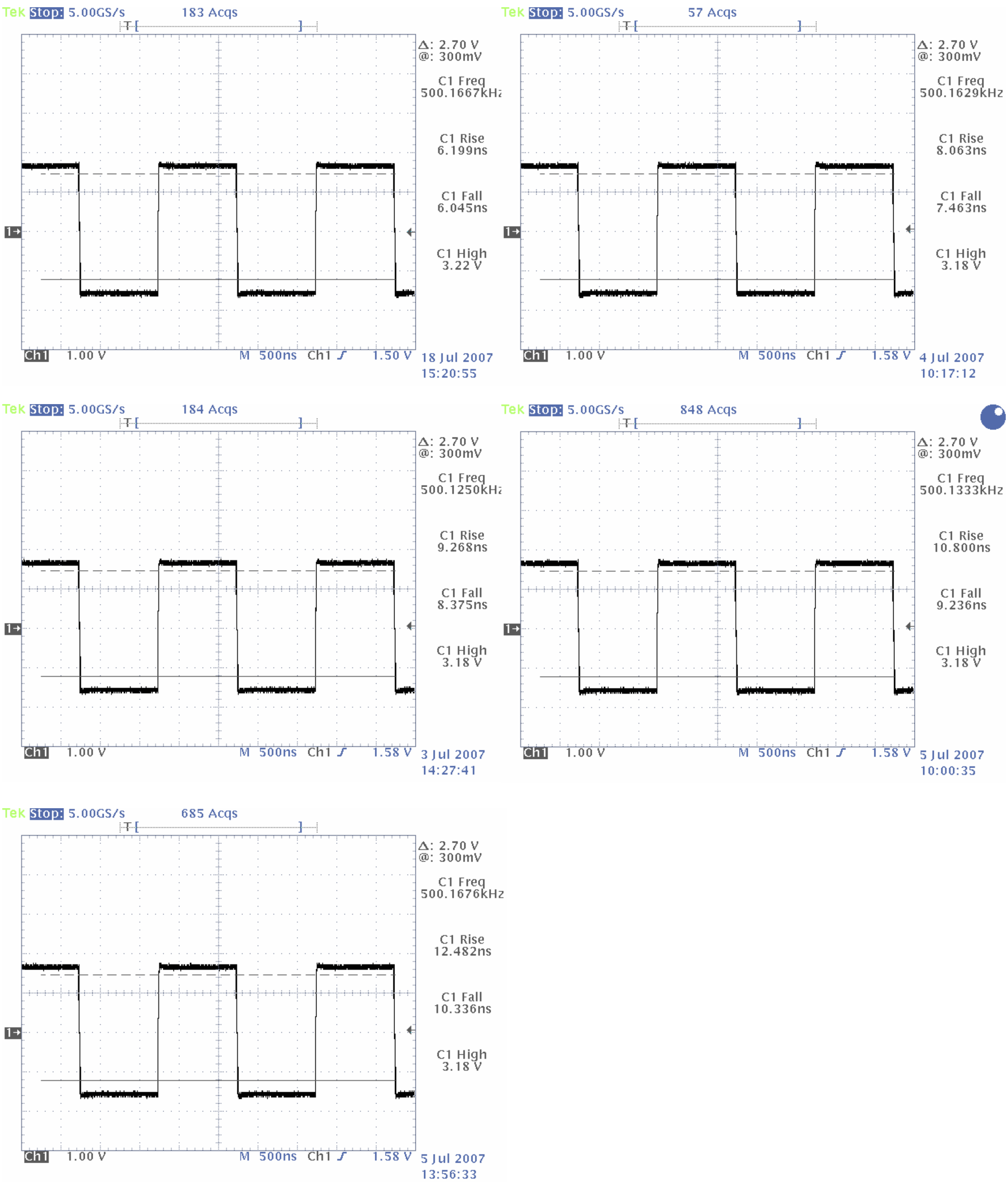

Figure 68: Waveforms EXTCLK 500 kHz “Strong-Sharp” at 3.3V and at 125°C ambient temperature

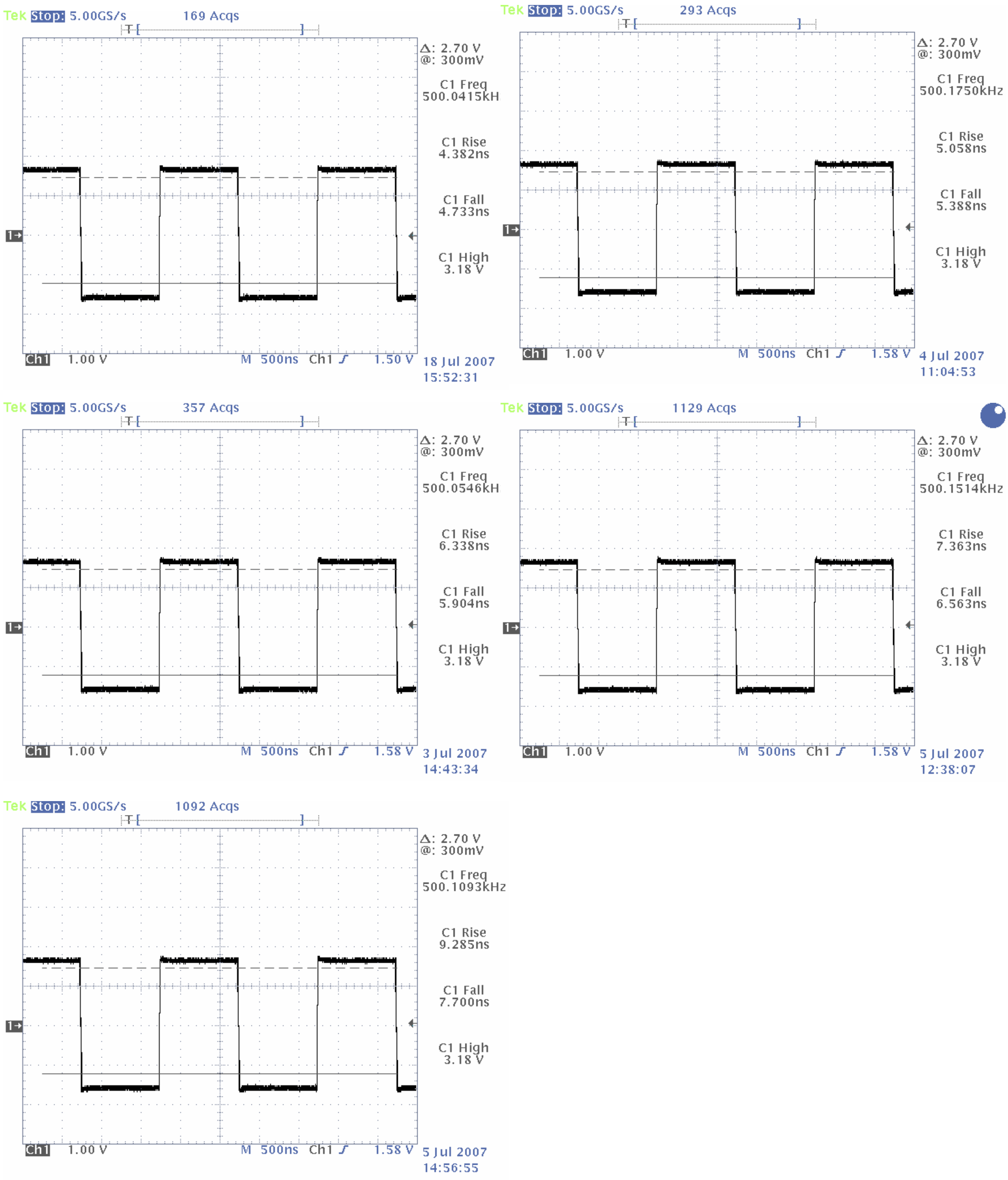

Figure 69: Waveforms EXTCLK 500 kHz "Strong-Sharp" at 3.3V and at -40°C ambient temperature

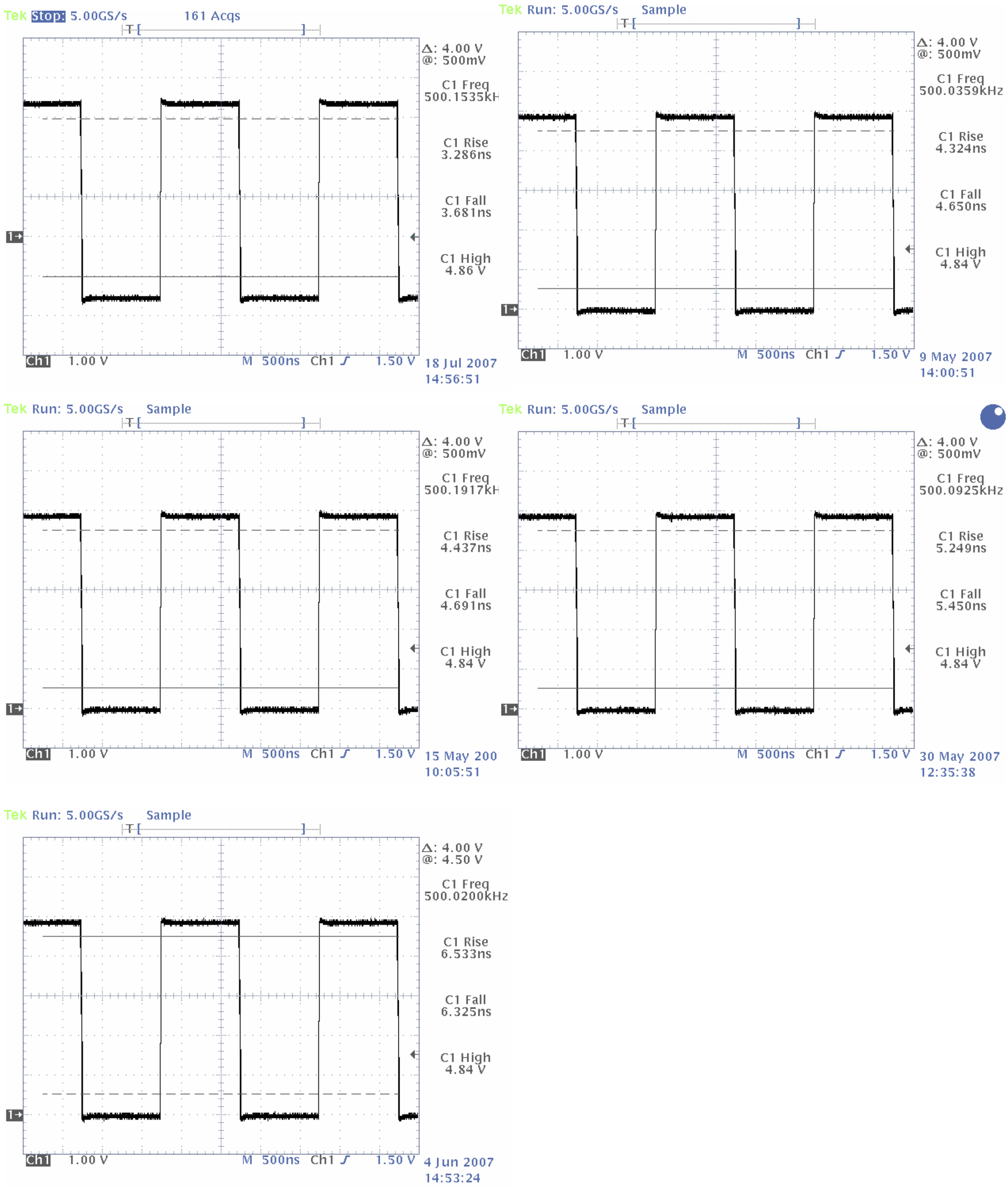

Figure 70: Waveforms EXTCLK 500 kHz "Strong-Sharp" at 5.0V and at 25°C ambient temperature

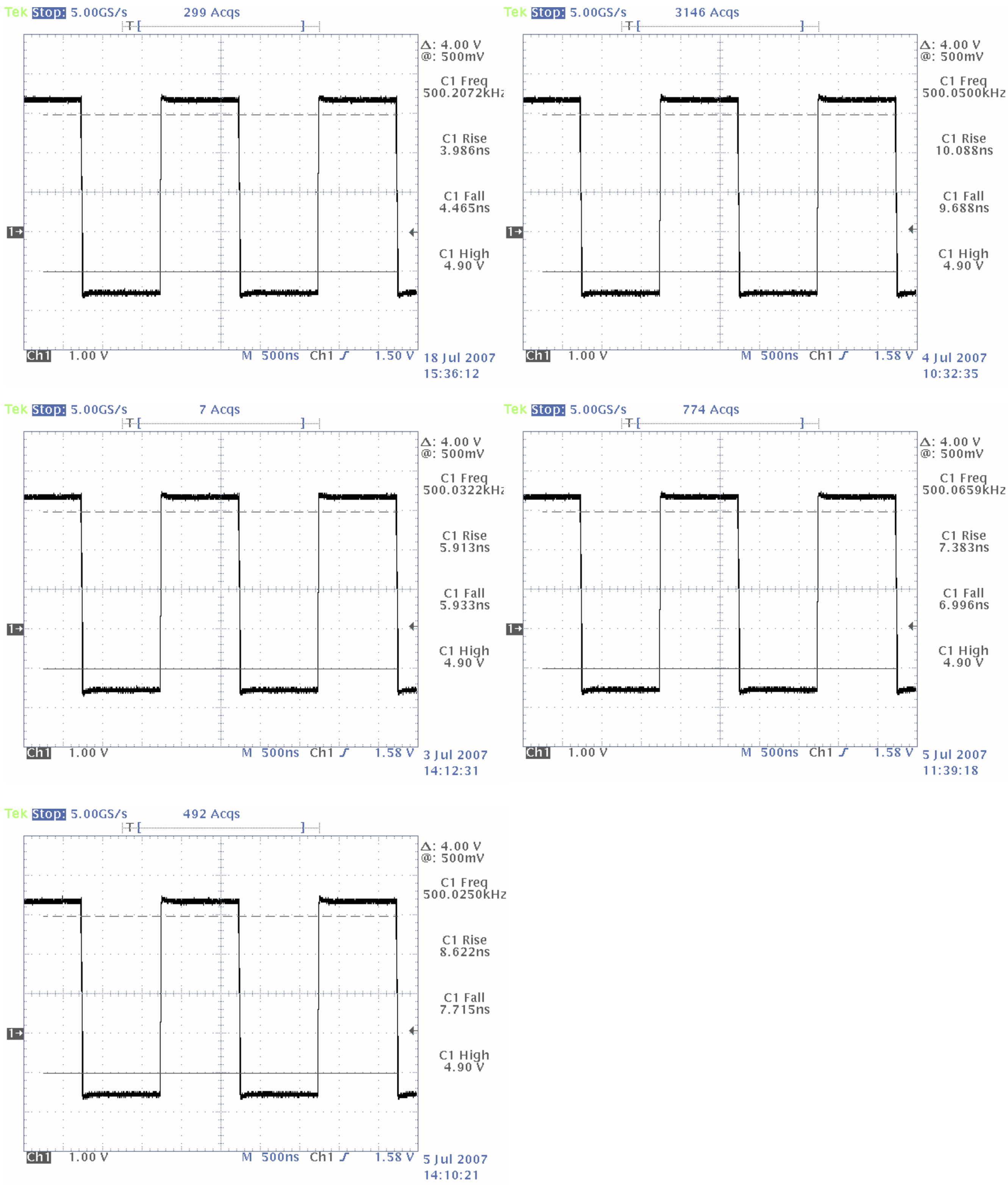

Figure 71: Waveforms EXTCLK 500 kHz "Strong-Sharp" at 5.0V and at 125°C ambient temperature

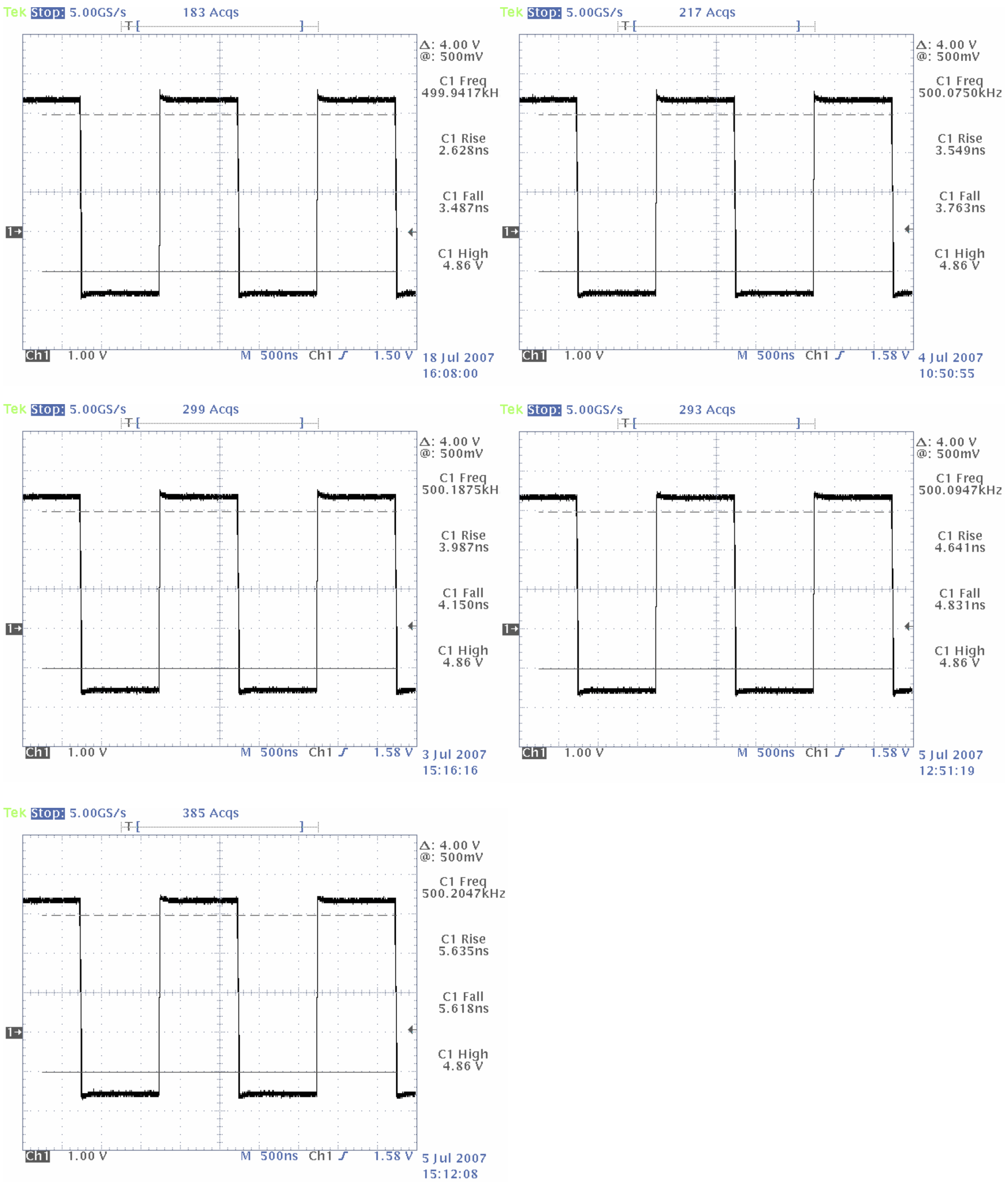

Figure 72: Waveforms EXTCLK 500 kHz "Strong-Sharp" at 5.0V and at -40°C ambient temperature

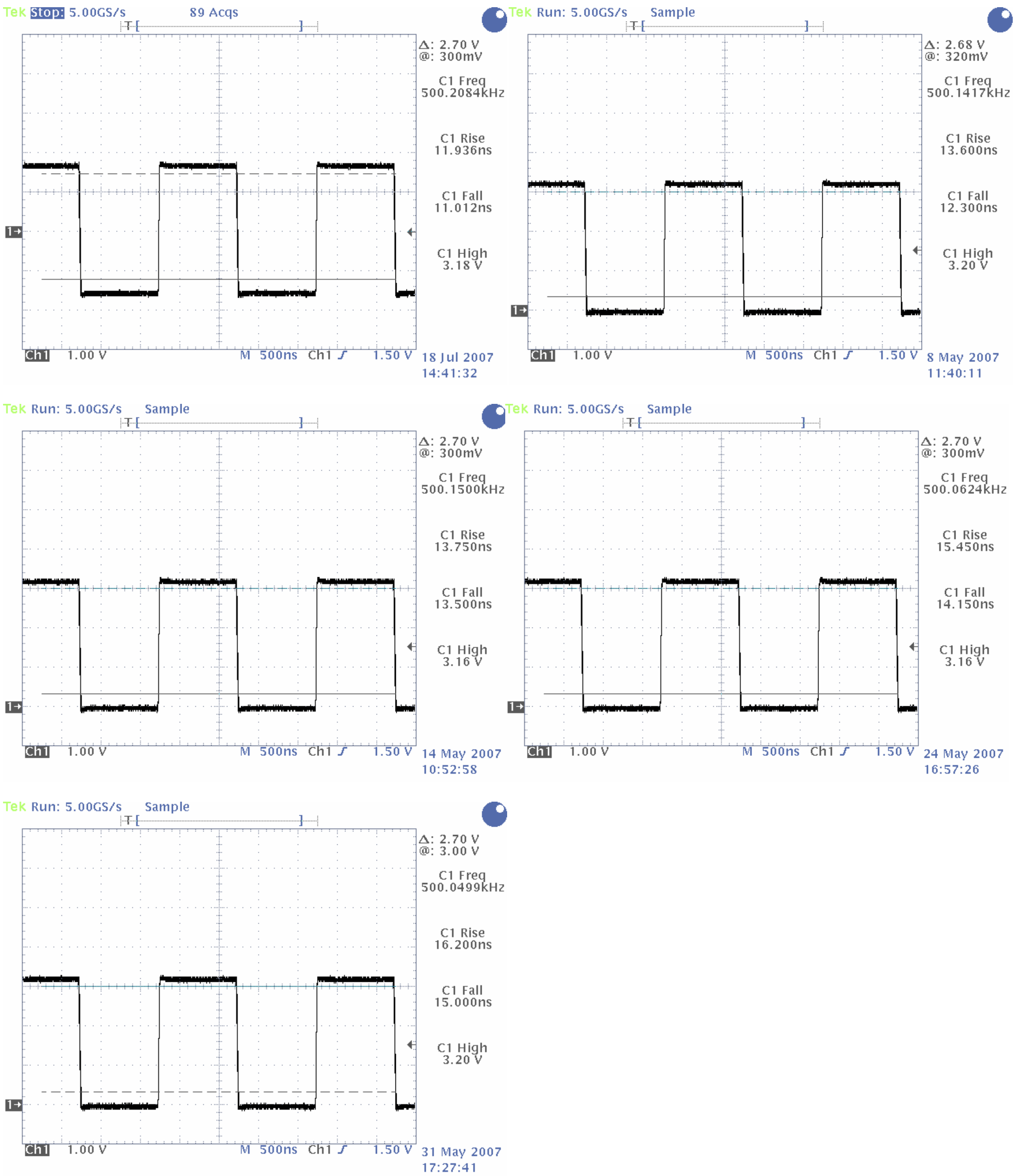

Figure 73: Waveforms EXTCLK 500 kHz "Strong-Medium" at 3.3V and at 25°C ambient temperature

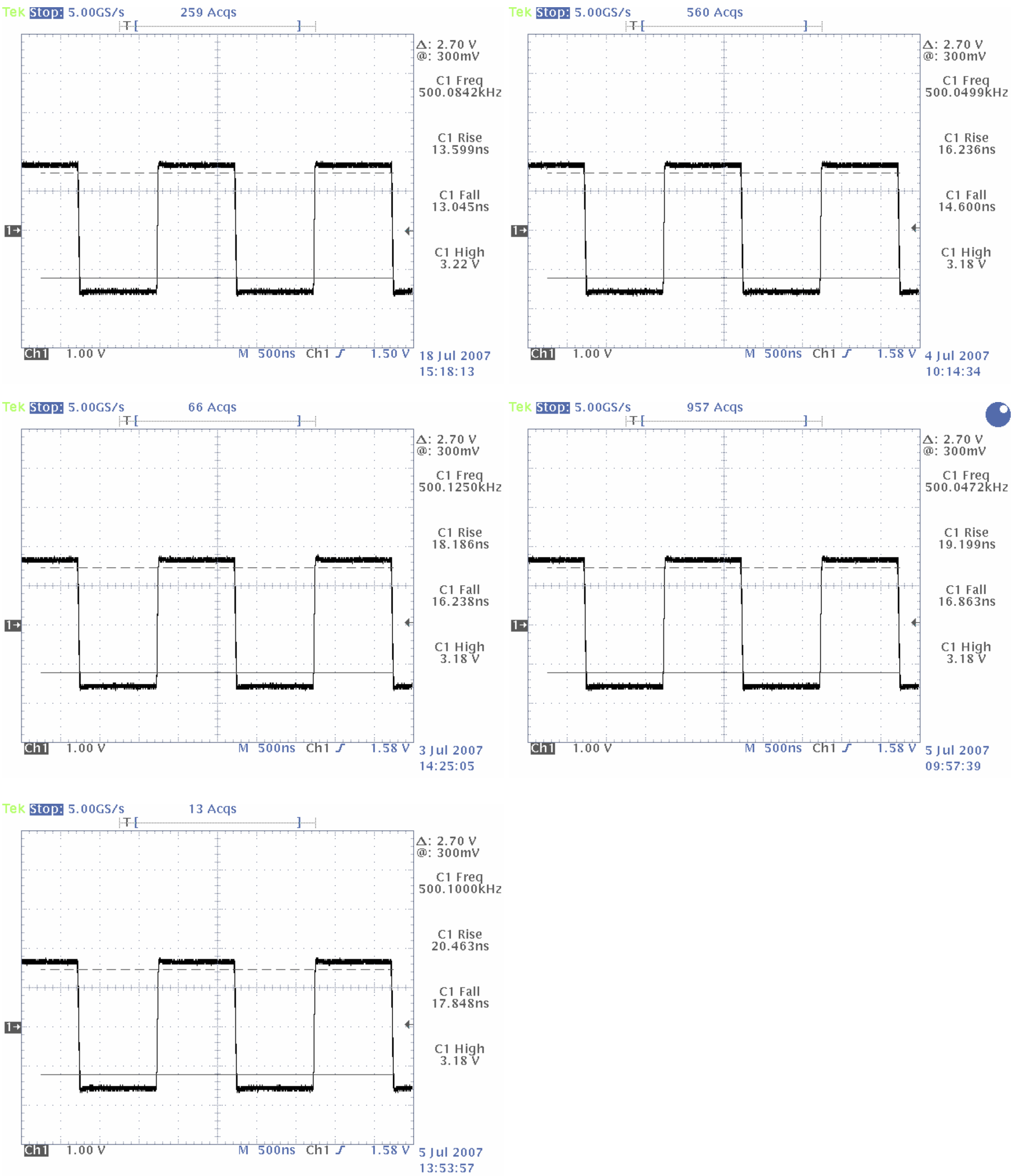

Figure 74: Waveforms EXTCLK 500 kHz “Strong-Medium” at 3.3V and at 125°C ambient temperature

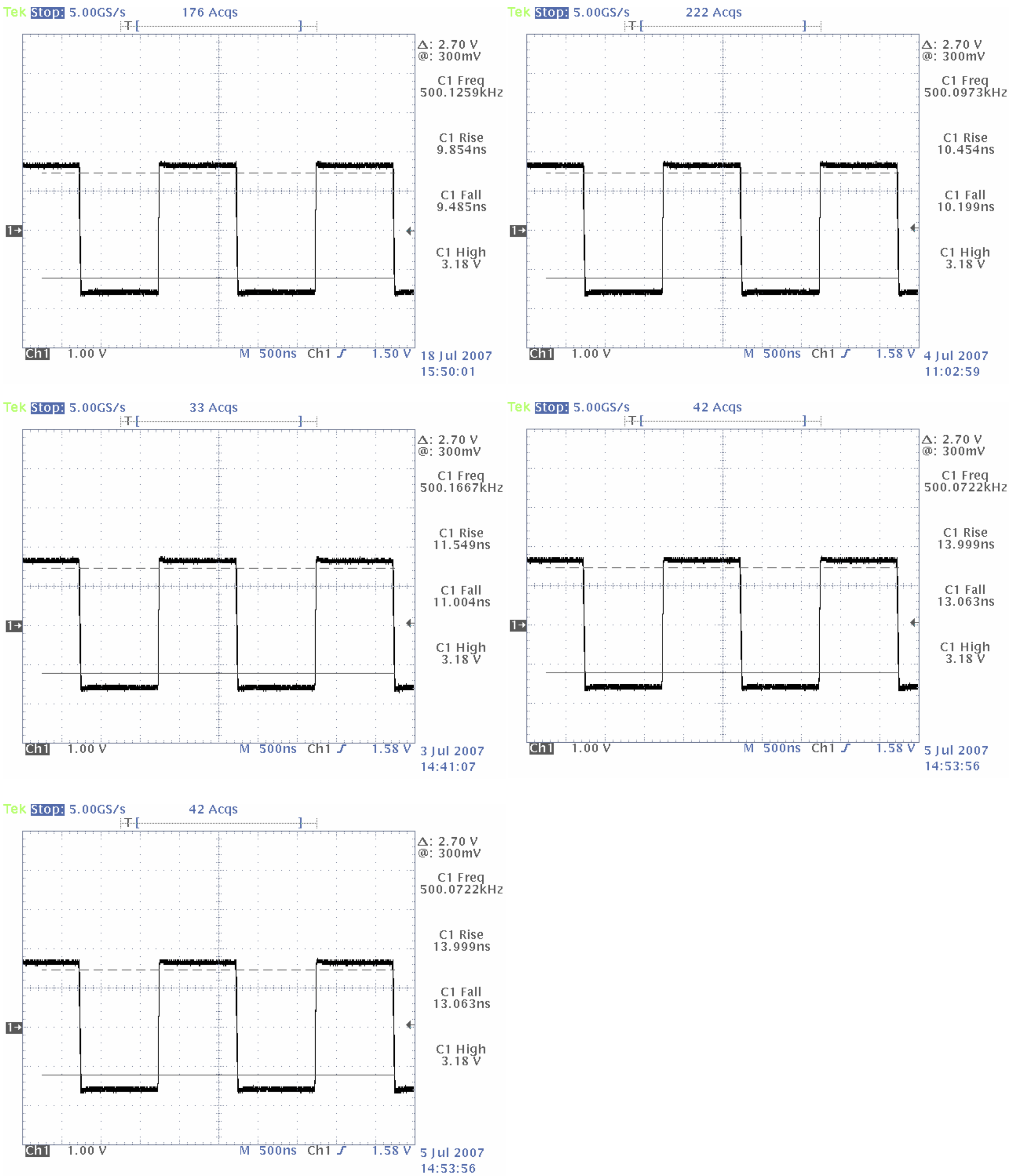

Figure 75: Waveforms EXTCLK 500 kHz “Strong-Medium” at 3.3V and at -40°C ambient temperature

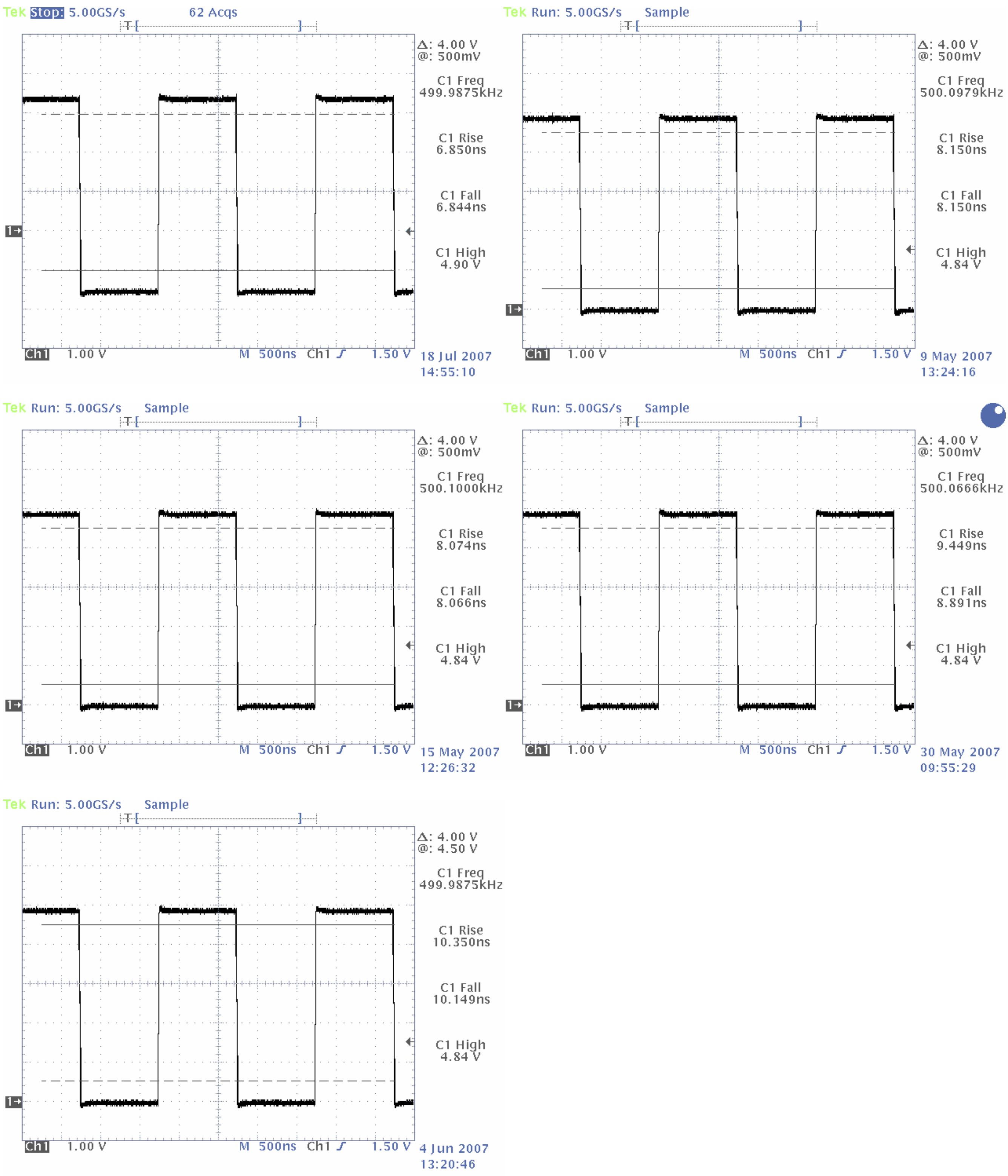

Figure 76: Waveforms EXTCLK 500 kHz "Strong-Medium" at 5.0V and at 25°C ambient temperature

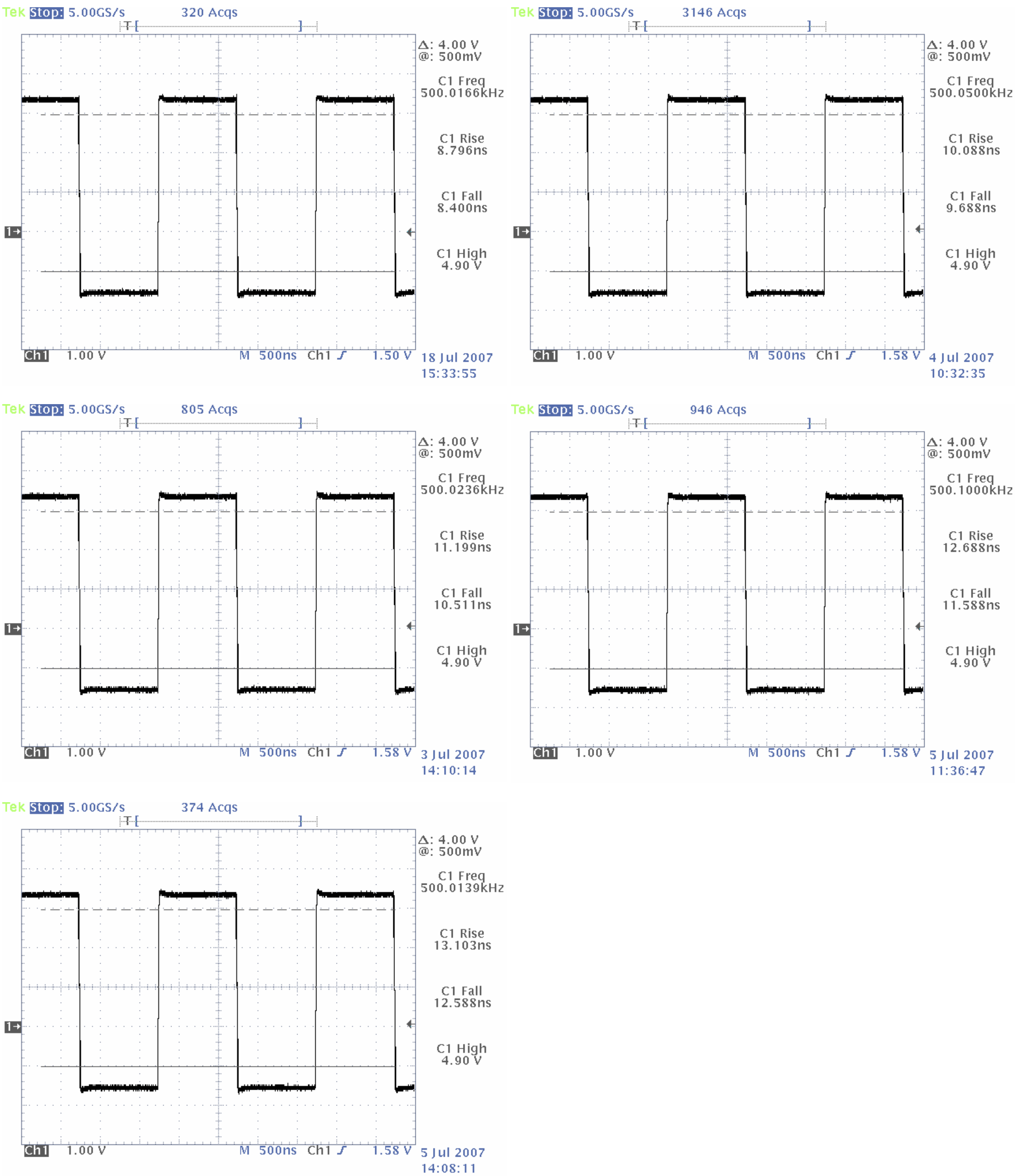

Figure 77: Waveforms EXTCLK 500 kHz “Strong-Medium” at 5.0V and at 125°C ambient temperature

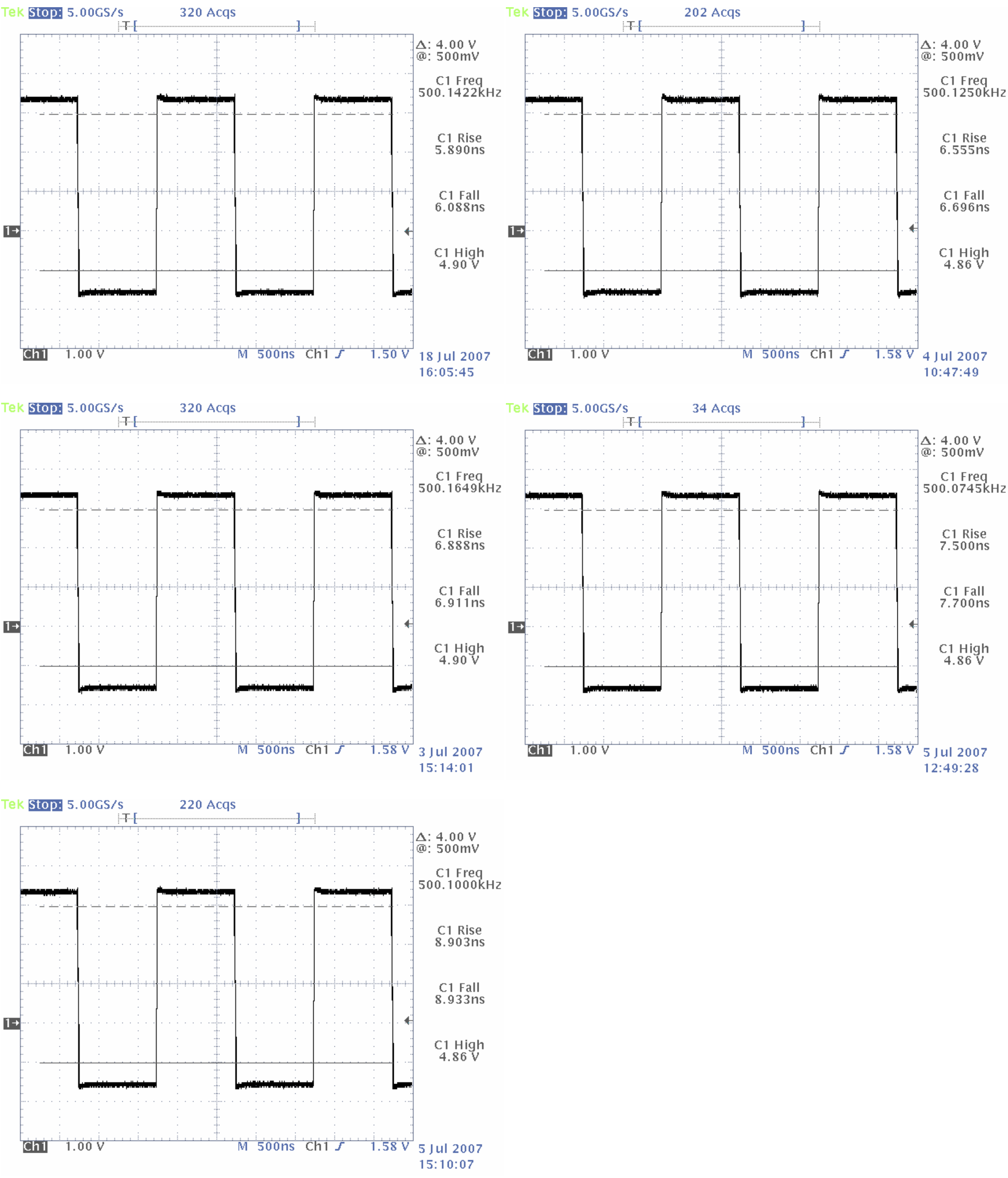

Figure 78: Waveforms EXTCLK 500 kHz “Strong-Medium” at 5.0V and at -40°C ambient temperature

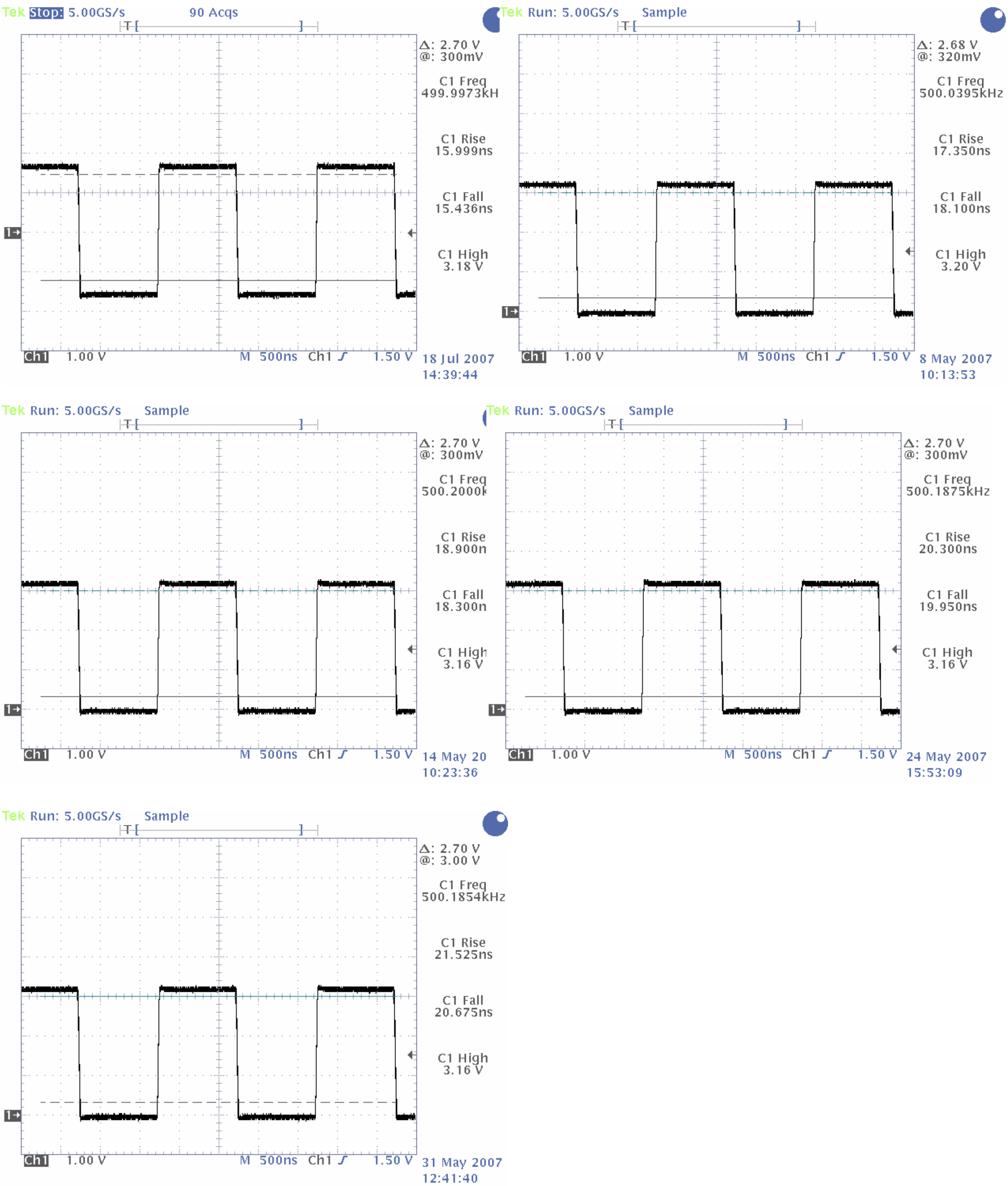

Figure 79: Waveforms EXTCLK 500 kHz "Strong-Soft" at 3.3V and at 25°C ambient temperature

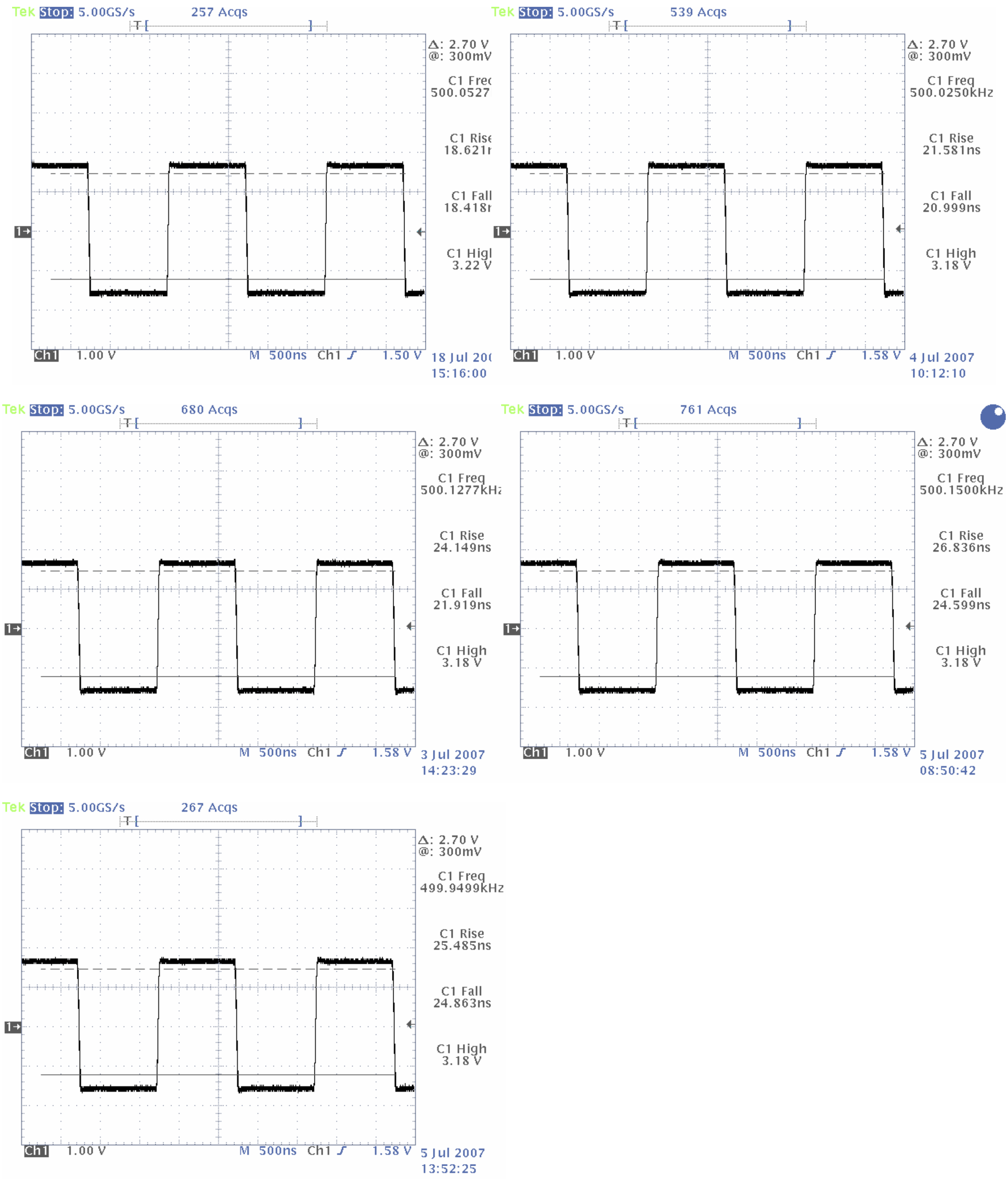

Figure 80: Waveforms EXTCLK 500 kHz “Strong-Soft” at 3.3V and at 125°C ambient temperature

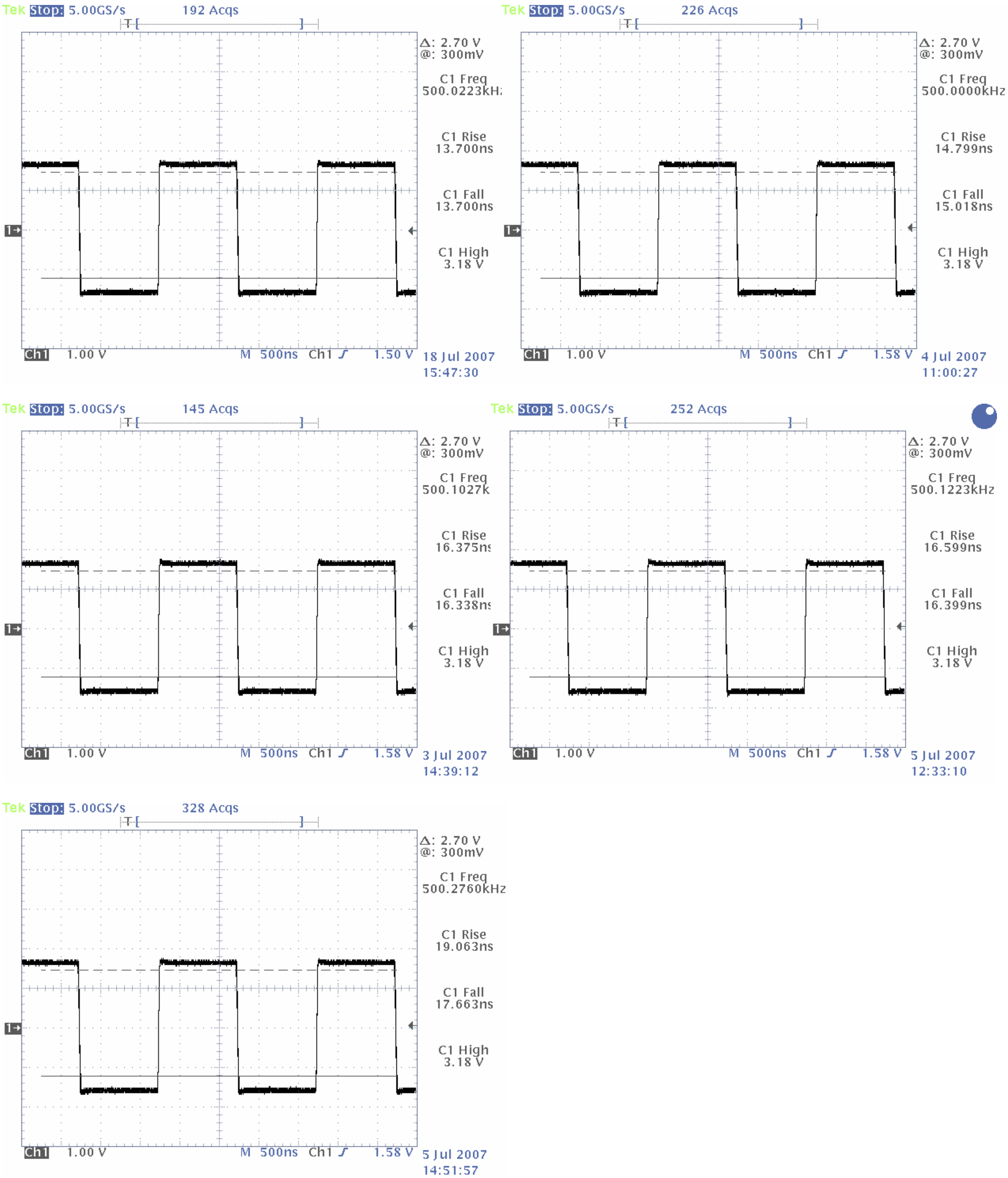

Figure 81: Waveforms EXTCLK 500 kHz "Strong-Soft" at 3.3V and at -40°C ambient temperature

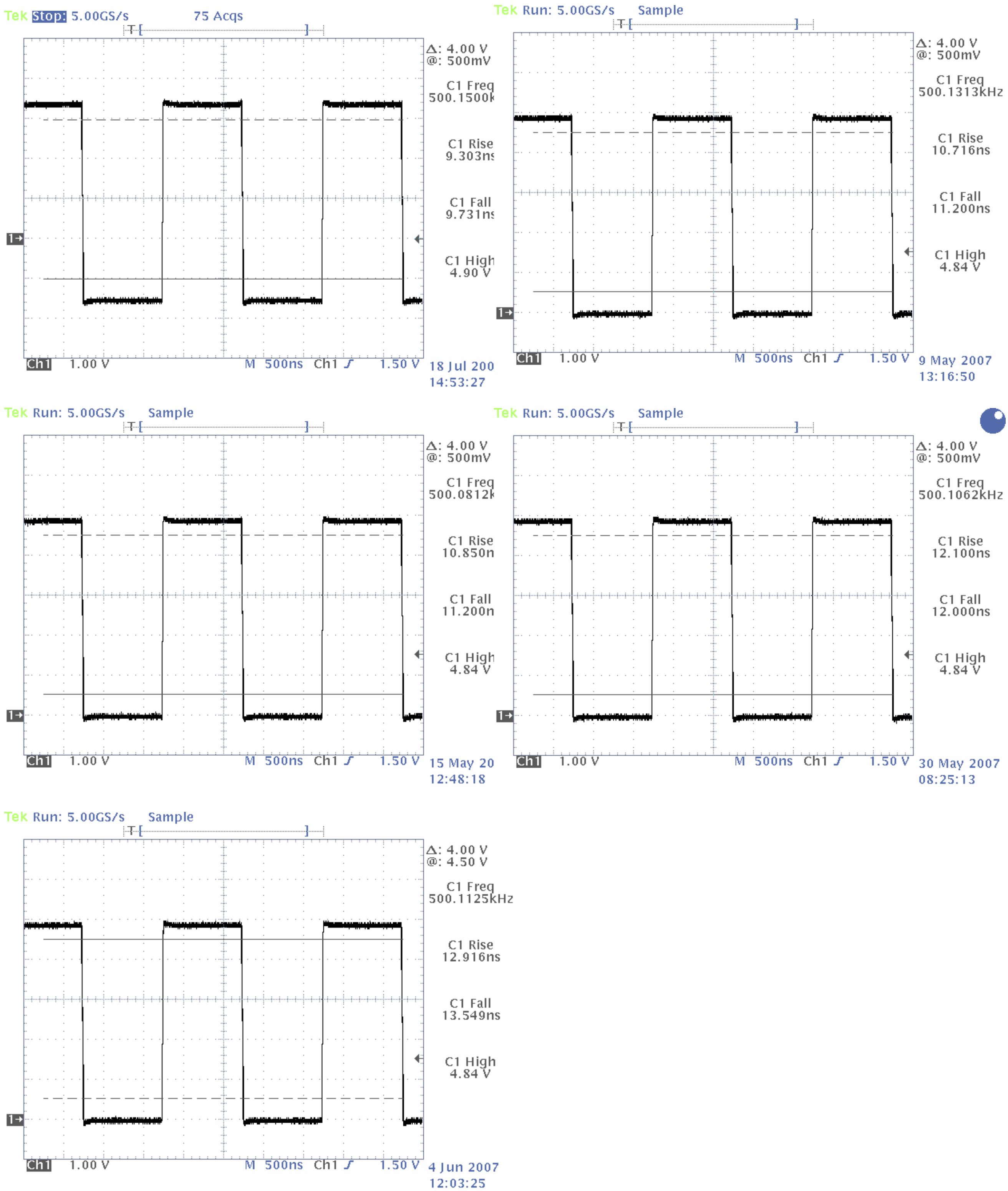

Figure 82: Waveforms EXTCLK 500 kHz “Strong-Soft” at 5.0V and at 25°C ambient temperature

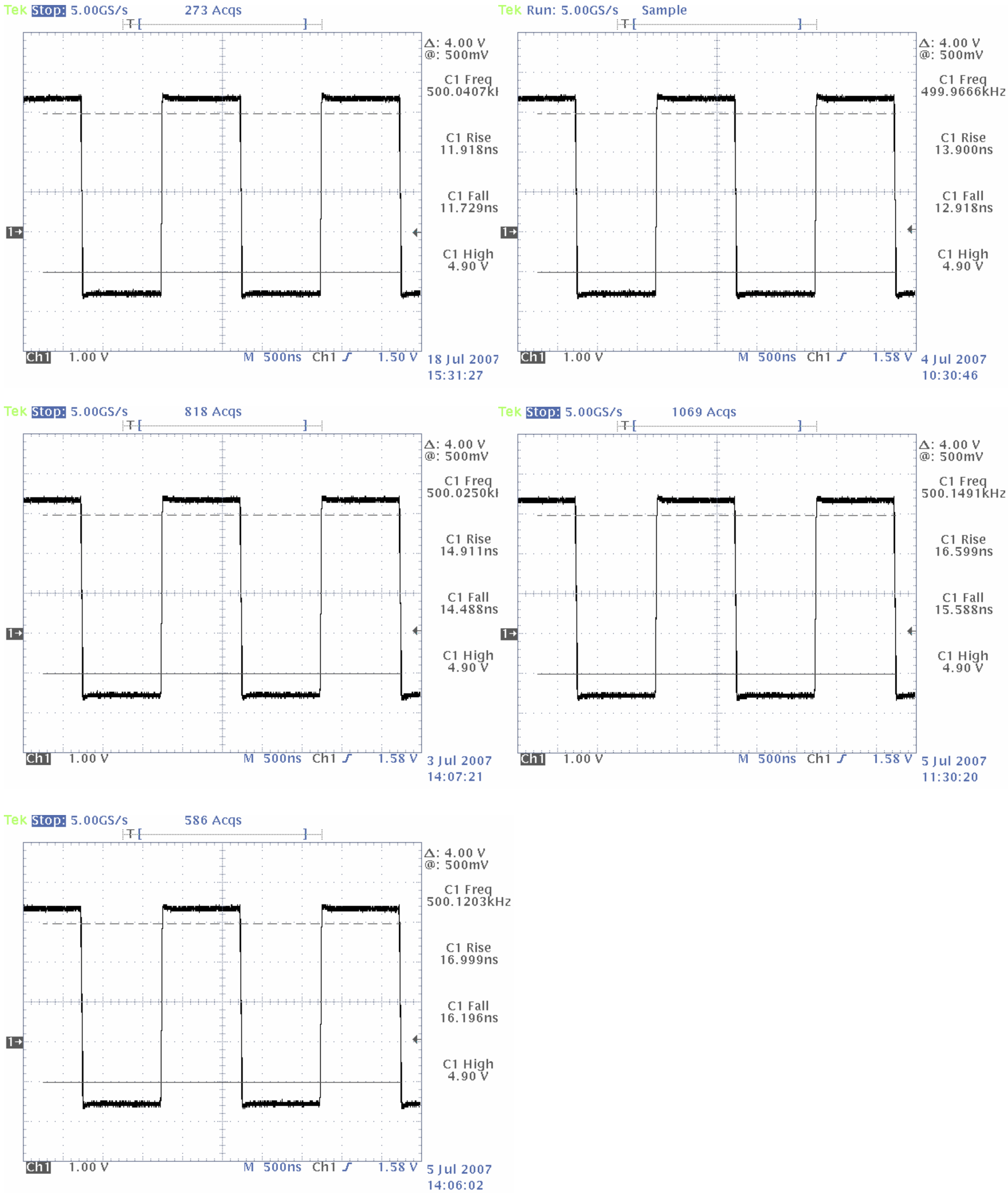

Figure 83: Waveforms EXTCLK 500 kHz "Strong-Soft" at 5.0V and at 125°C ambient temperature

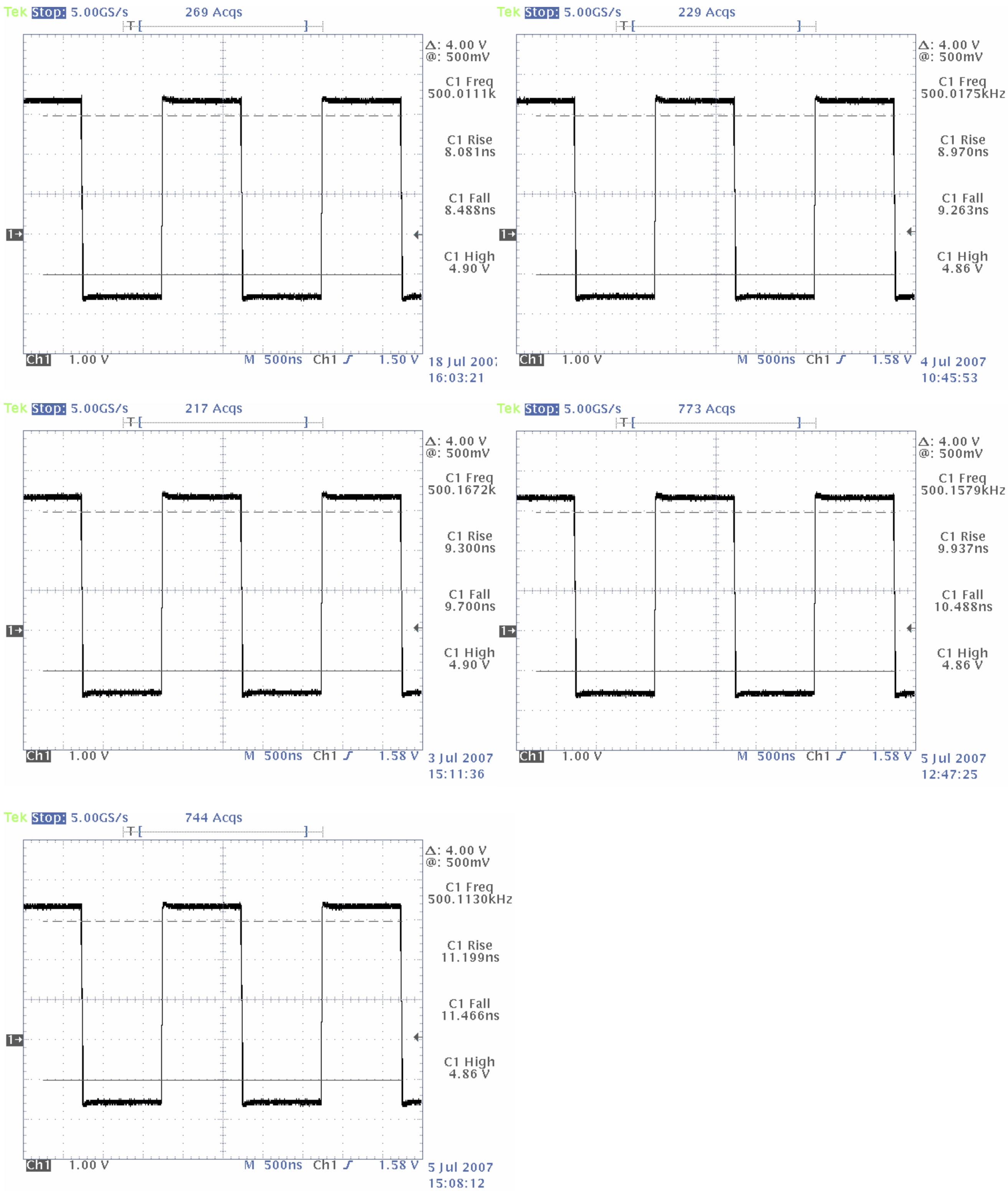

Figure 84: Waveforms EXTCLK 500 kHz “Strong-Soft” at 5.0V and at -40°C ambient temperature

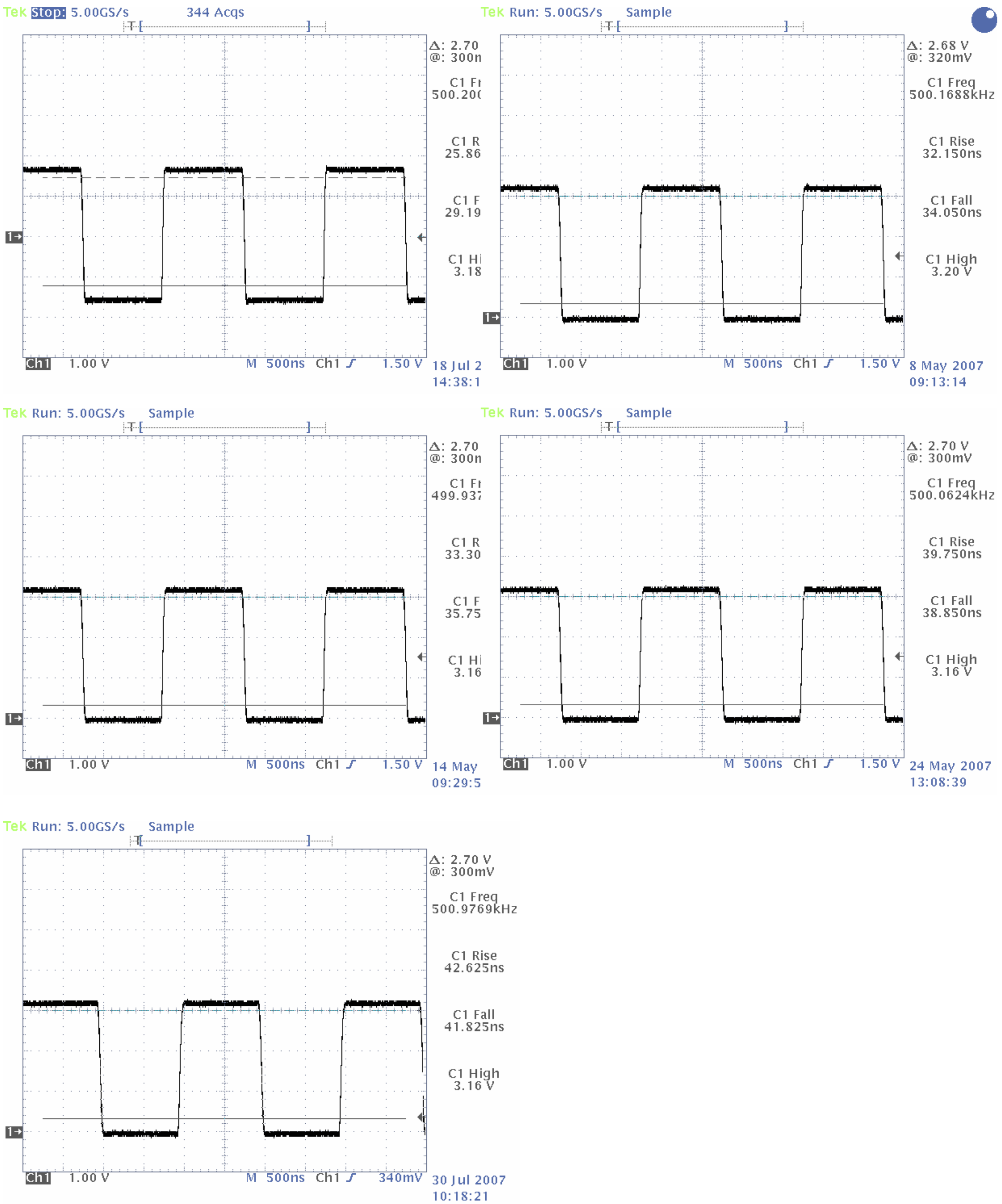

Figure 85: Waveforms EXTCLK 500 kHz "Medium" at 3.3V and at 25°C ambient temperature

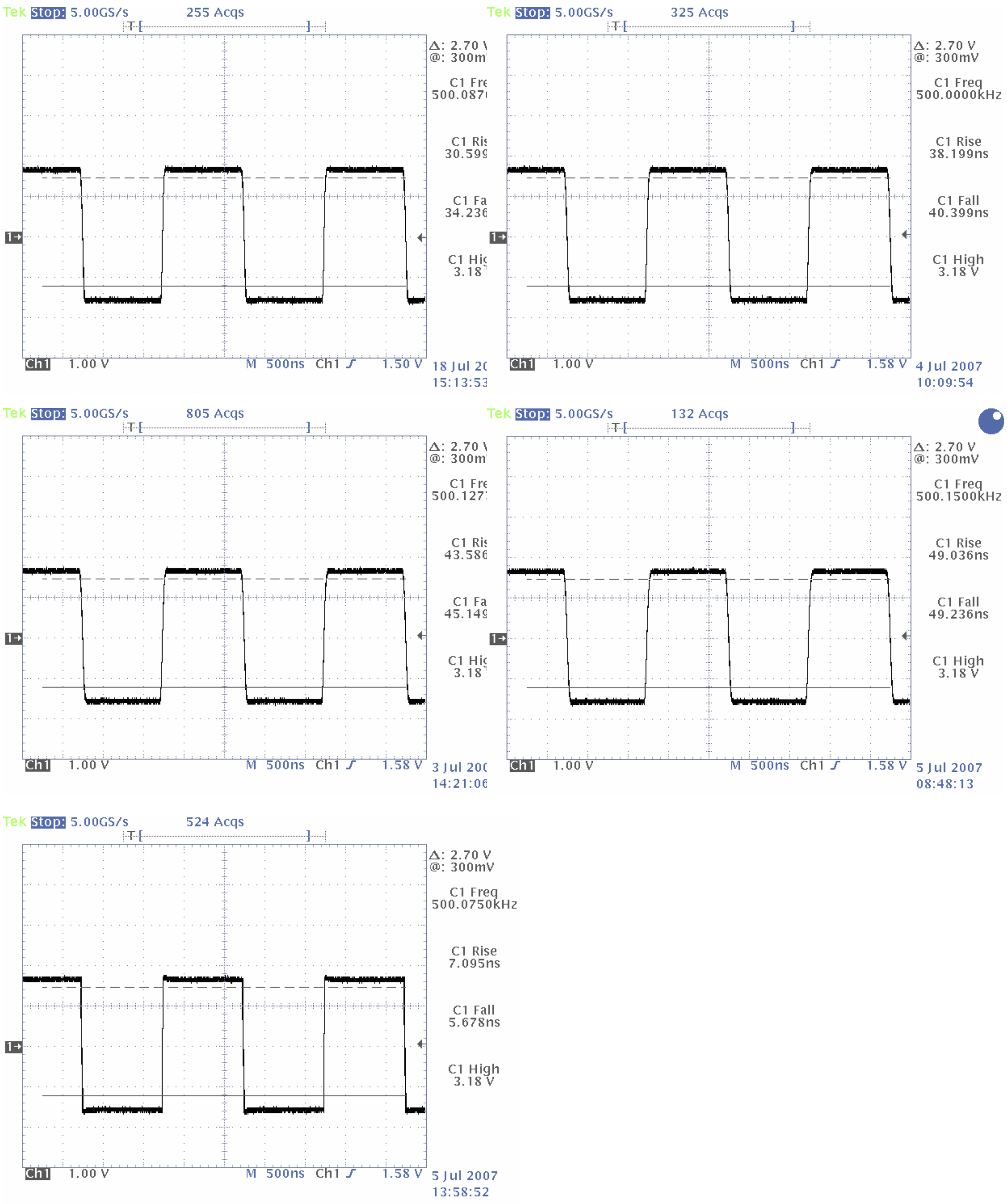

Figure 86: Waveforms EXTCLK 500 kHz "Medium" at 3.3V and at 125°C ambient temperature

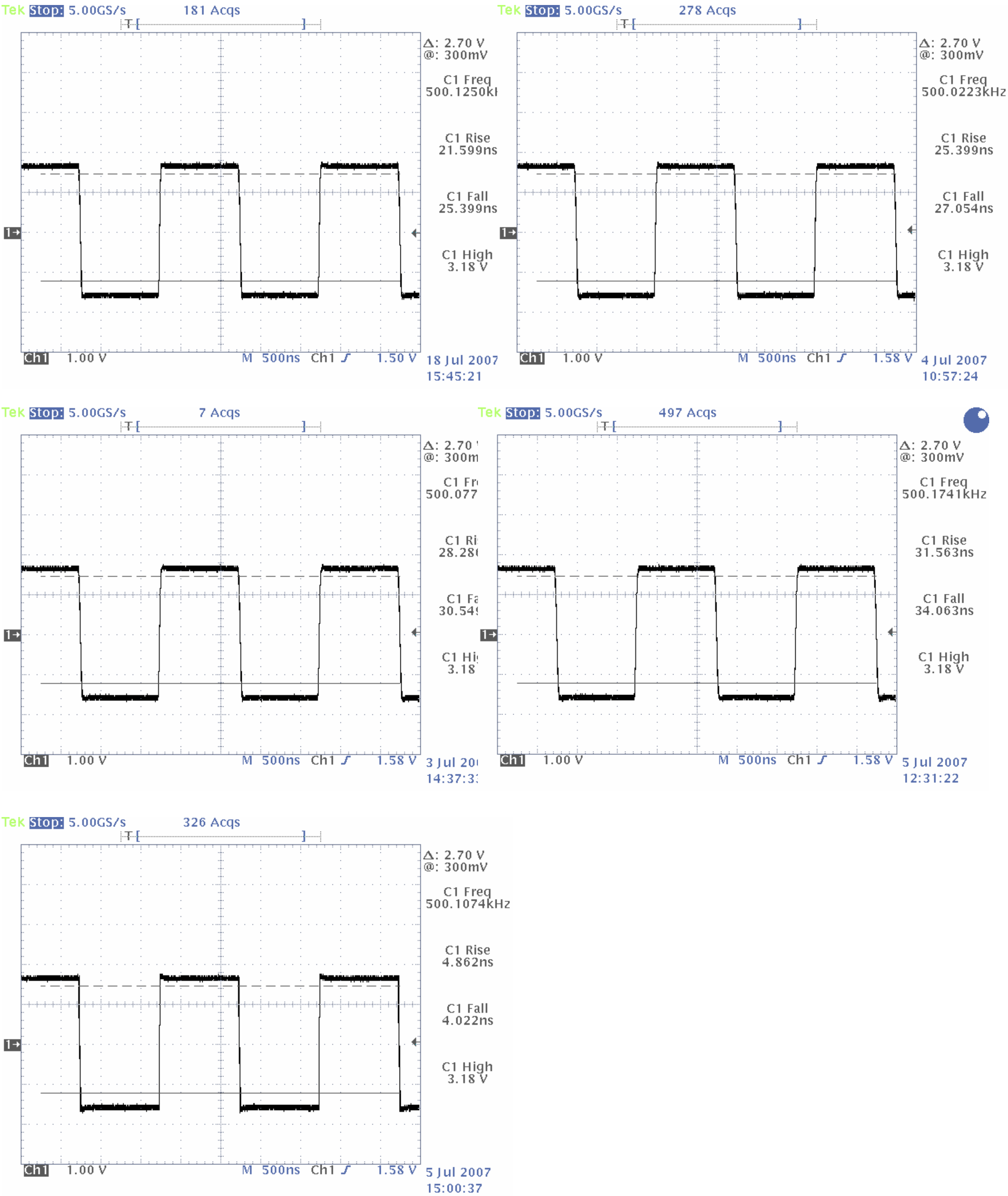

Figure 87: Waveforms EXTCLK 500 kHz "Medium" at 3.3V and at -40°C ambient temperature

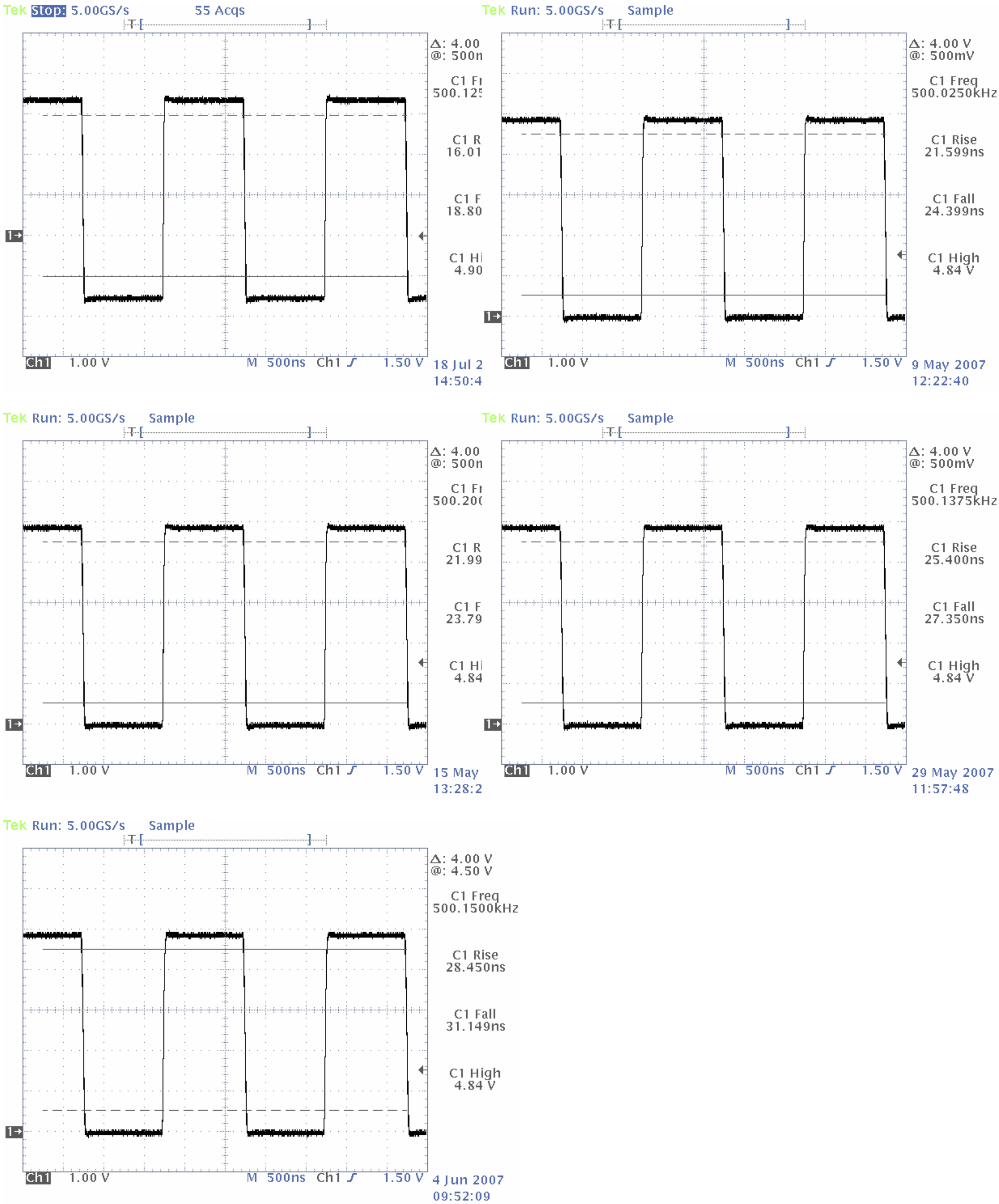

Figure 88: Waveforms EXTCLK 500 kHz “Medium” at 5.0V and at 25°C ambient temperature

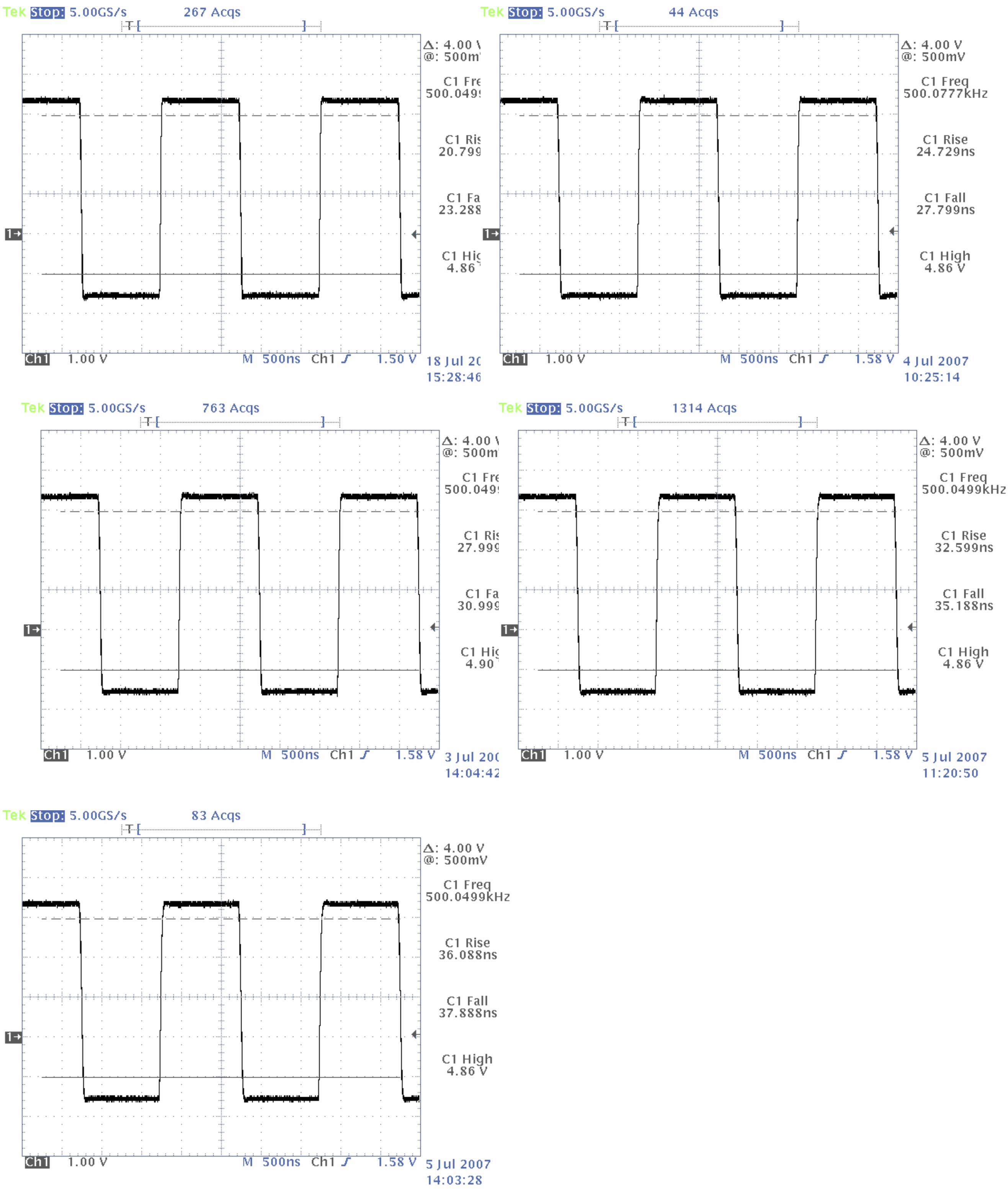

Figure 89: Waveforms EXTCLK 500 kHz "Medium" at 5.0V and at 125°C ambient temperature

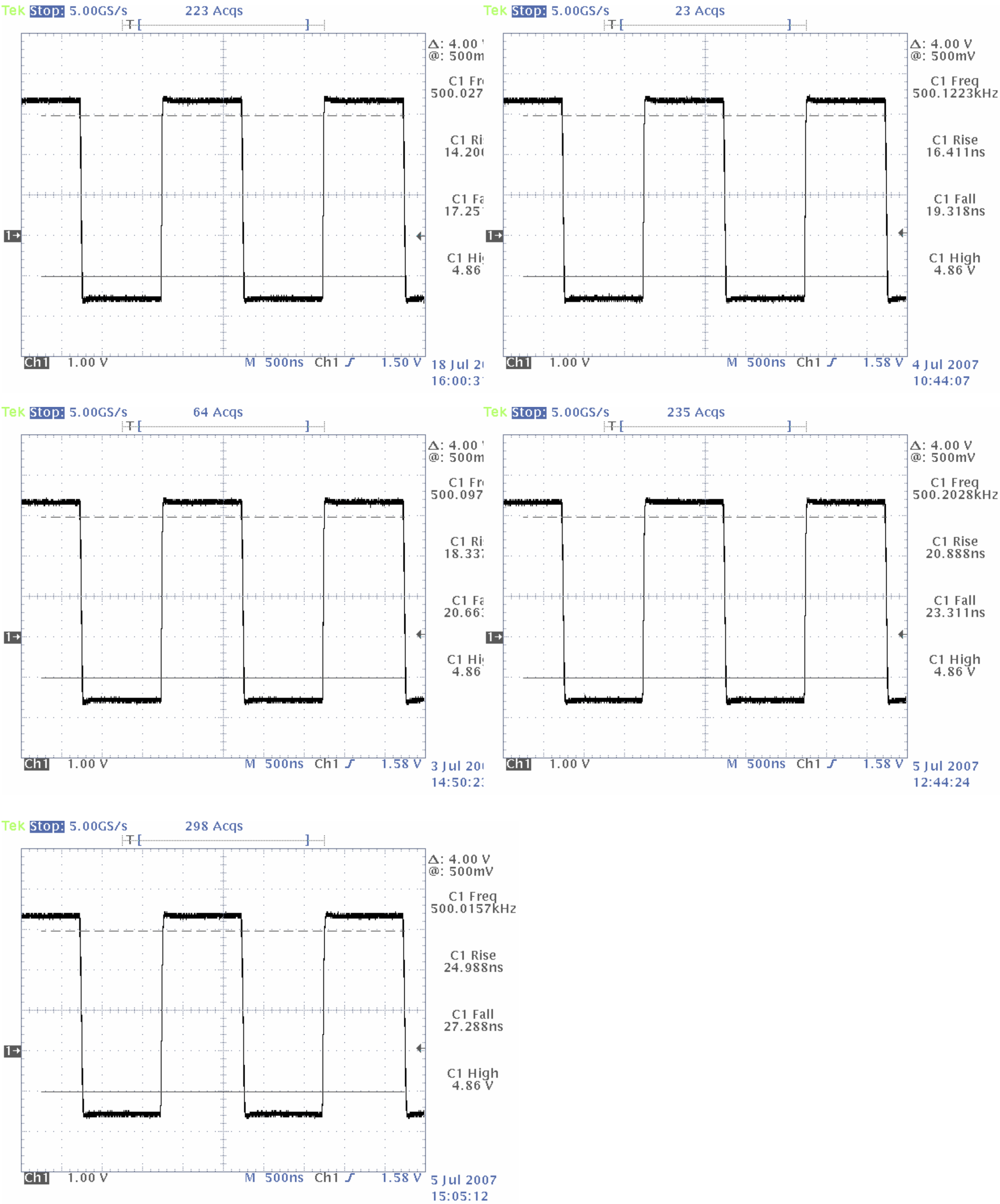

Figure 90: Waveforms EXTCLK 500 kHz “Medium” at 5.0V and at -40°C ambient temperature

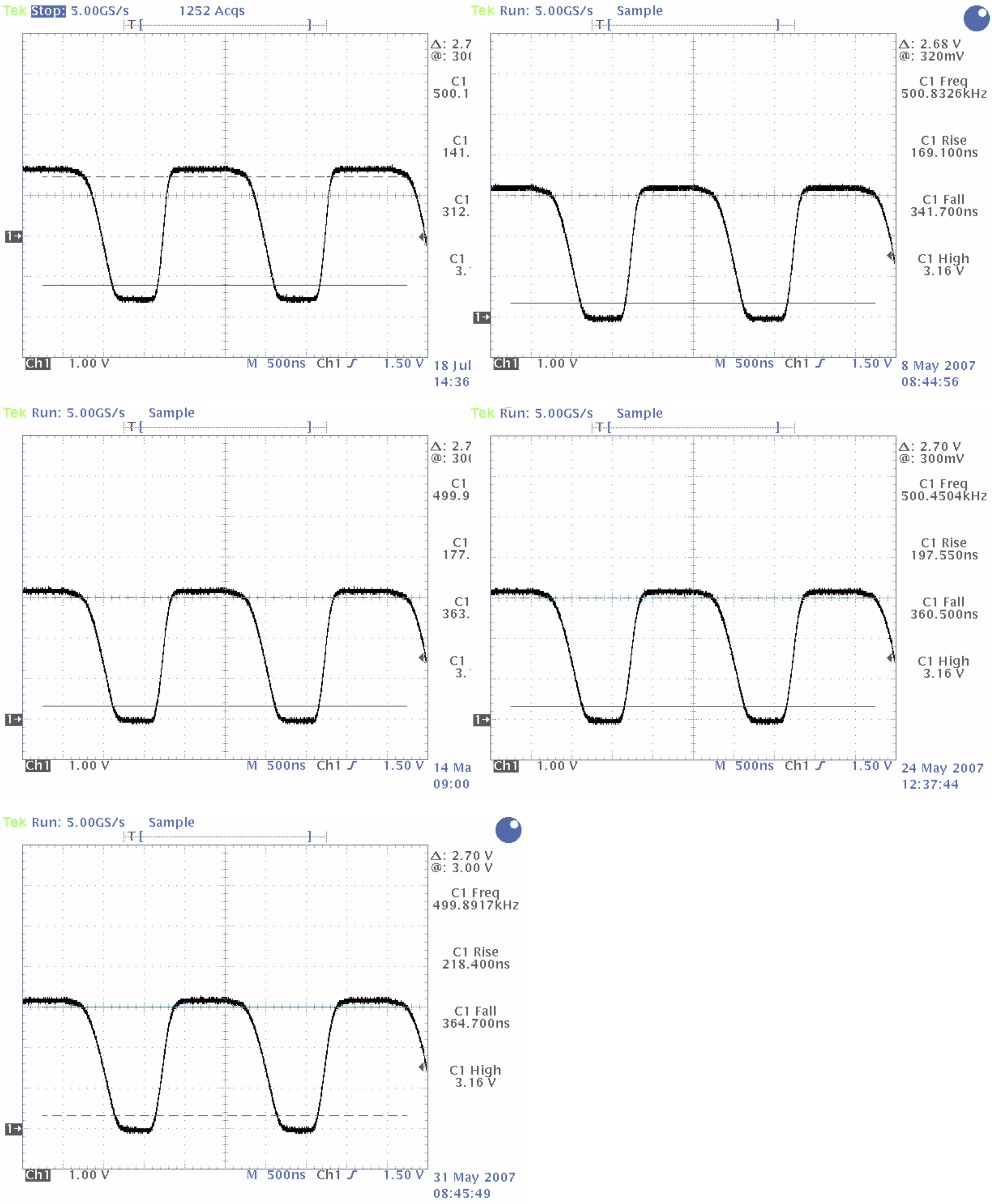

Figure 91: Waveforms EXTCLK 500 kHz "Weak" at 3.3V and at 25°C ambient temperature

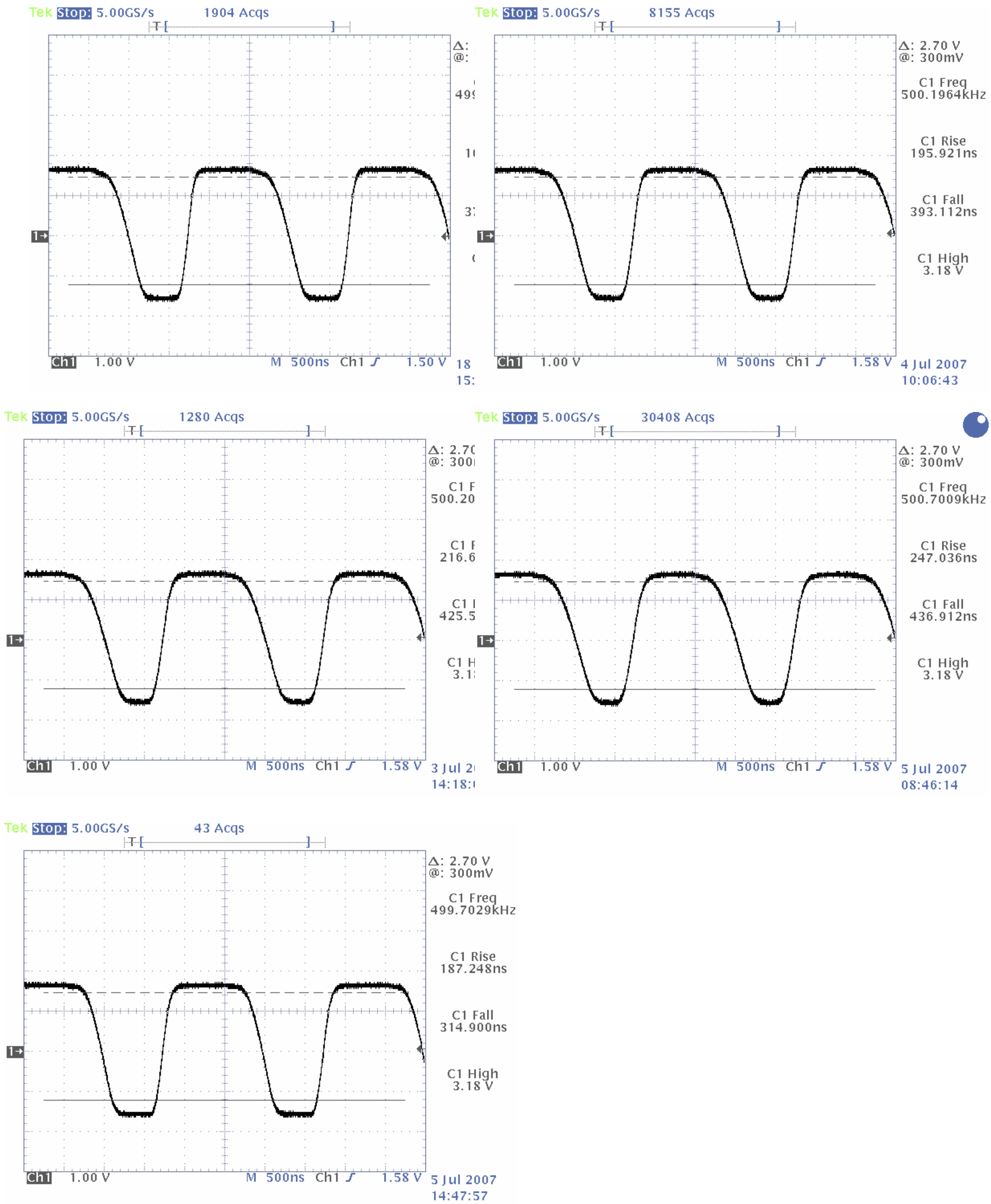

Figure 92: Waveforms EXTCLK 500 kHz “Weak” at 3.3V and at 125°C ambient temperature

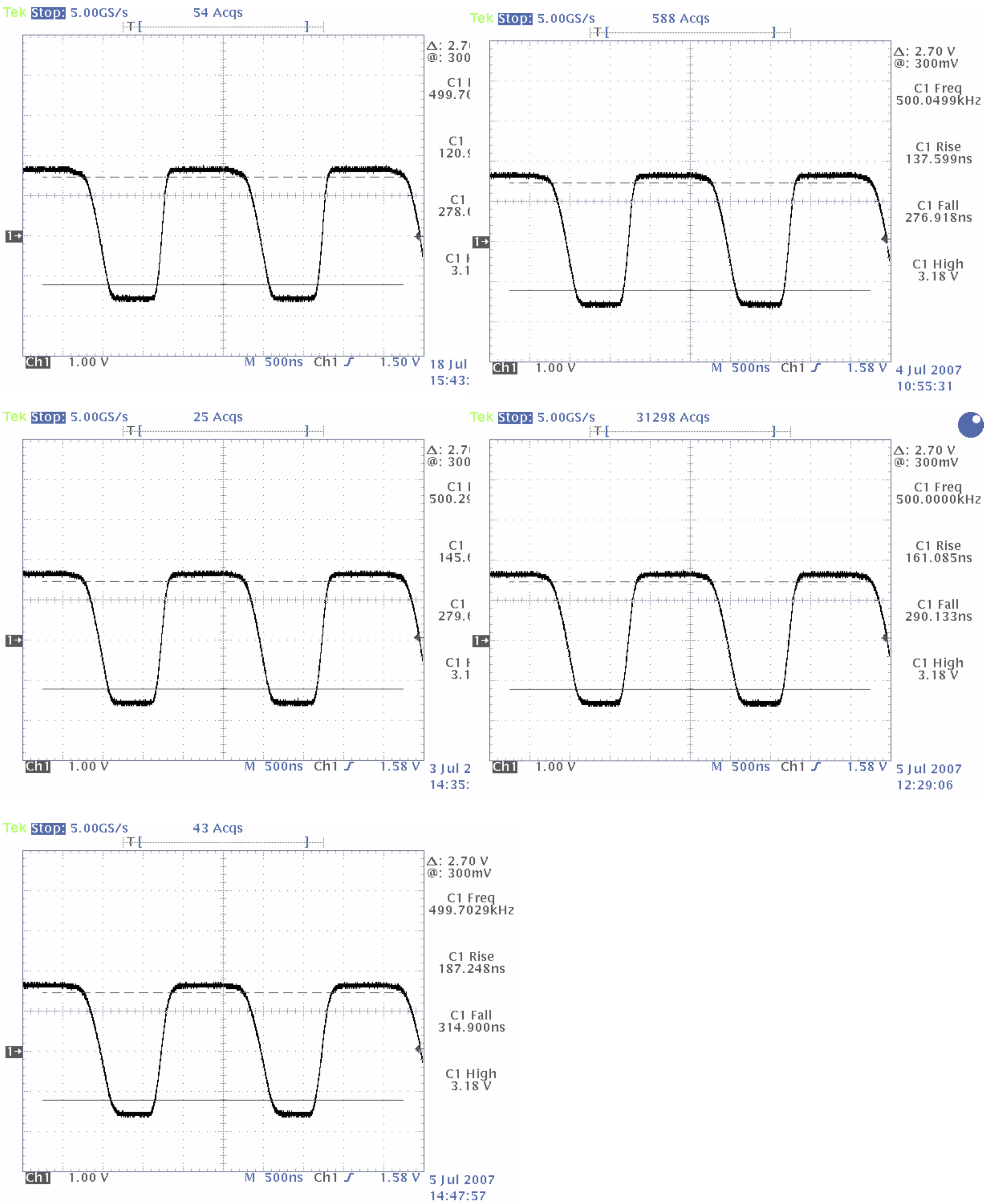

Figure 93: Waveforms EXTCLK 500 kHz "Weak" at 3.3V and at -40°C ambient temperature

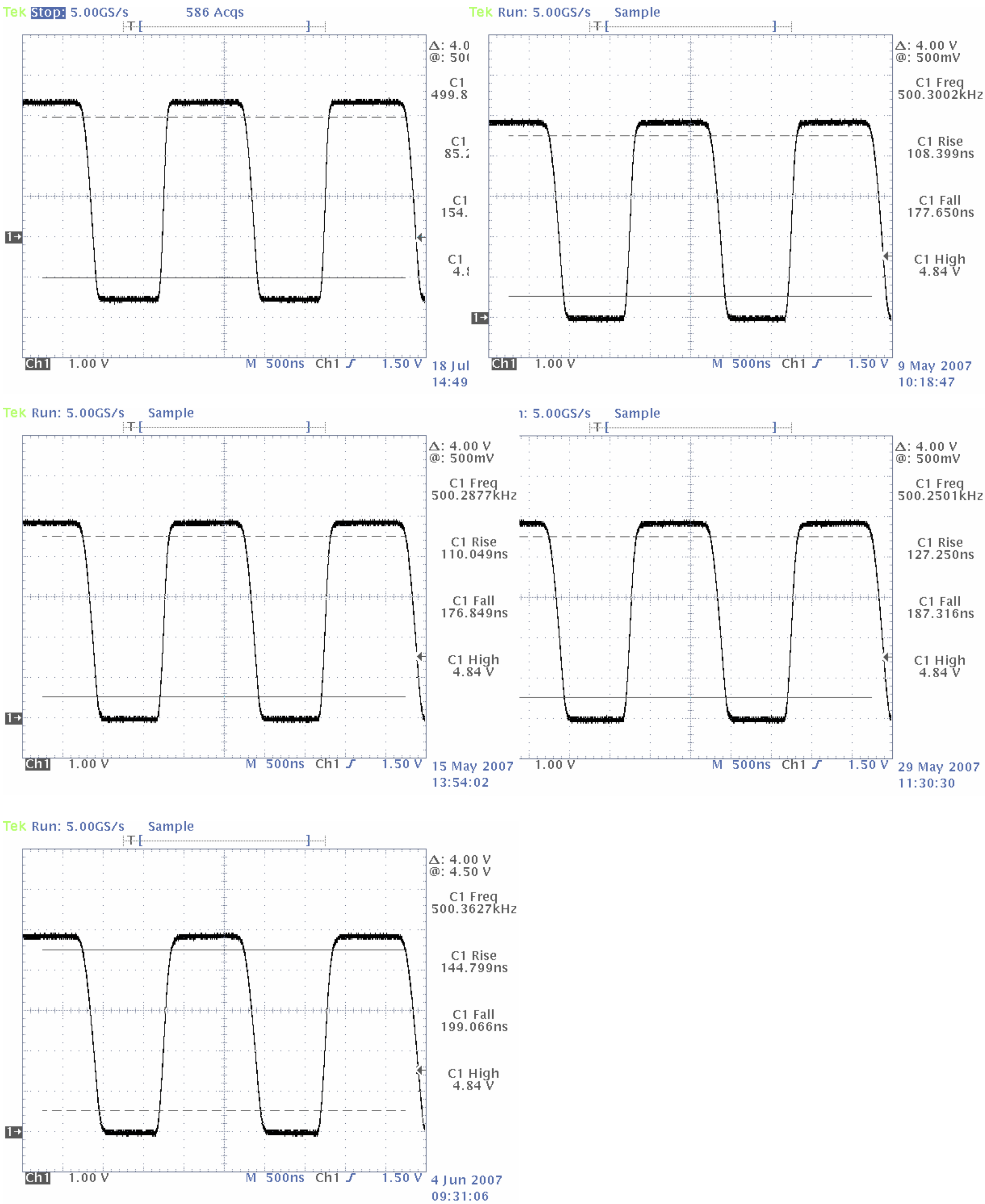

Figure 94: Waveforms EXTCLK 500 kHz "Weak" at 5.0V and at 25°C ambient temperature

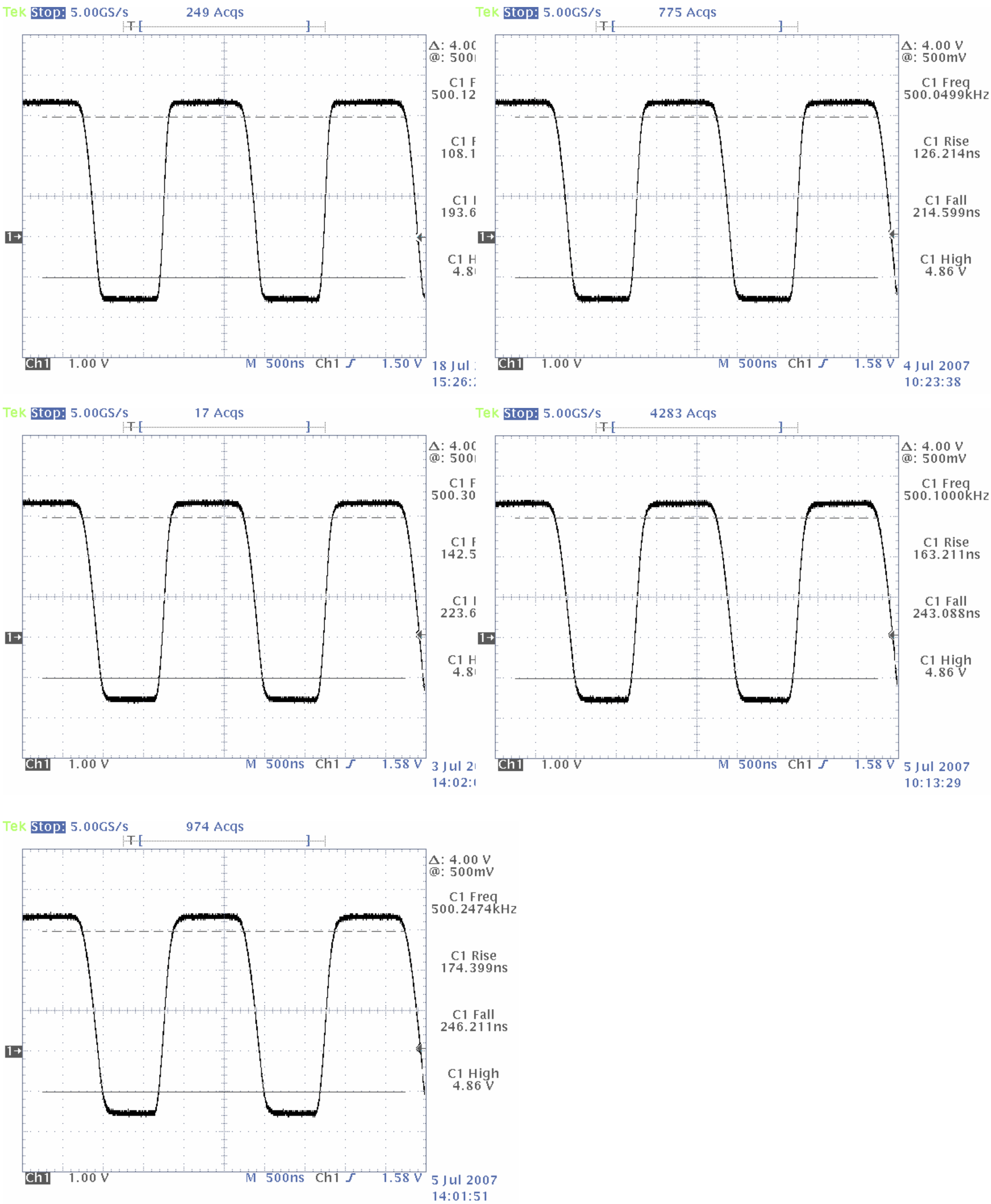

Figure 95: Waveforms EXTCLK 500 kHz "Weak" at 5.0V and at 125°C ambient temperature

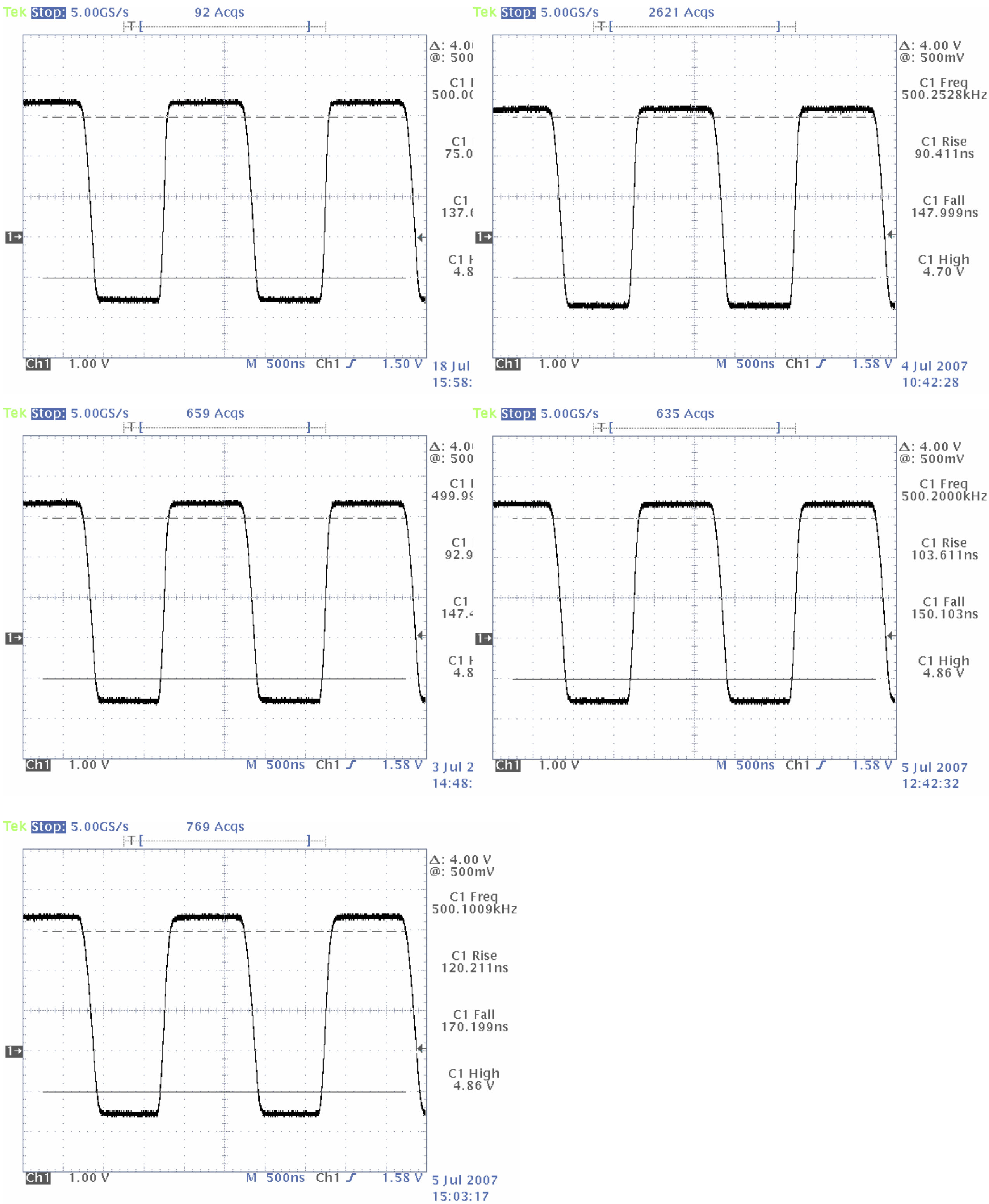

Figure 96: Waveforms EXTCLK 500 kHz “Weak” at 5.0V and at -40°C ambient temperature

Annex B: Measured emission spectra

Emission test result diagrams are provided for selected EXTCLK driver settings and capacitive loads, according Table 12. These results have been discussed in Chapter 5 concerning the benefit of using reduced driver settings and reduced pad supply voltage. This Annex B shows the measured emission spectra for reference puposes.

EXTCLK Driver	Data Rate	Capacitive Load	VDDP Voltage	Test Setup
WEAK	500kHz	10pF	3.3V	Conducted Emission
WEAK	500kHz	10pF	3.3V	Radiated Emission
WEAK	500kHz	10pF	5.0V	Conducted Emission
WEAK	500kHz	10pF	5.0V	Radiated Emission
MEDIUM	2MHz	10pF	3.3V	Conducted Emission
MEDIUM	2MHz	10pF	3.3V	Radiated Emission
MEDIUM	2MHz	10pF	5.0V	Conducted Emission
MEDIUM	2MHz	10pF	5.0V	Radiated Emission
STRONG-SOFT	10MHz	10pF	3.3V	Conducted Emission
STRONG-SOFT	10MHz	10pF	3.3V	Radiated Emission
STRONG-SOFT	10MHz	10pF	5.0V	Conducted Emission
STRONG-SOFT	10MHz	10pF	5.0V	Radiated Emission
STRONG-MEDIUM	10MHz	10pF	3.3V	Conducted Emission
STRONG-MEDIUM	10MHz	10pF	3.3V	Radiated Emission
STRONG-MEDIUM	20MHz	10pF	5.0V	Conducted Emission
STRONG-MEDIUM	20MHz	10pF	5.0V	Radiated Emission
STRONG-SHARP	20MHz	10pF	3.3V	Conducted Emission
STRONG-SHARP	20MHz	10pF	3.3V	Radiated Emission
STRONG-SHARP	40MHz	10pF	5.0V	Conducted Emission
STRONG-SHARP	40MHz	10pF	5.0V	Radiated Emission
EXTRA-STRONG	40MHz	10pF	3.3V	Conducted Emission
EXTRA-STRONG	40MHz	10pF	3.3V	Radiated Emission
EXTRA-STRONG	66MHz	10pF	5.0V	Conducted Emission
EXTRA-STRONG	66MHz	10pF	5.0V	Radiated Emission
WEAK	500kHz	47pF	3.3V	Conducted Emission
WEAK	500kHz	47pF	3.3V	Radiated Emission
WEAK	500kHz	47pF	5.0V	Conducted Emission
WEAK	500kHz	47pF	5.0V	Radiated Emission
MEDIUM	2MHz	47pF	3.3V	Conducted Emission
MEDIUM	2MHz	47pF	3.3V	Radiated Emission
MEDIUM	2MHz	47pF	5.0V	Conducted Emission
MEDIUM	2MHz	47pF	5.0V	Radiated Emission
STRONG-SOFT	10MHz	47pF	3.3V	Conducted Emission
STRONG-SOFT	10MHz	47pF	3.3V	Radiated Emission

STRONG-SOFT	10MHz	47pF	5.0V	Conducted Emission
STRONG-SOFT	10MHz	47pF	5.0V	Radiated Emission
STRONG-MEDIUM	10MHz	47pF	3.3V	Conducted Emission
STRONG-MEDIUM	10MHz	47pF	3.3V	Radiated Emission
STRONG-MEDIUM	20MHz	47pF	5.0V	Conducted Emission
STRONG-MEDIUM	20MHz	47pF	5.0V	Radiated Emission
STRONG-SHARP	20MHz	47pF	3.3V	Conducted Emission
STRONG-SHARP	20MHz	47pF	3.3V	Radiated Emission
STRONG-SHARP	40MHz	47pF	5.0V	Conducted Emission
STRONG-SHARP	40MHz	47pF	5.0V	Radiated Emission
EXTRA-STRONG	40MHz	47pF	3.3V	Conducted Emission
EXTRA-STRONG	40MHz	47pF	3.3V	Radiated Emission
EXTRA-STRONG	66MHz	47pF	5.0V	Conducted Emission
EXTRA-STRONG	66MHz	47pF	5.0V	Radiated Emission

Table 12: List of emission measurements

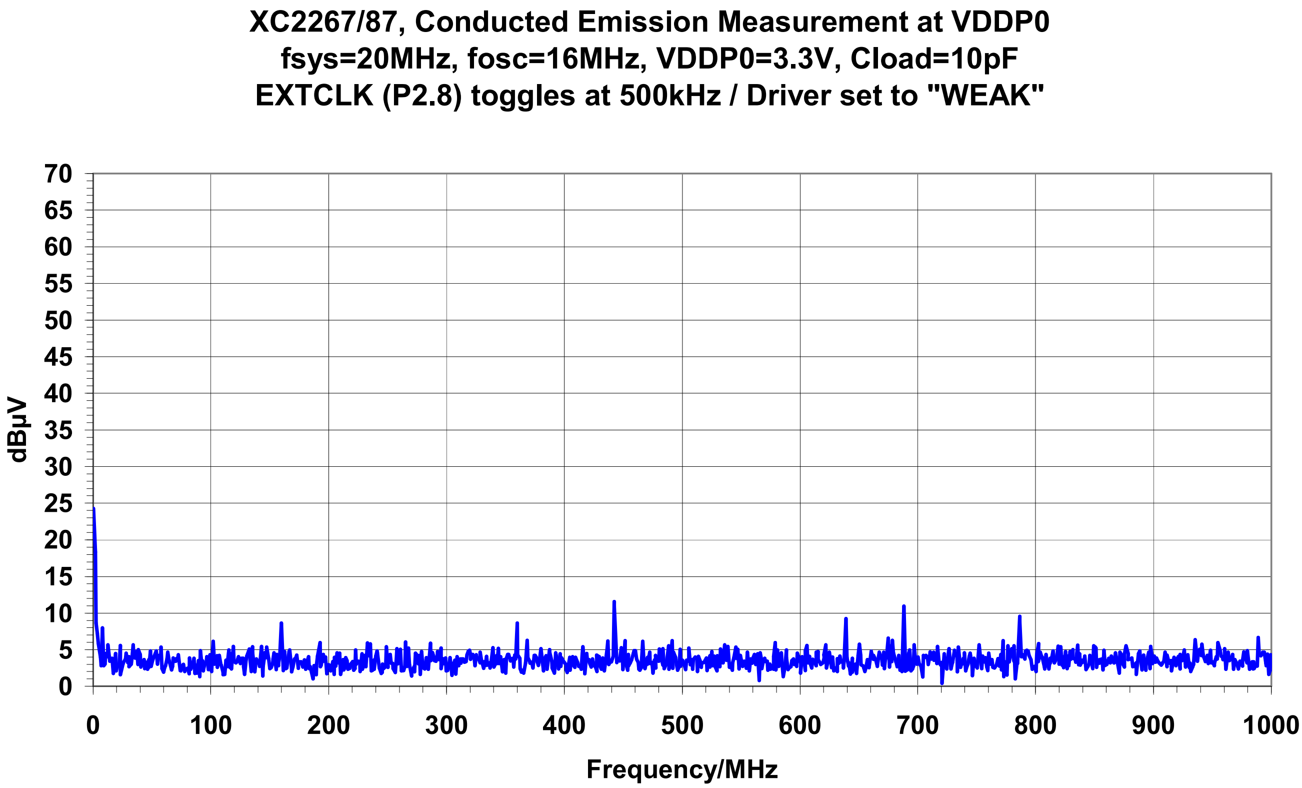

Figure 97: Emission Spectrum for WEAK/500kHz/10pF/3.3V/Conducted

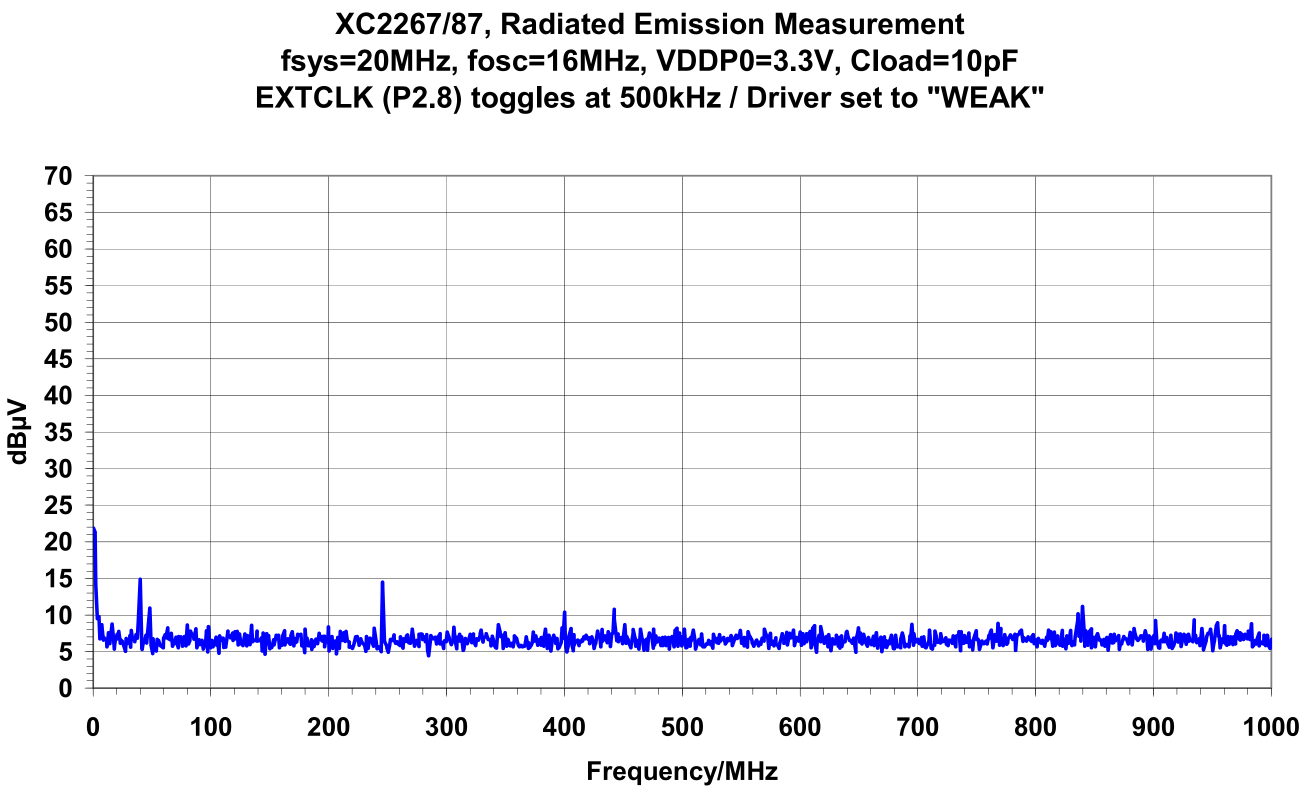

Figure 98: Emission Spectrum for WEAK/500kHz/10pF/3.3V/Radiated

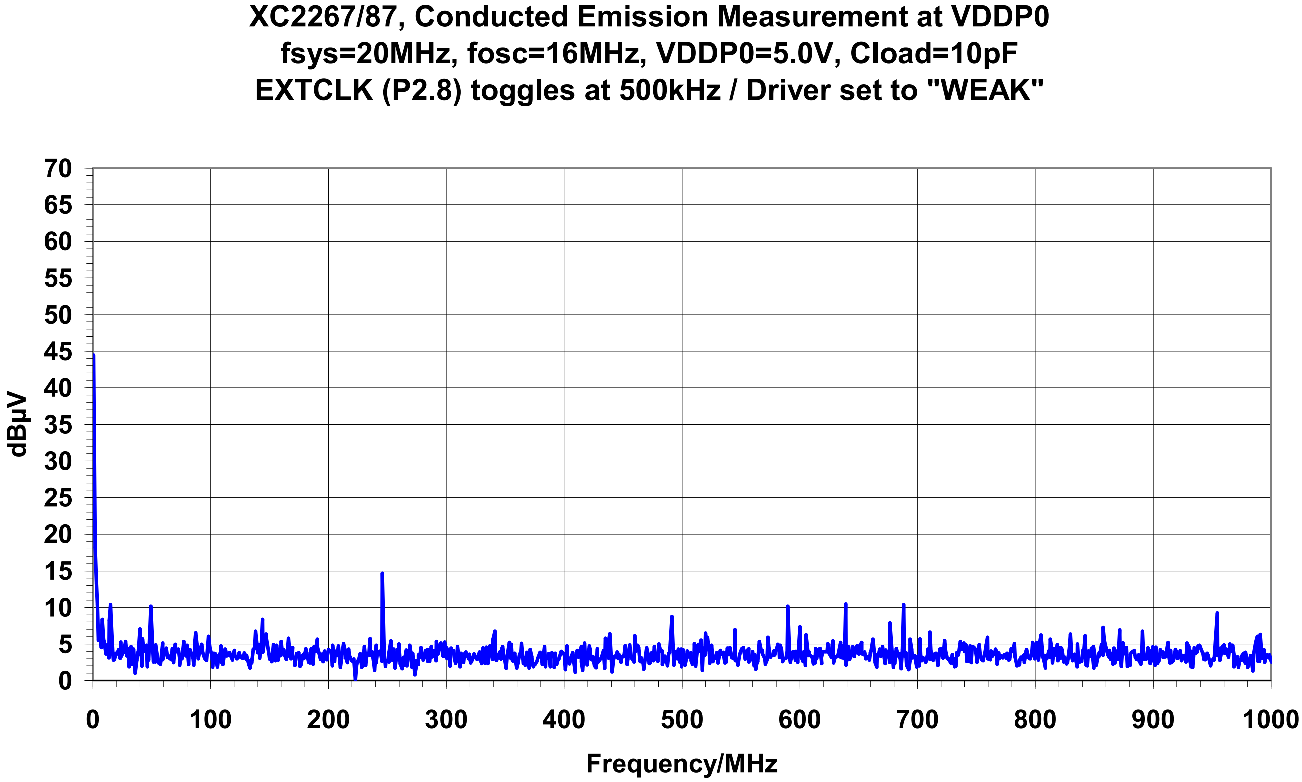

Figure 99: Emission Spectrum for WEAK/500kHz/10pF/5.0V/Conducted

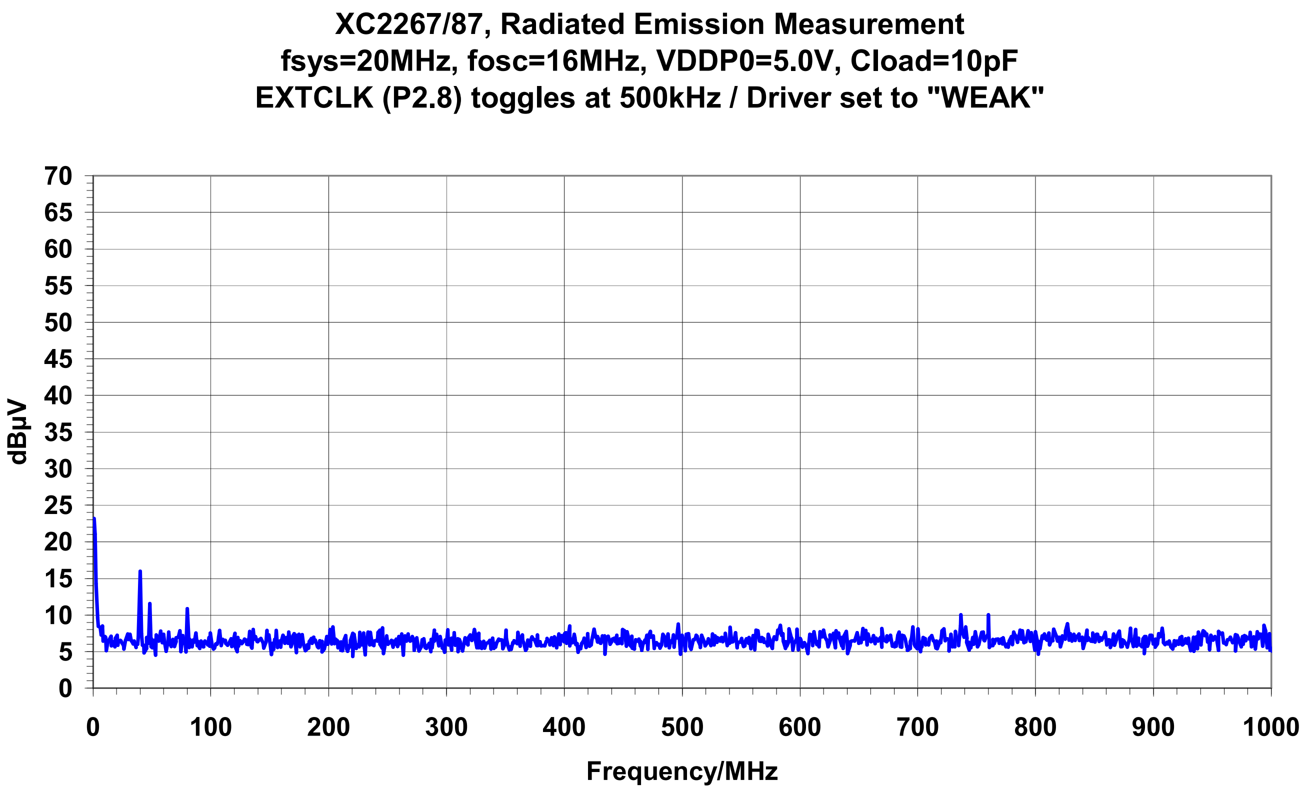

Figure 100: Emission Spectrum for WEAK/500kHz/10pF/5.0V/Radiated

XC2267/87, Conducted Emission Measurement at VDDP0
fsys=20MHz, fosc=16MHz, VDDP0=3.3V, Cload=10pF
EXTCLK (P2.8) toggles at 2MHz / Driver set to "MEDIUM"

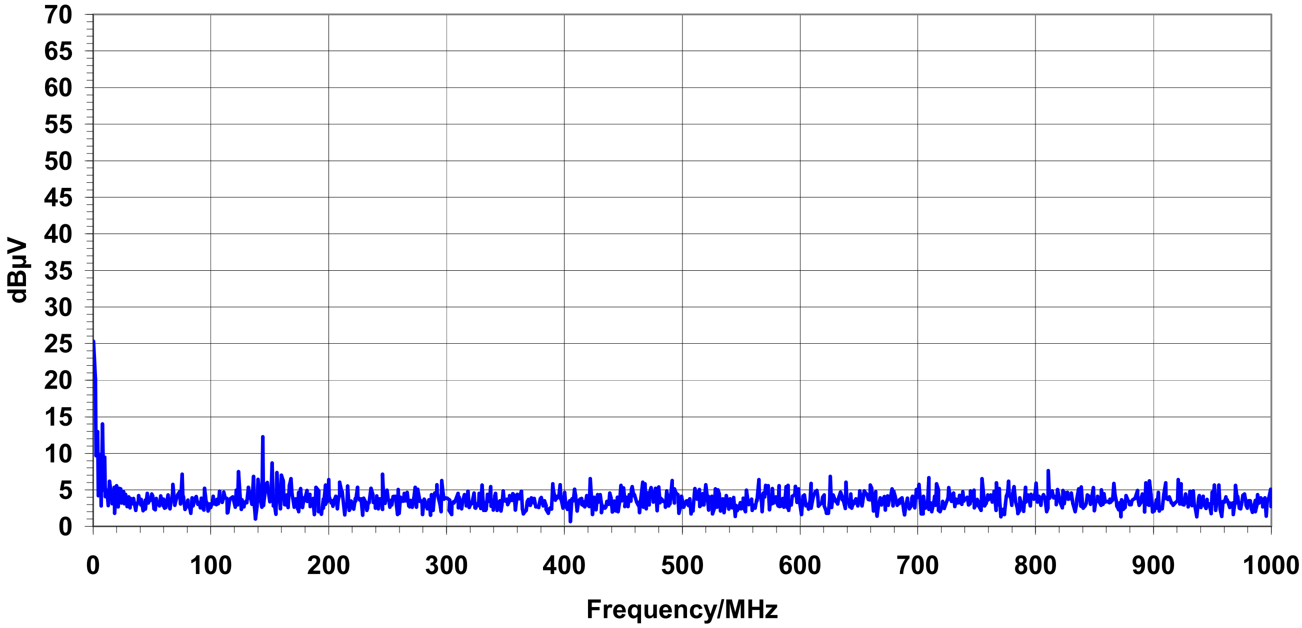

Figure 101: Emission Spectrum for MEDIUM/2MHz/10pF/3.3V/Conducted

XC2267/87, Radiated Emission Measurement
fsys=20MHz, fosc=16MHz, VDDP0=3.3V, Cload=10pF
EXTCLK (P2.8) toggles at 2MHz / Driver set to "MEDIUM"

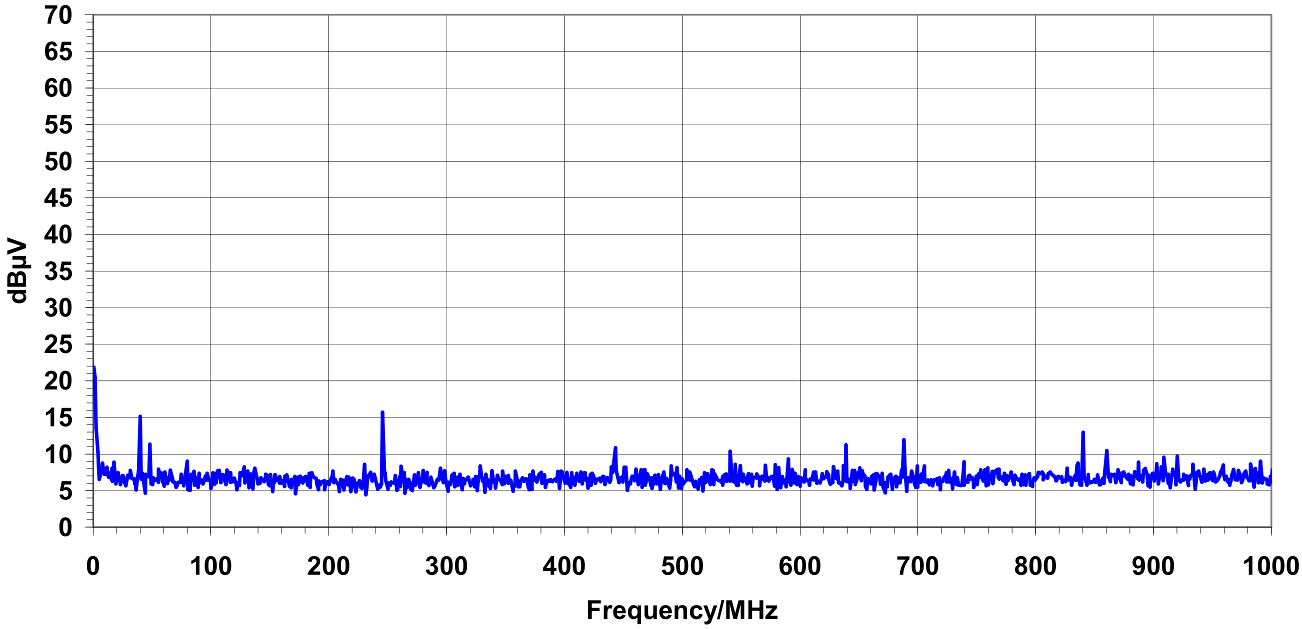

Figure 102: Emission Spectrum for MEDIUM/2MHz/10pF/3.3V/Radiated

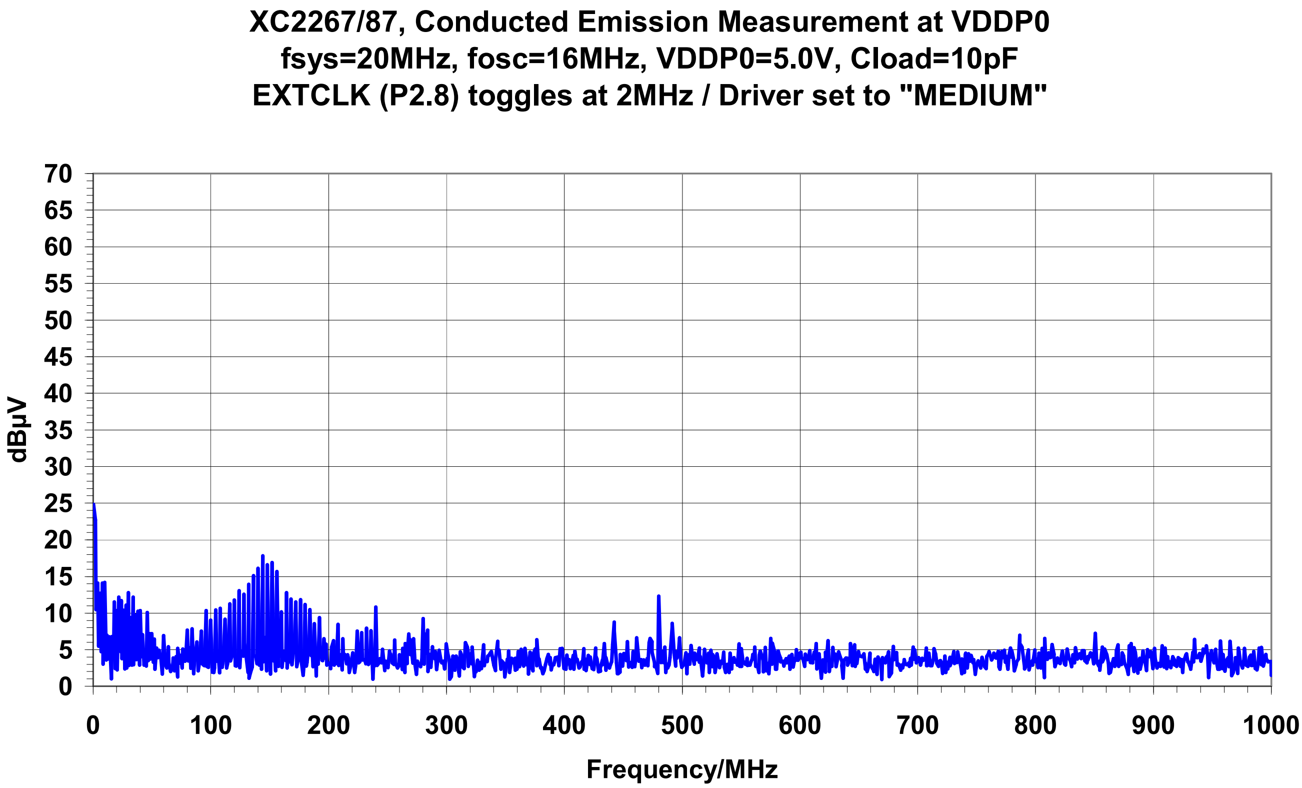

Figure 103: Emission Spectrum for MEDIUM/2MHz/10pF/5.0V/Conducted

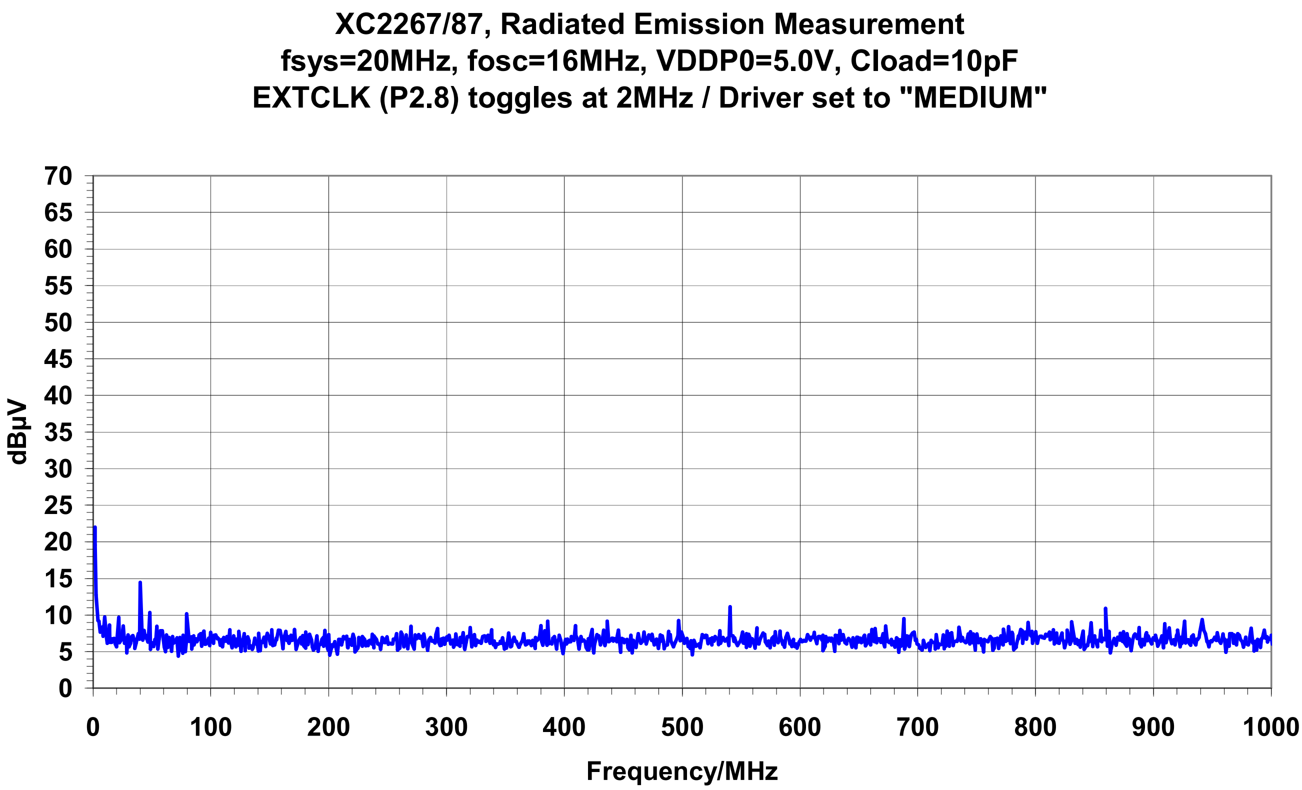

Figure 104: Emission Spectrum for MEDIUM/2MHz/10pF/5.0V/Radiated

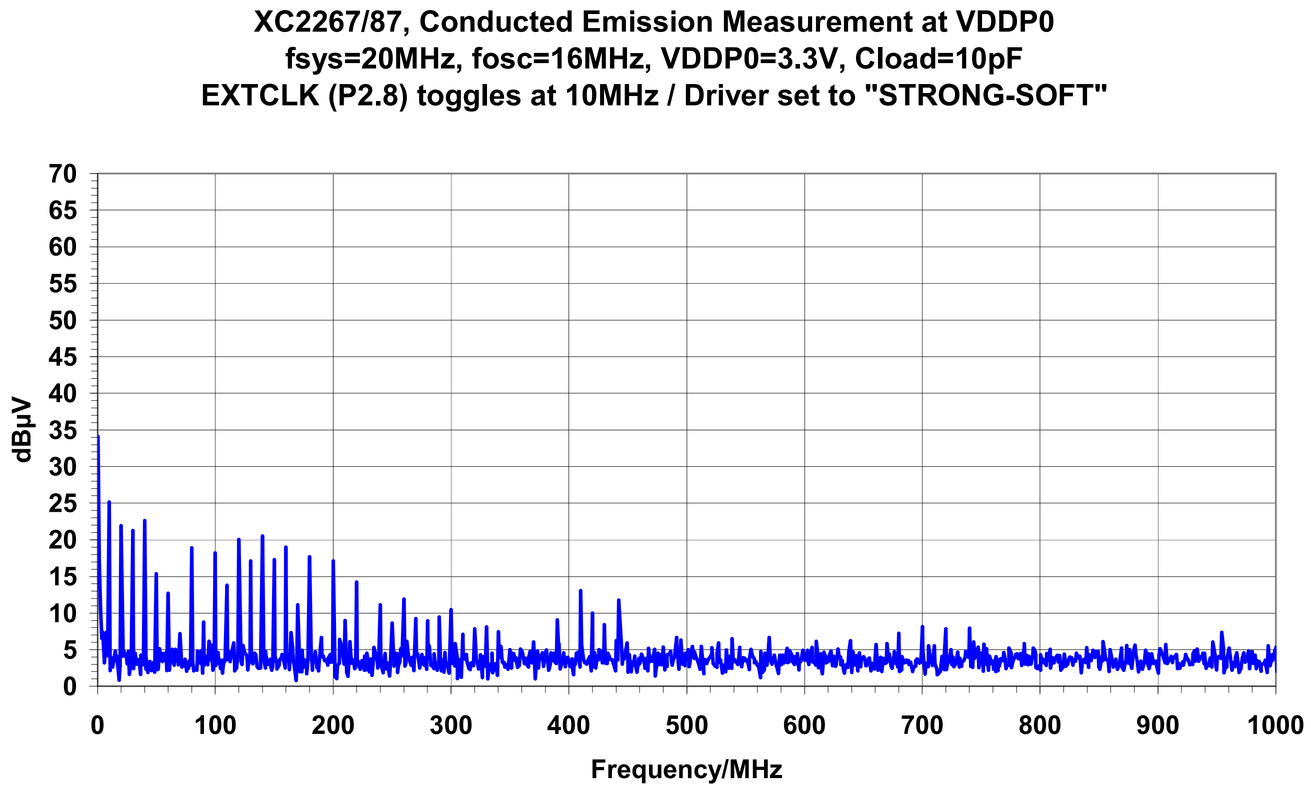

Figure 105: Emission Spectrum for STRONG-SOFT/20MHz/10pF/3.3V/Conducted

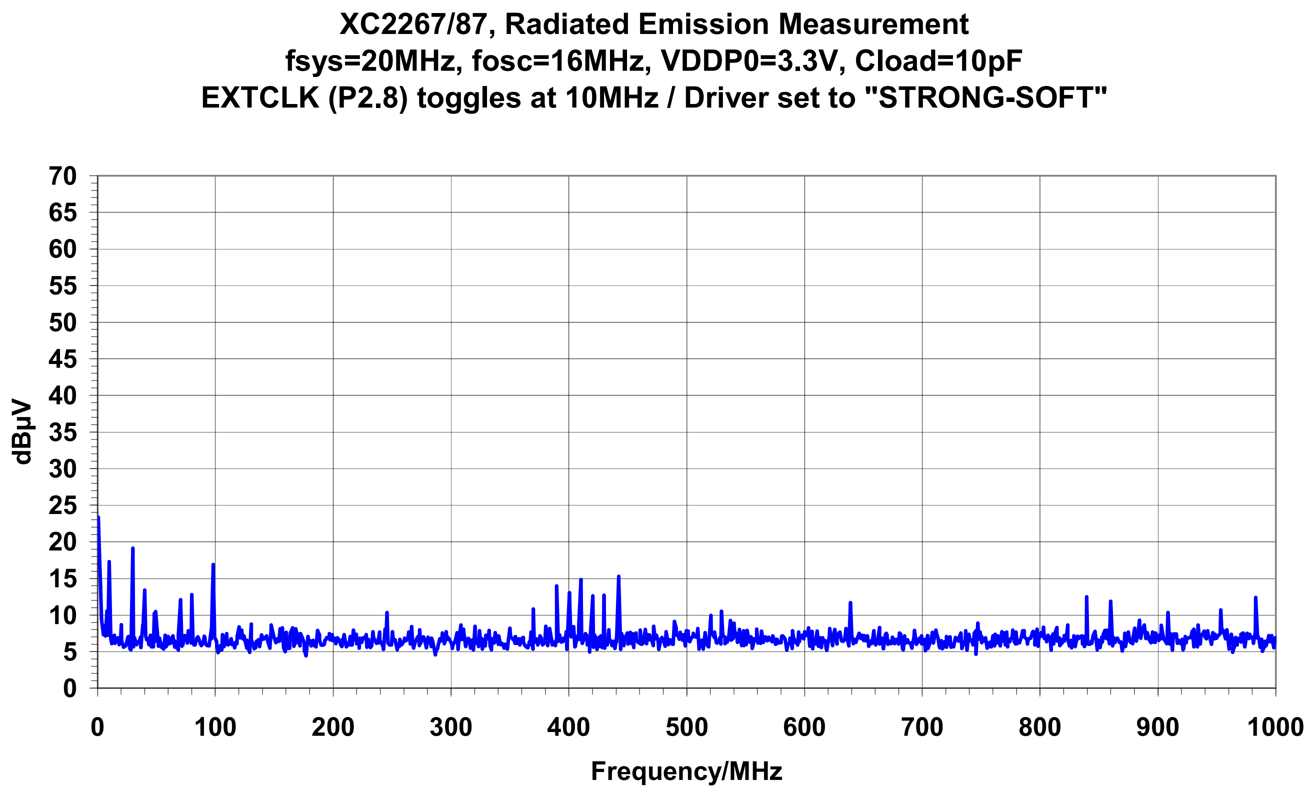

Figure 106: Emission Spectrum for STRONG-SOFT/20MHz/10pF/3.3V/Radiated

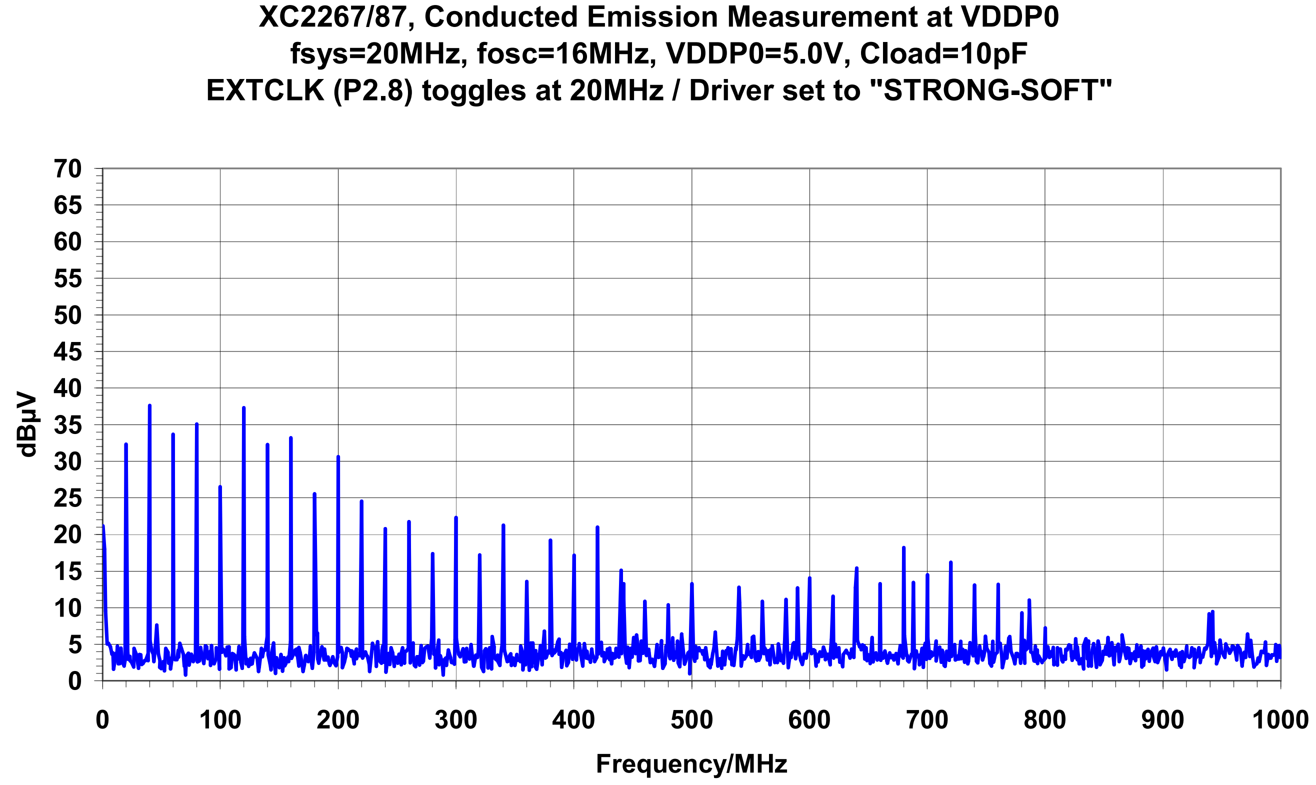

Figure 107: Emission Spectrum for STRONG-SOFT/20MHz/10pF/5.0V/Conducted

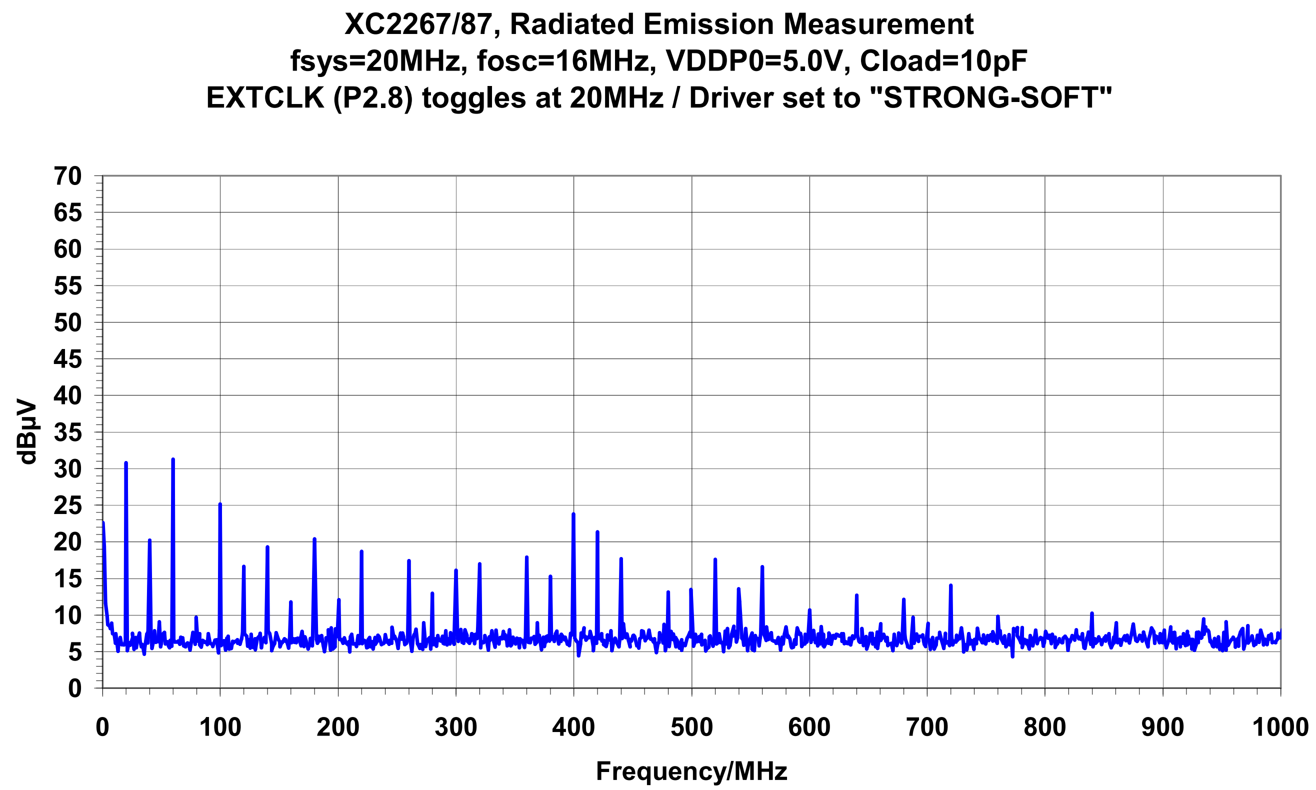

Figure 108: Emission Spectrum for STRONG-SOFT/20MHz/10pF/5.0V/Radiated

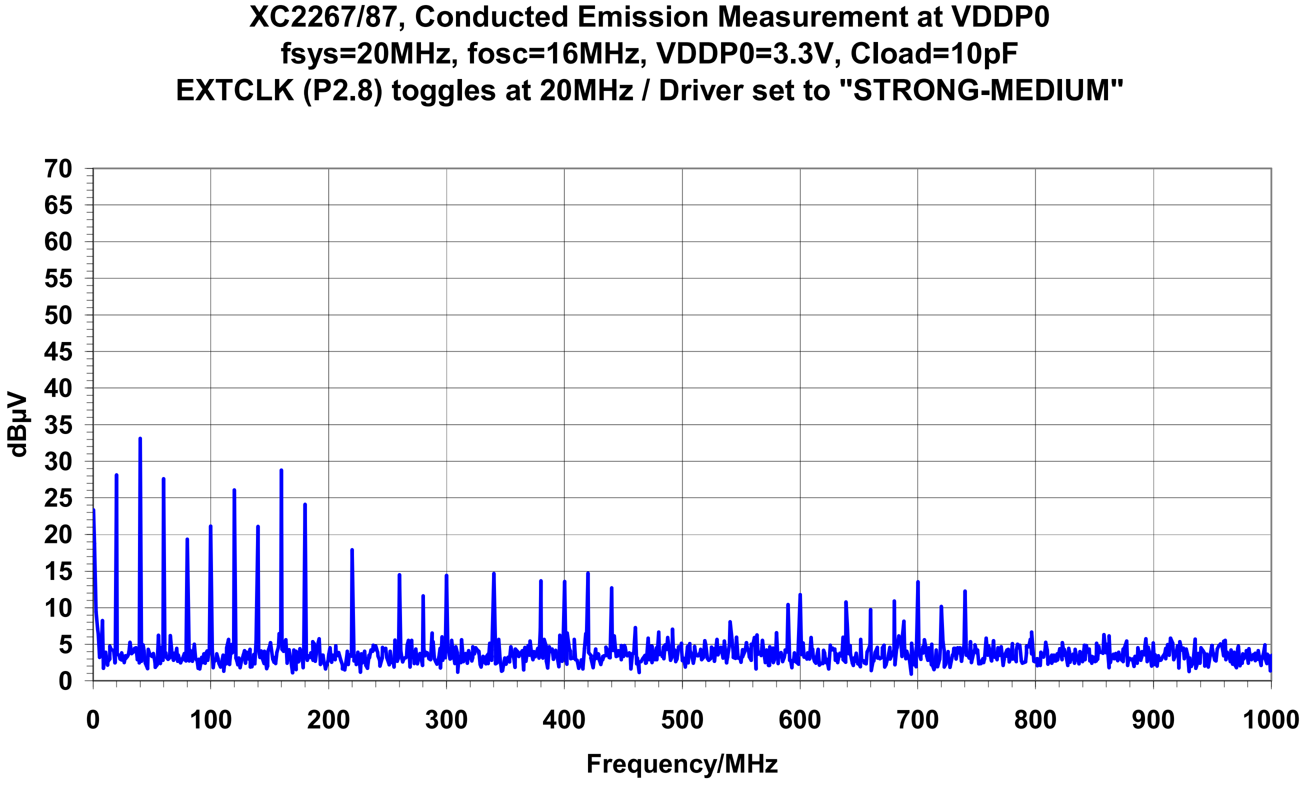

Figure 109: Emission Spectrum for STRONG-MEDIUM/20MHz/10pF/3.3V/Conducted

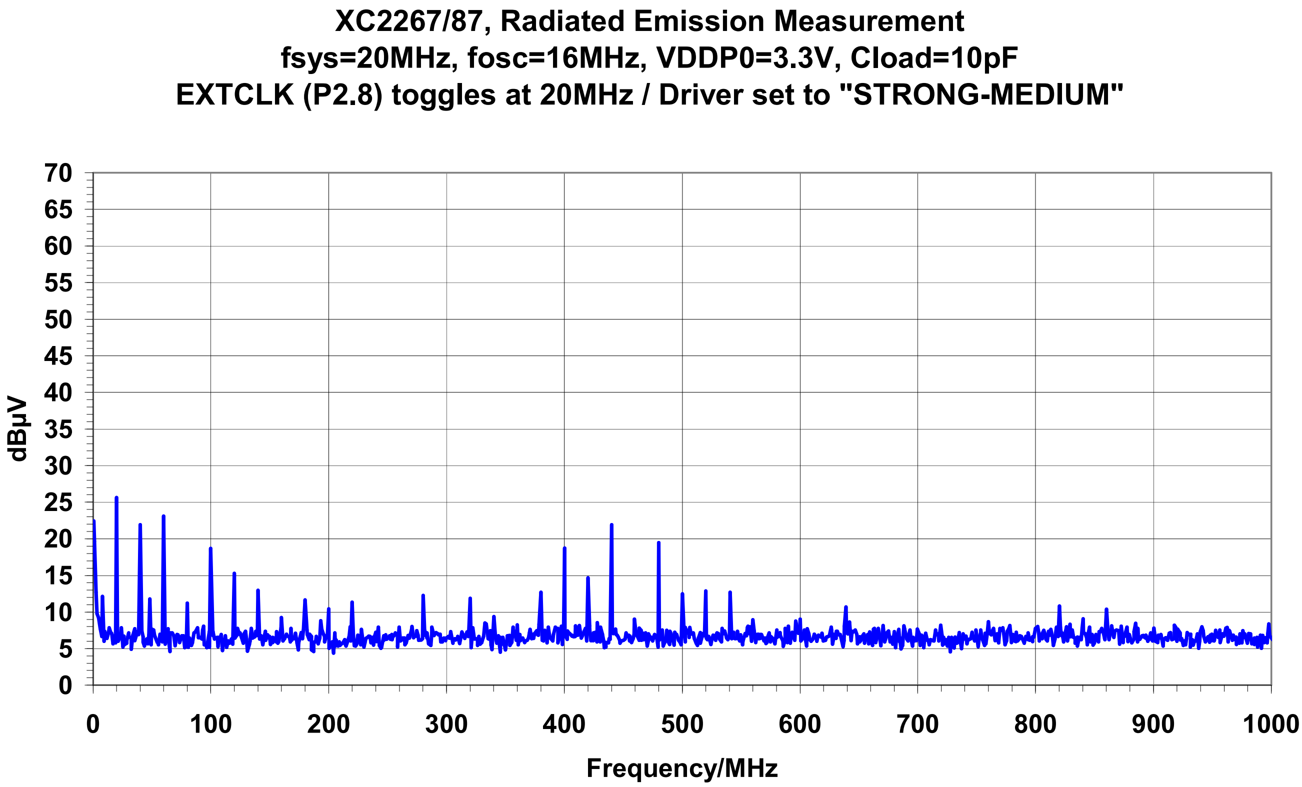

Figure 110: Emission Spectrum for STRONG-MEDIUM/20MHz/10pF/3.3V/Radiated

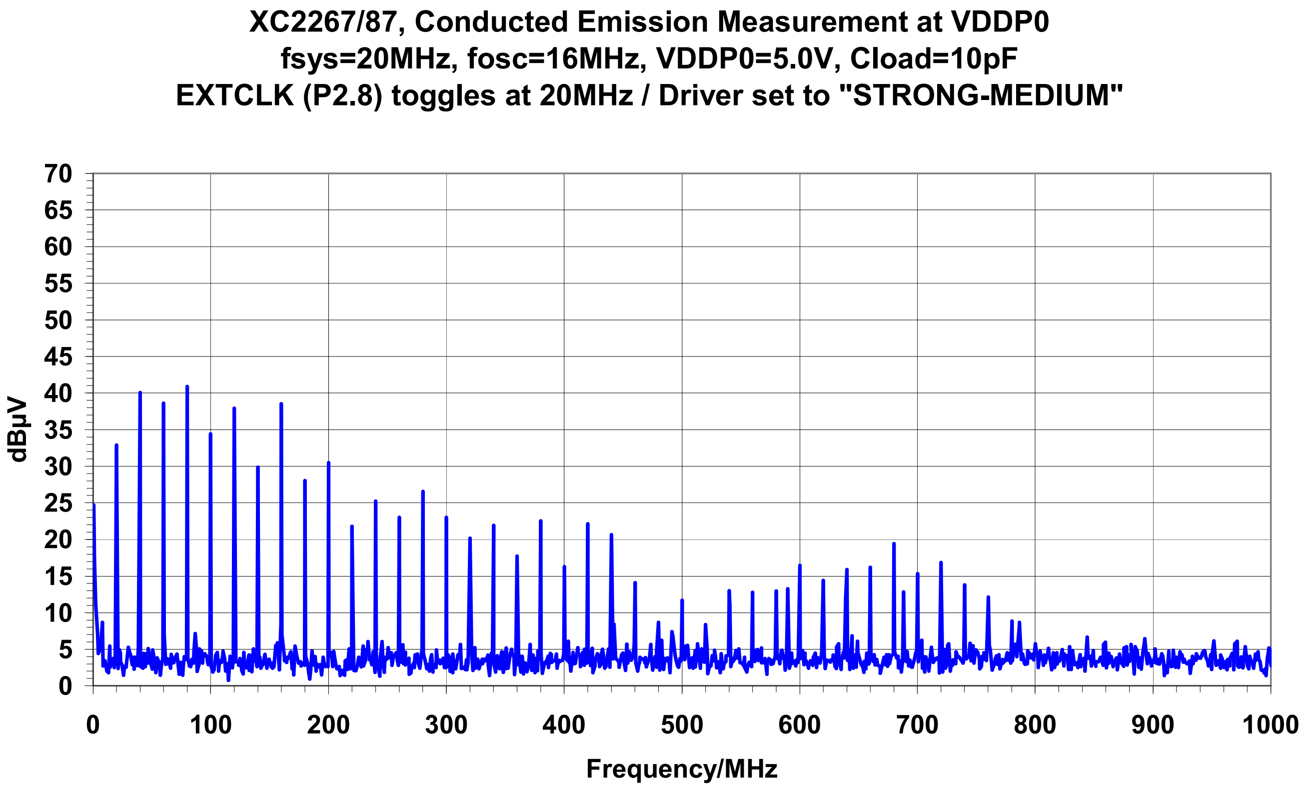

Figure 111: Emission Spectrum for STRONG-MEDIUM/20MHz/10pF/5.0V/Conducted

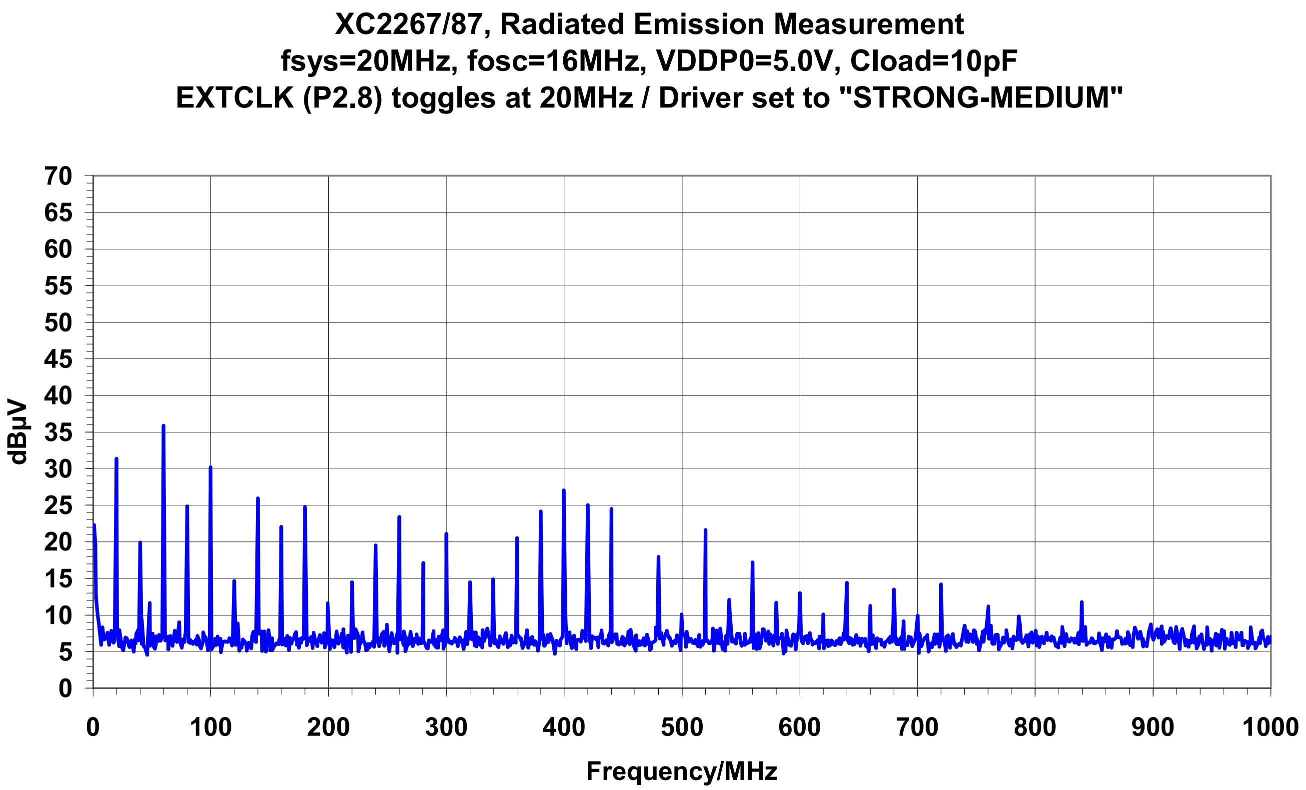

Figure 112: Emission Spectrum for STRONG-MEDIUM/20MHz/10pF/5.0V/Radiated

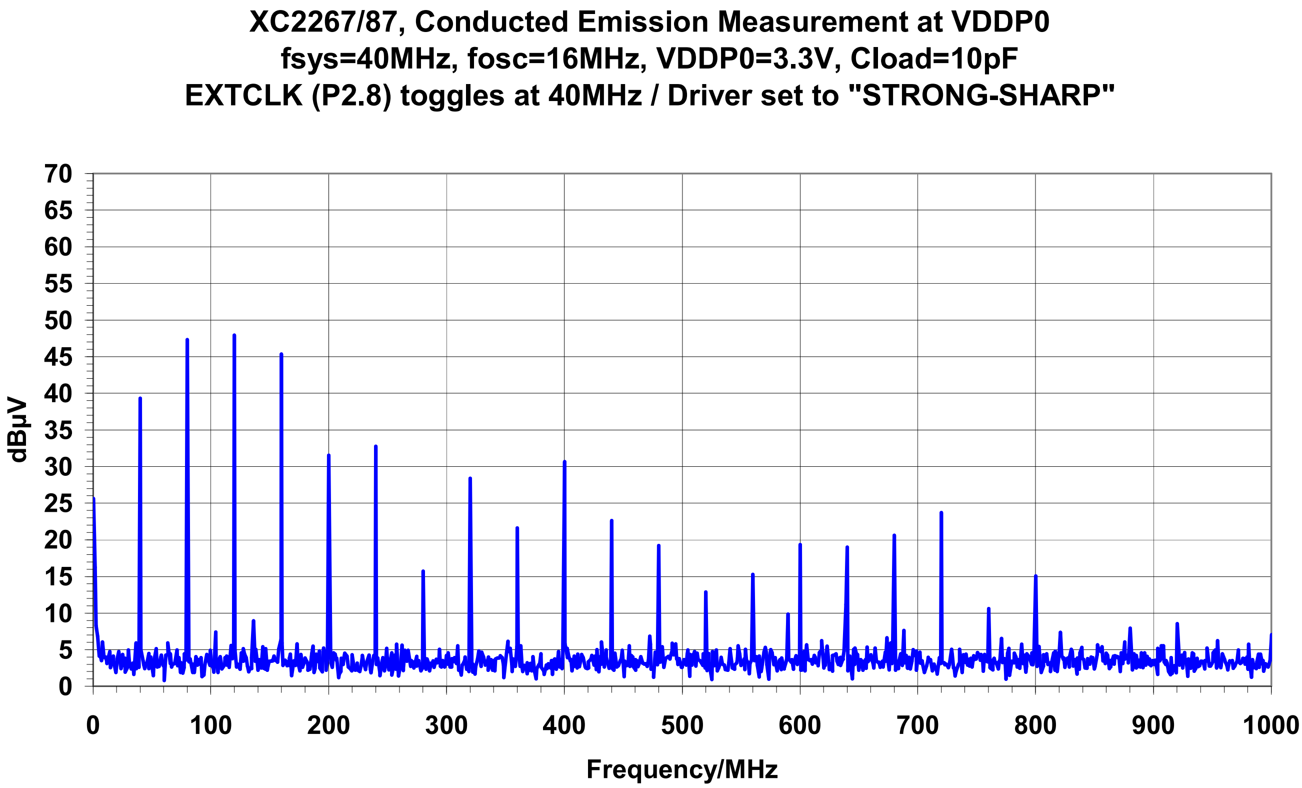

Figure 113: Emission Spectrum for STRONG-SHARP/40MHz/10pF/3.3V/Conducted

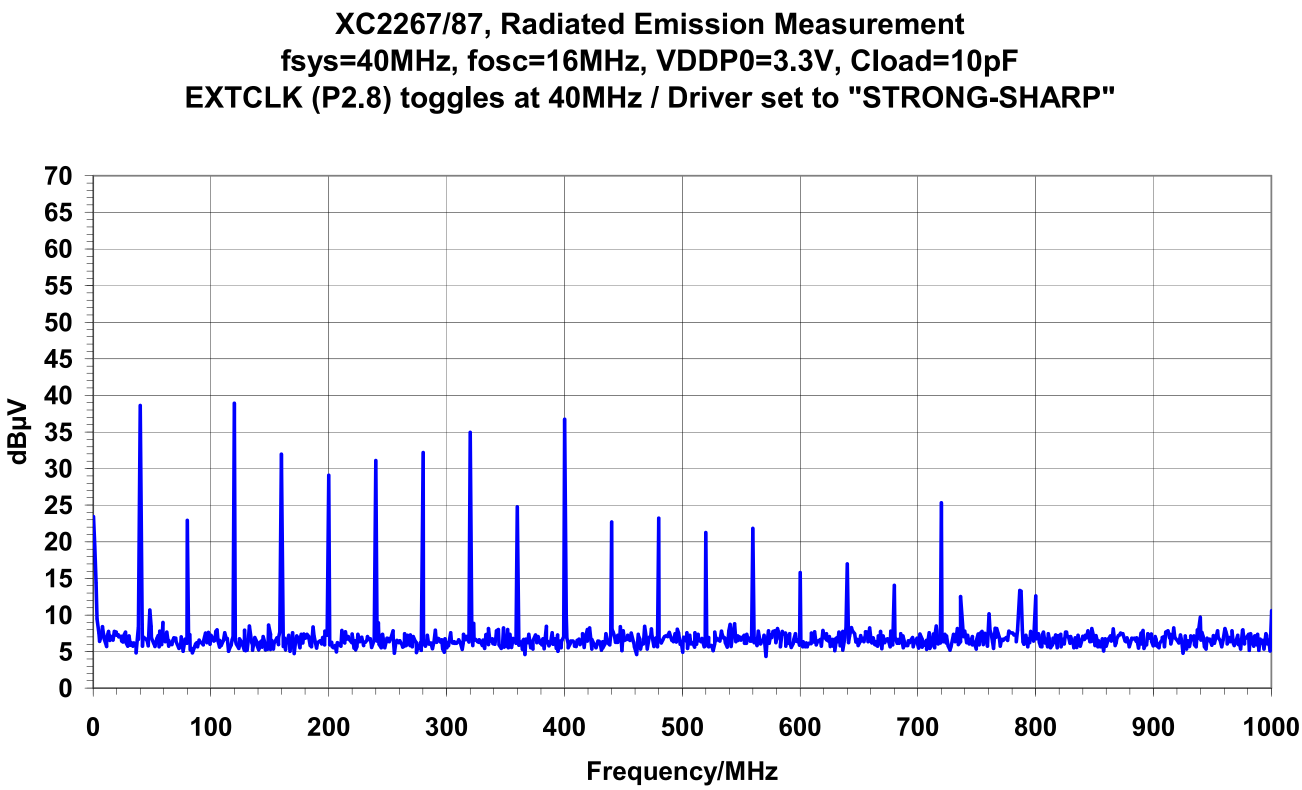

Figure 114: Emission Spectrum for STRONG-SHARP/40MHz/10pF/3.3V/Radiated

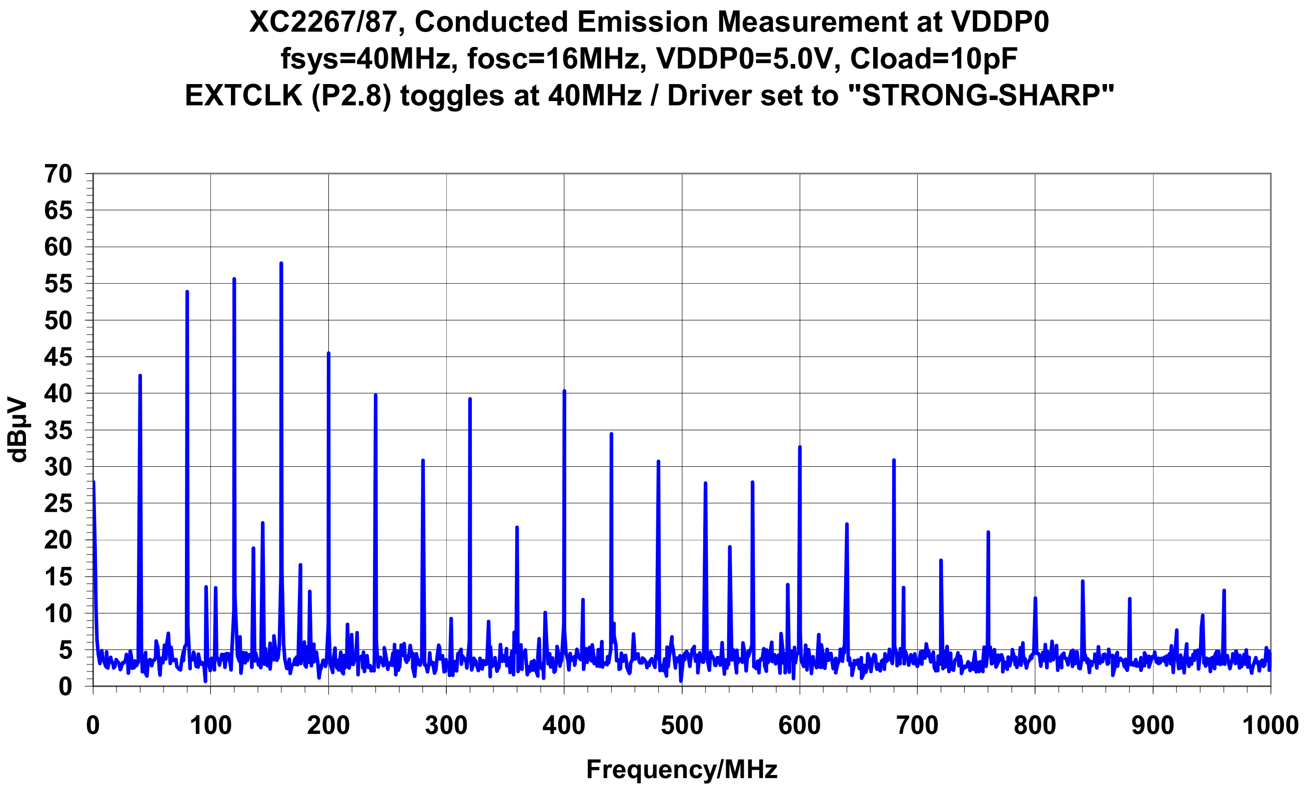

Figure 115: Emission Spectrum for STRONG-SHARP/40MHz/10pF/5.0V/Conducted

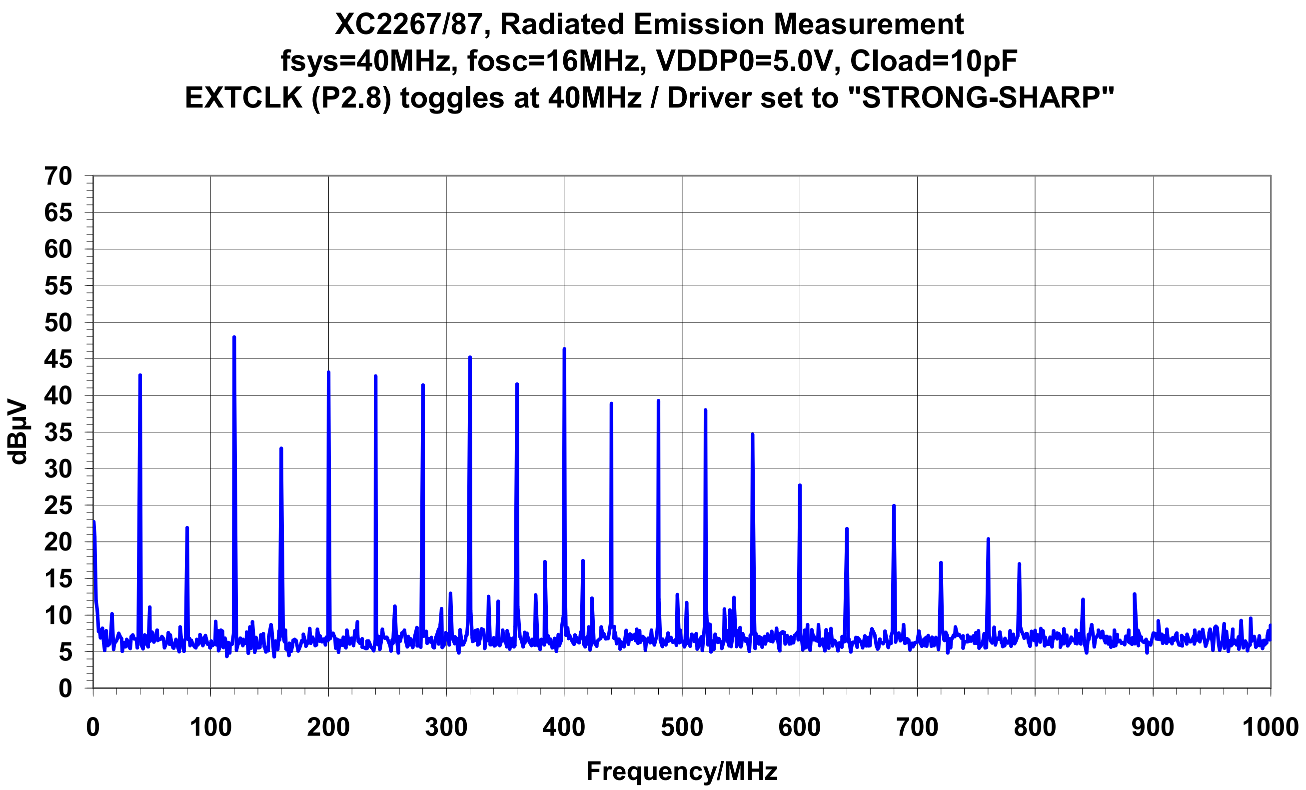

Figure 116: Emission Spectrum for STRONG-SHARP/40MHz/10pF/5.0V/Radiated

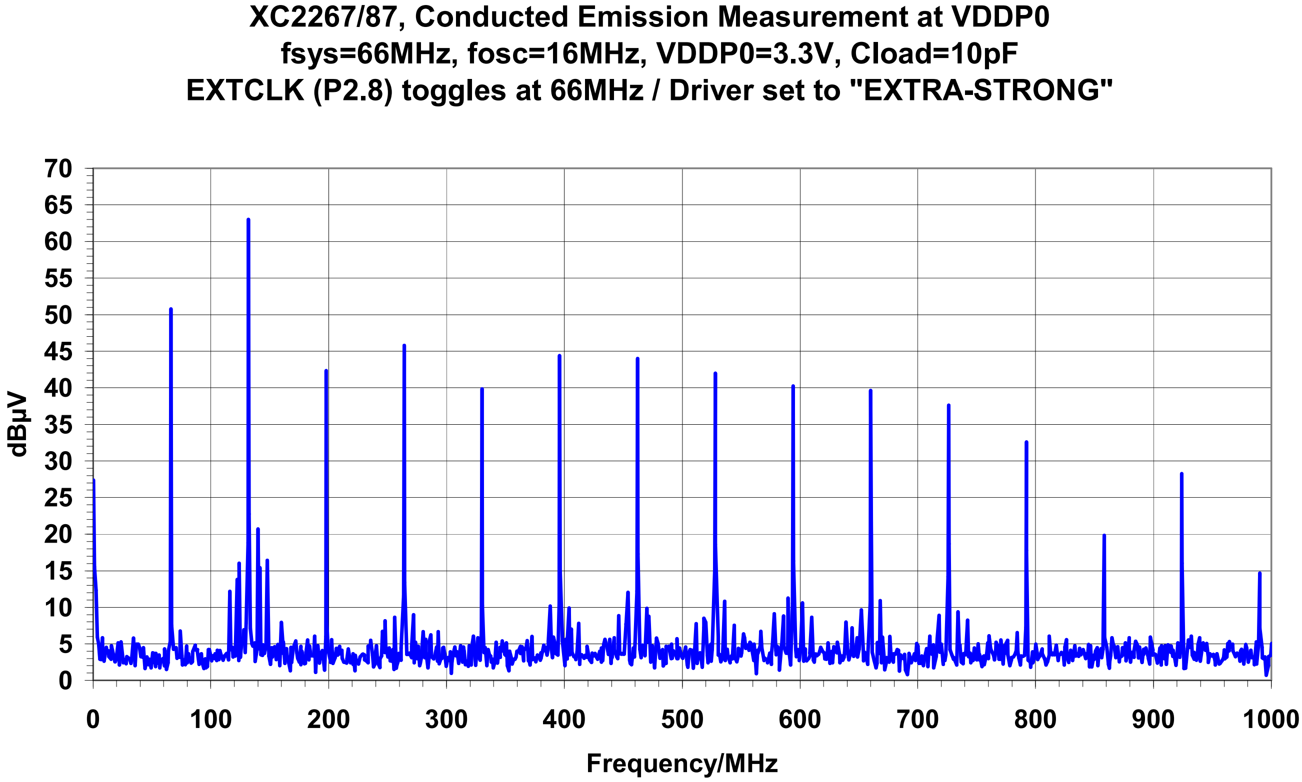

Figure 117: Emission Spectrum for EXTRA-STRONG/66MHz/10pF/3.3V/Conducted

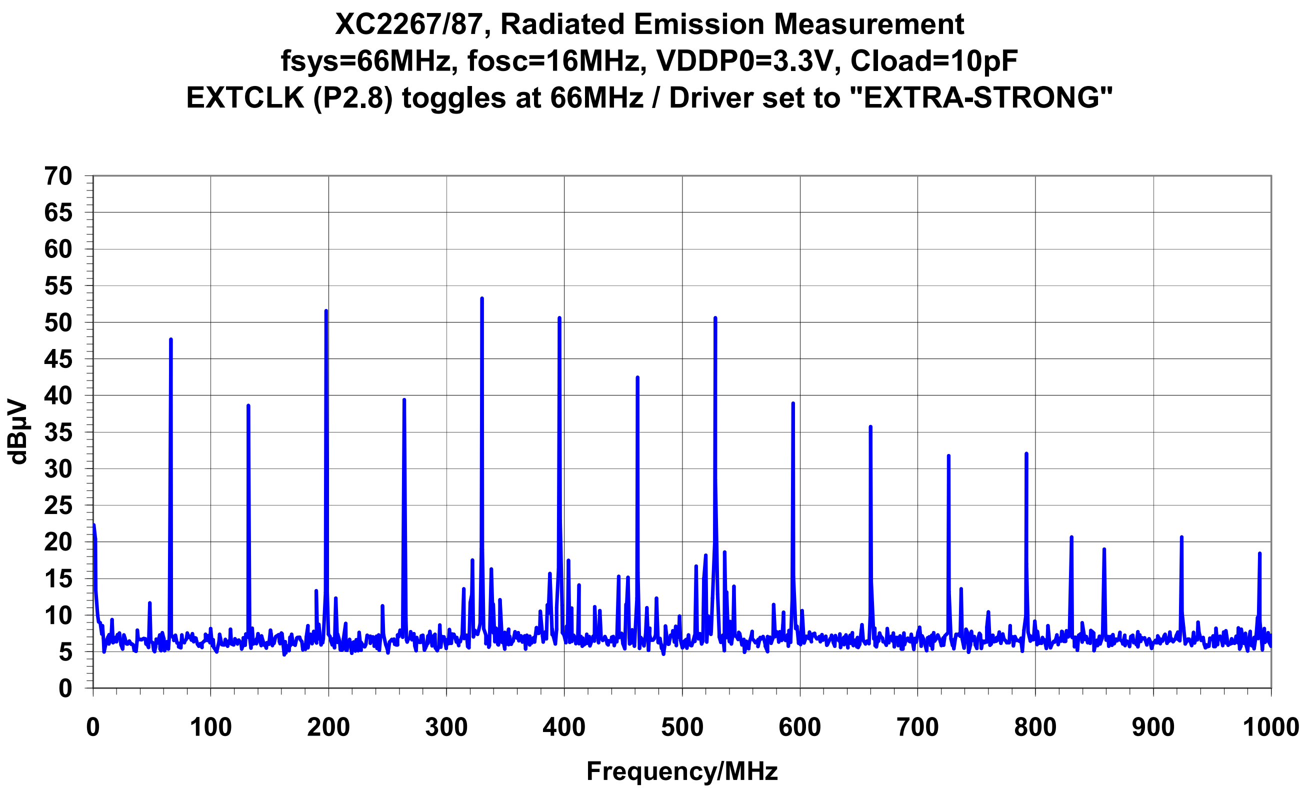

Figure 118: Emission Spectrum for EXTRA-STRONG/66MHz/10pF/3.3V/Radiated

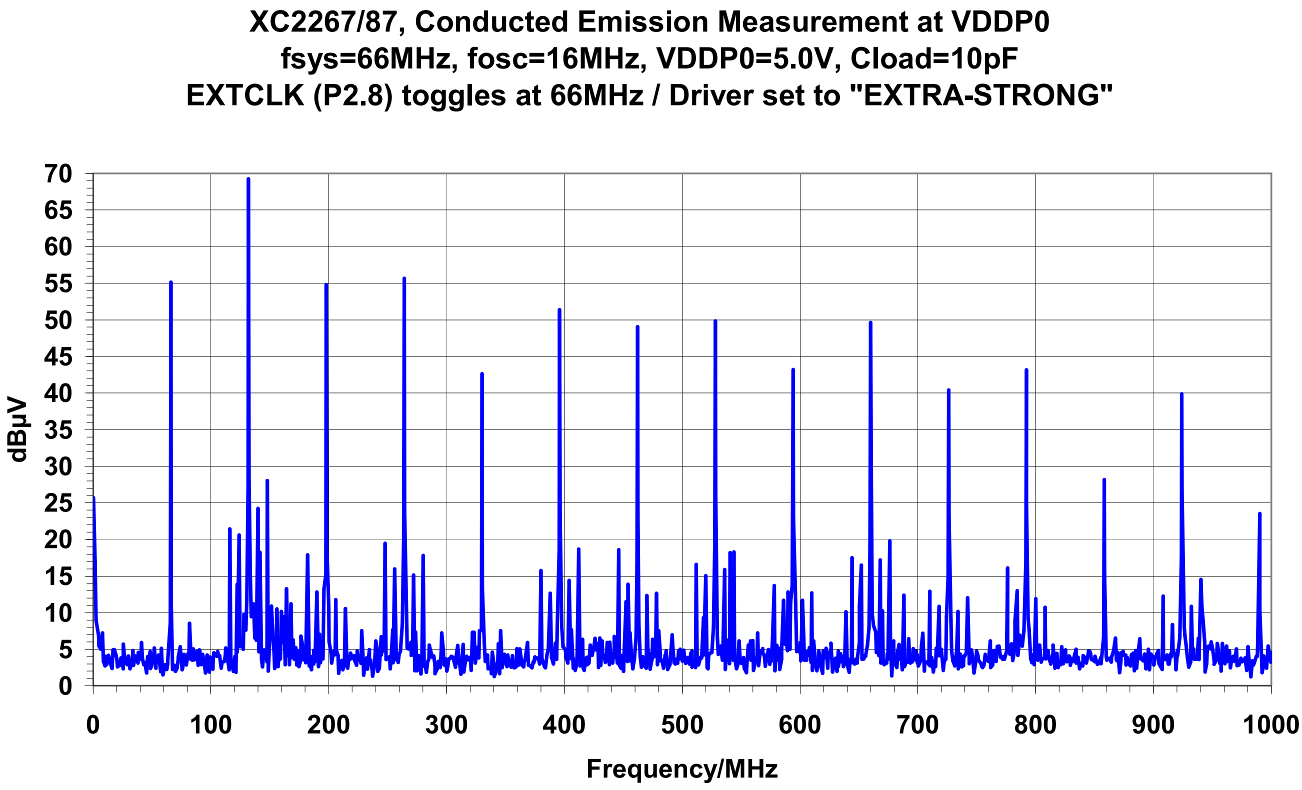

Figure 119: Emission Spectrum for EXTRA-STRONG/66MHz/10pF/5.0V/Conducted

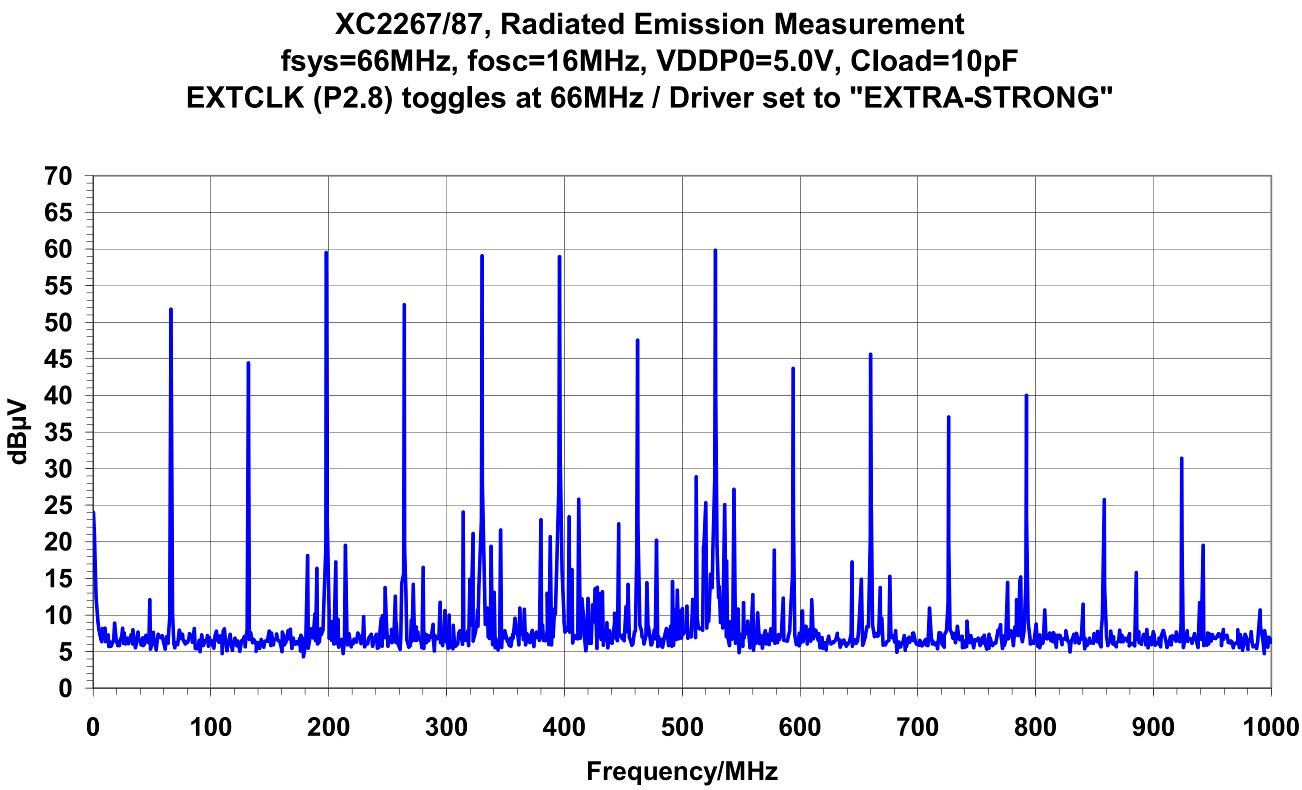

Figure 120: Emission Spectrum for EXTRA-STRONG/66MHz/10pF/5.0V/Radiated

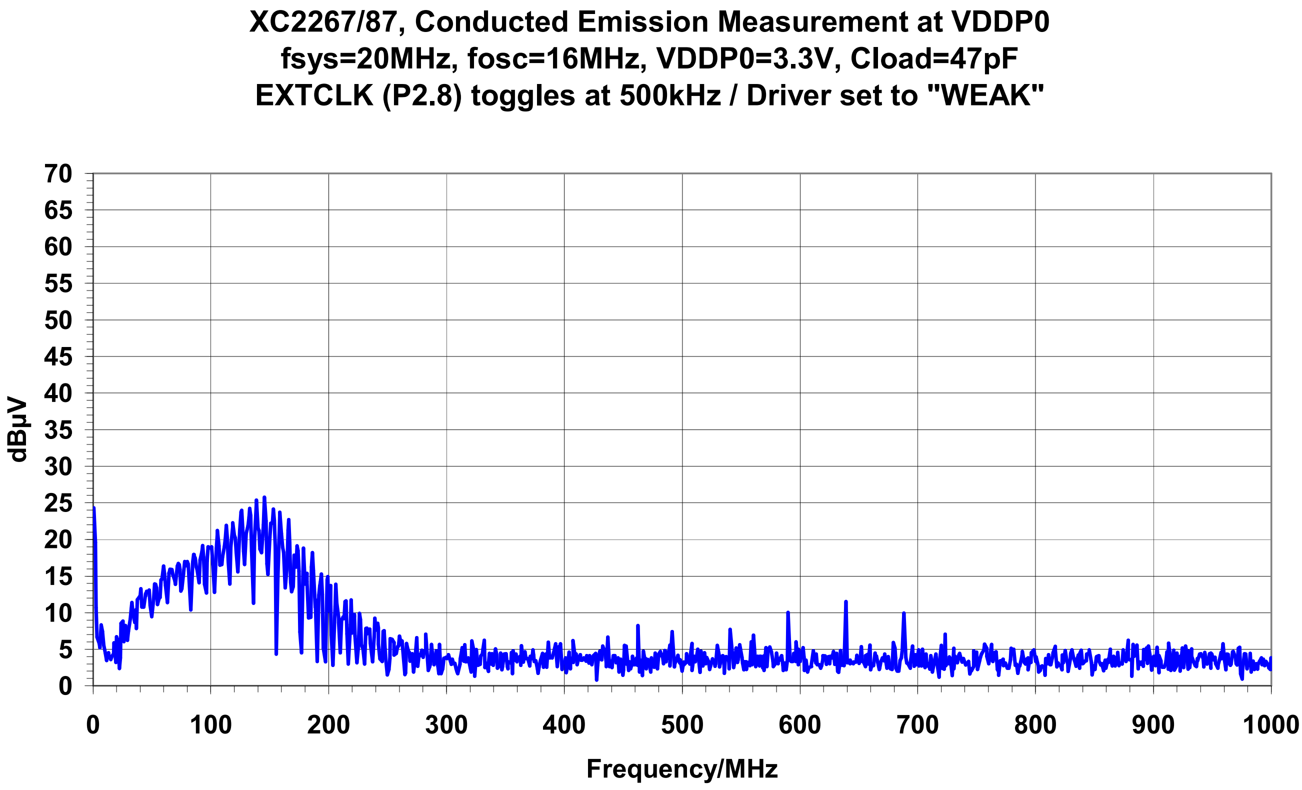

Figure 121: Emission Spectrum for WEAK/500kHz/47pF/3.3V/Conducted

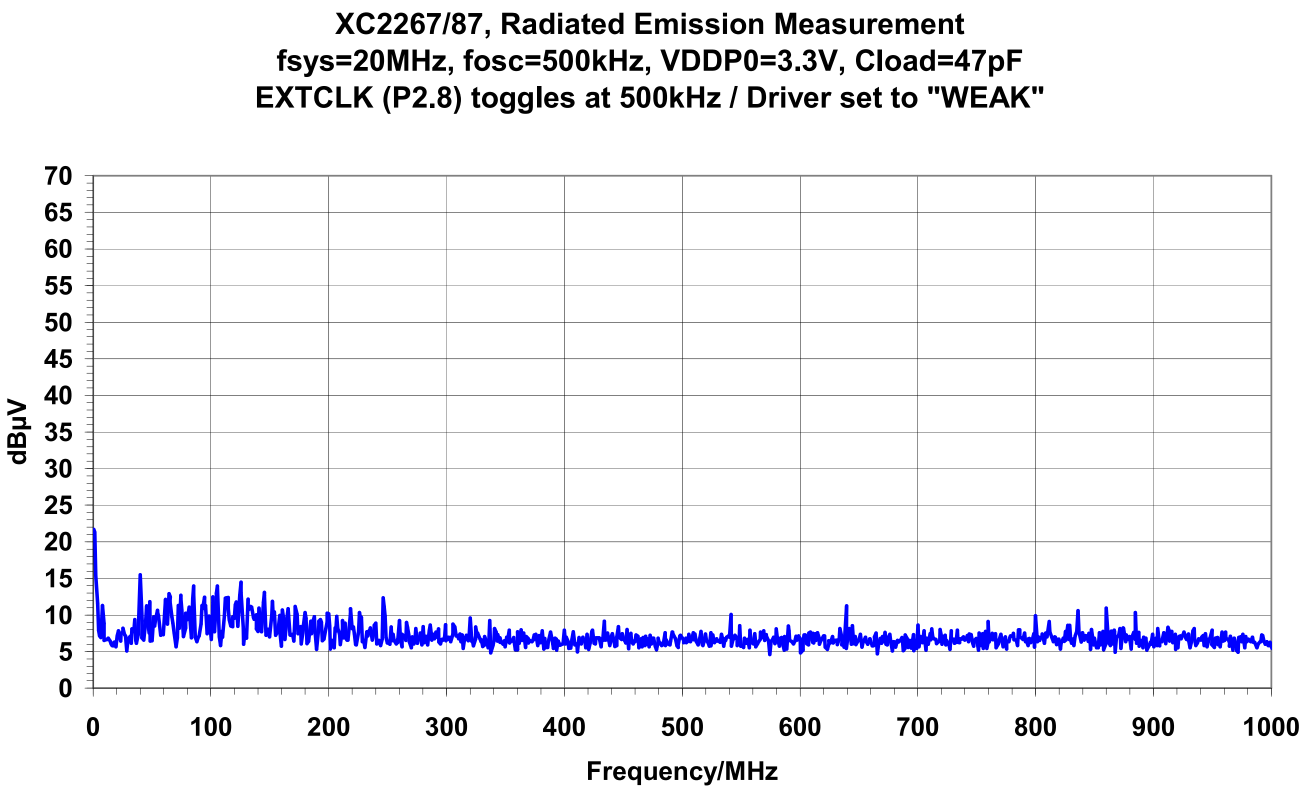

Figure 122: Emission Spectrum for WEAK/500kHz/47pF/3.3V/Radiated

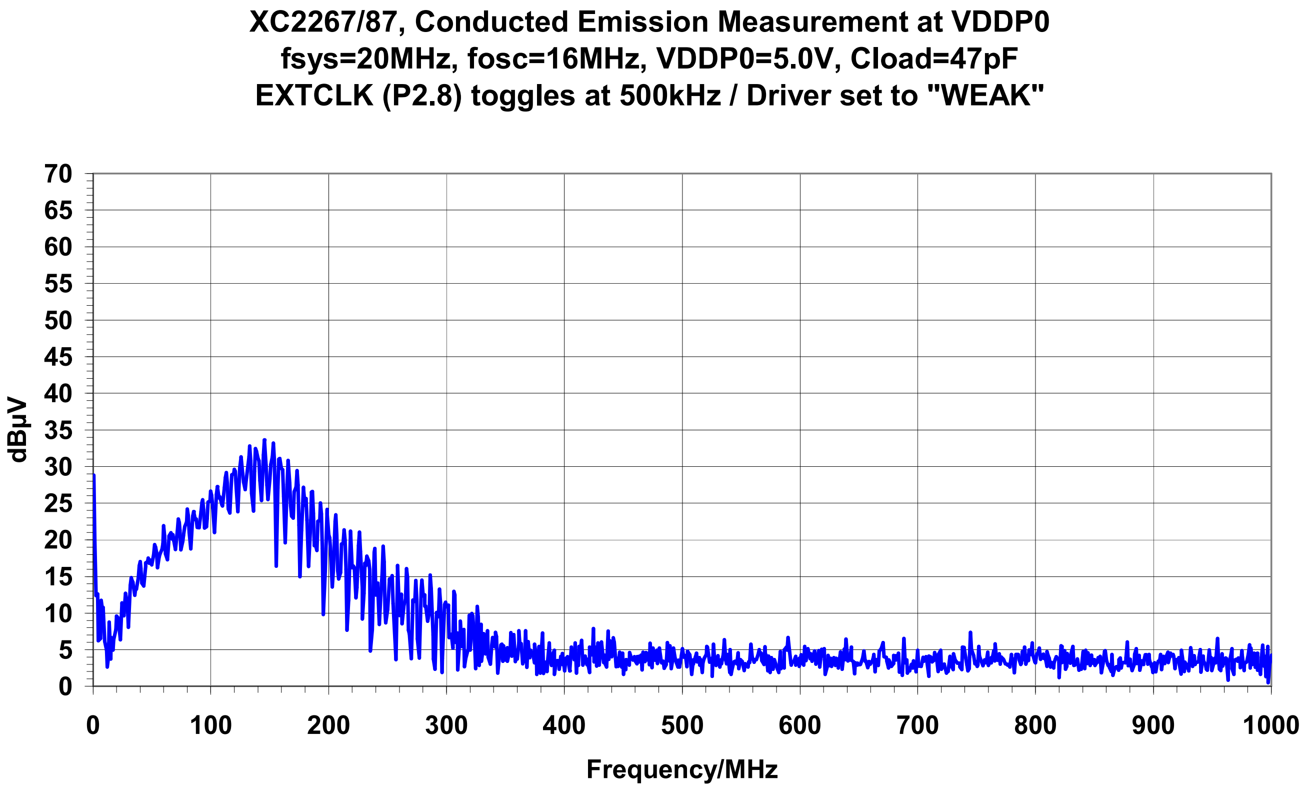

Figure 123: Emission Spectrum for WEAK/500kHz/47pF/5.0V/Conducted

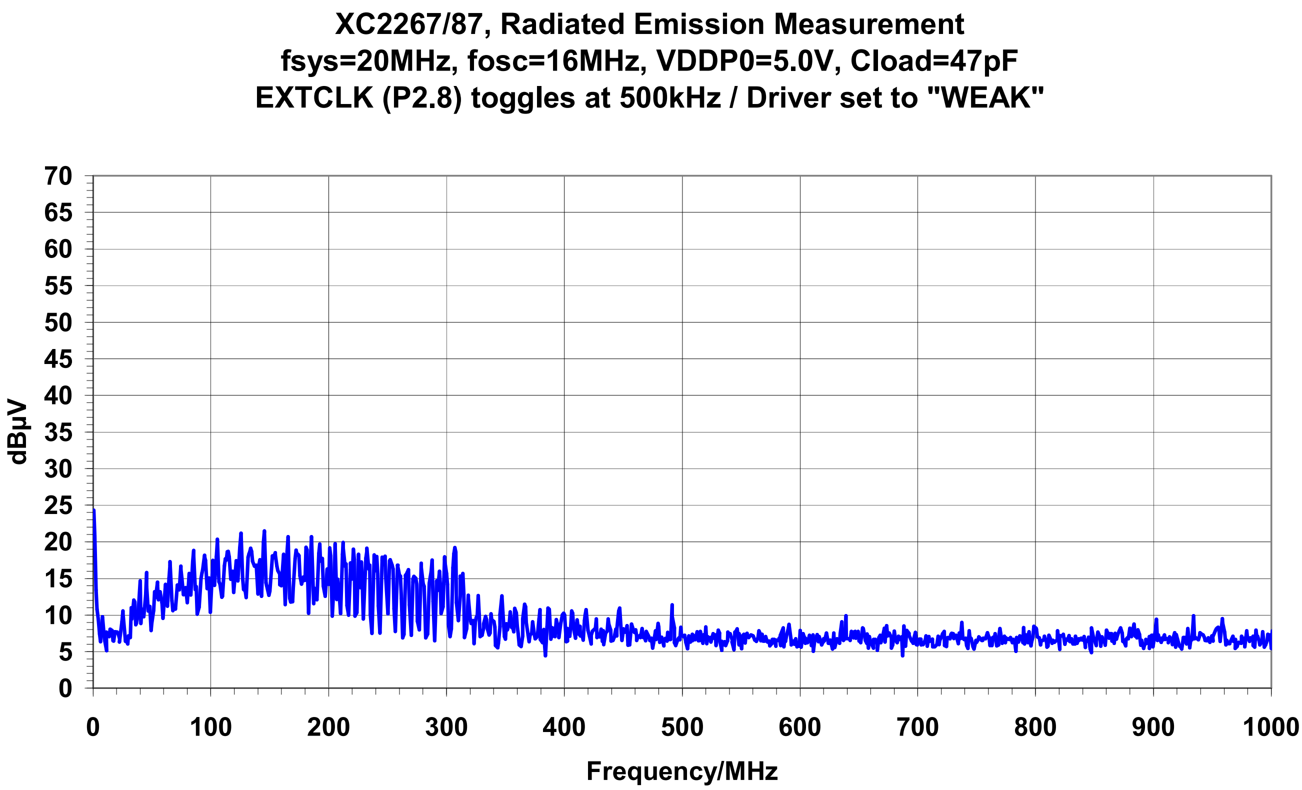

Figure 124: Emission Spectrum for WEAK/500kHz/47pF/5.0V/Radiated

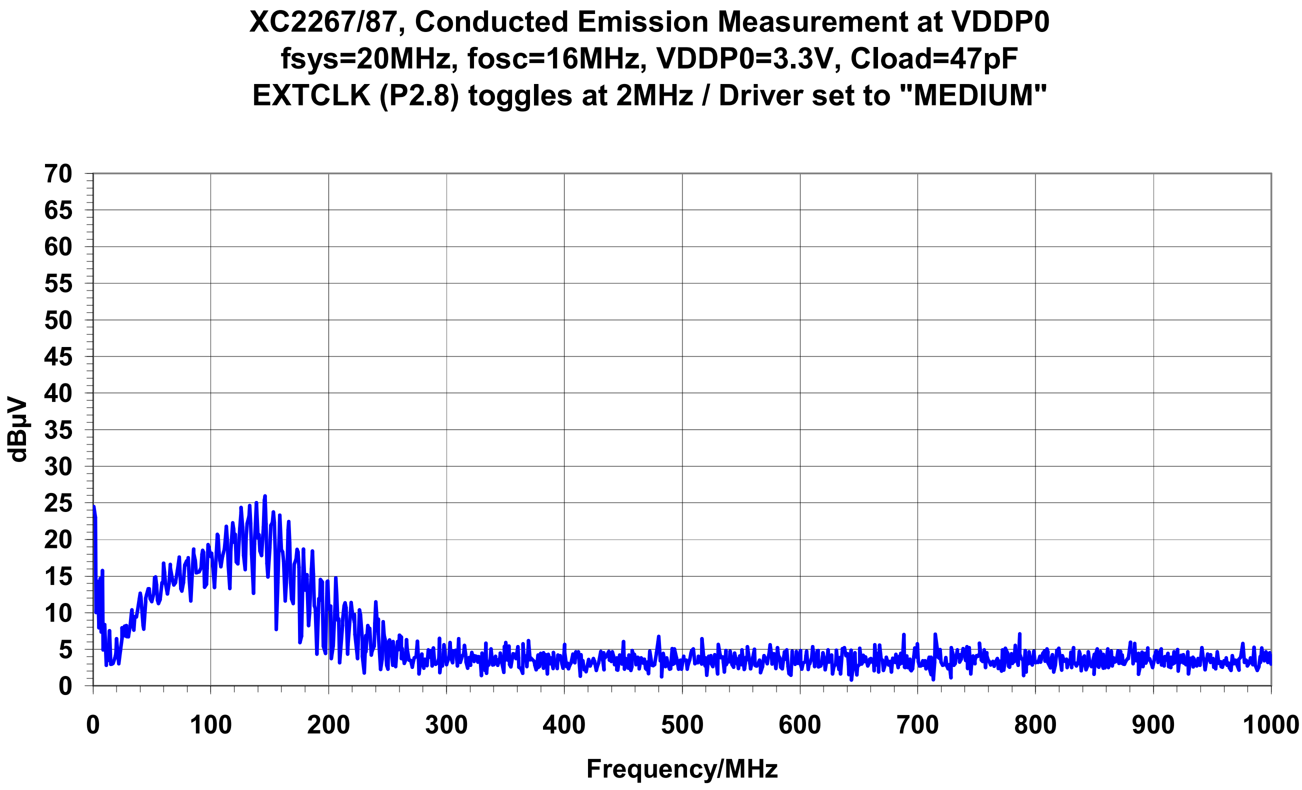

Figure 125: Emission Spectrum for MEDIUM/2MHz/47pF/3.3V/Conducted

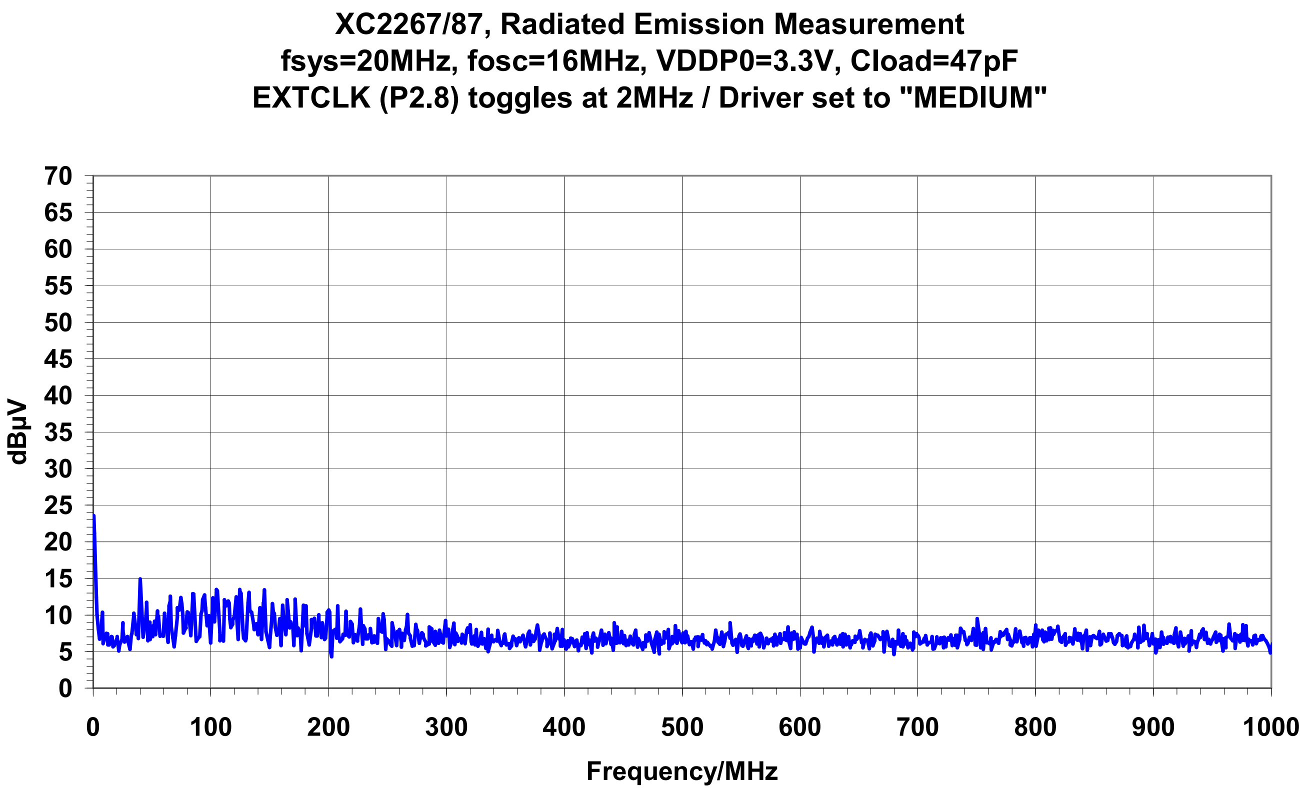

Figure 126: Emission Spectrum for MEDIUM/2MHz/47pF/3.3V/Radiated

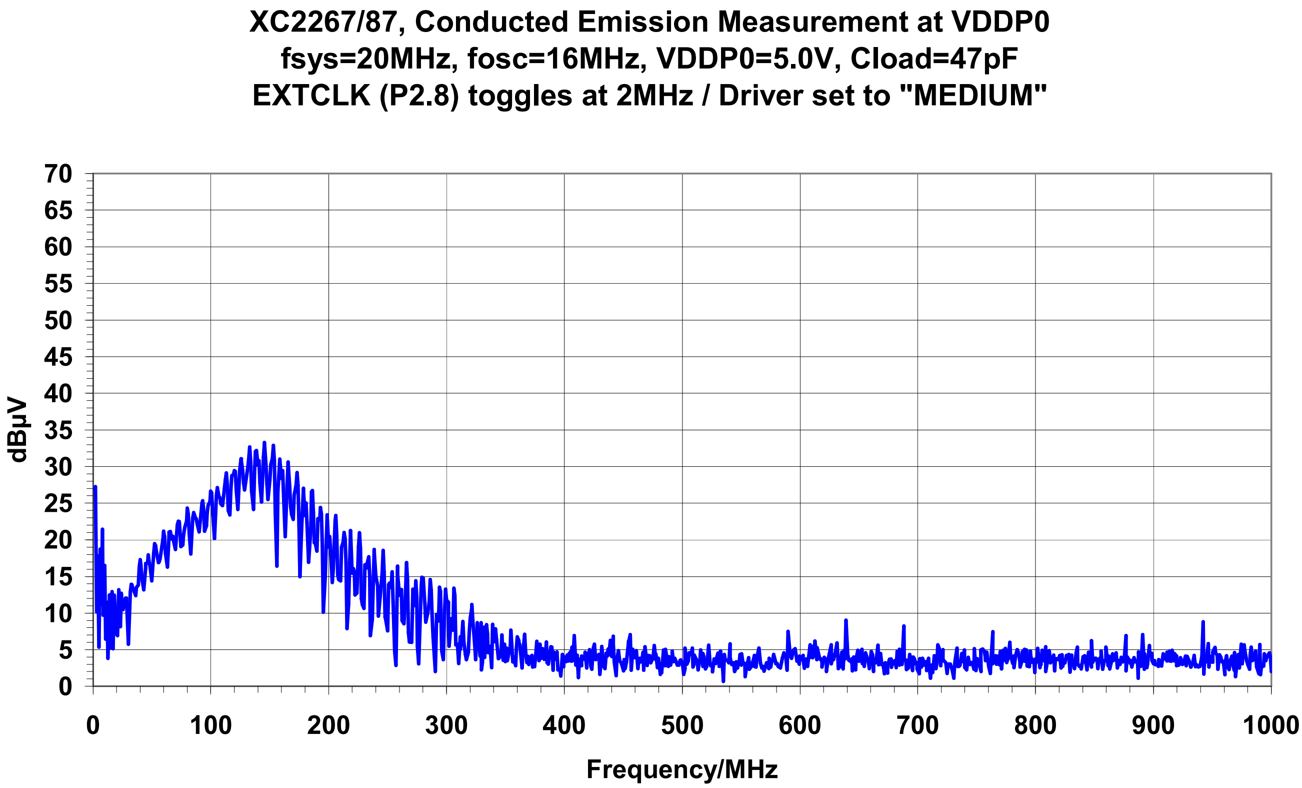

Figure 127: Emission Spectrum for MEDIUM/2MHz/47pF/5.0V/Conducted

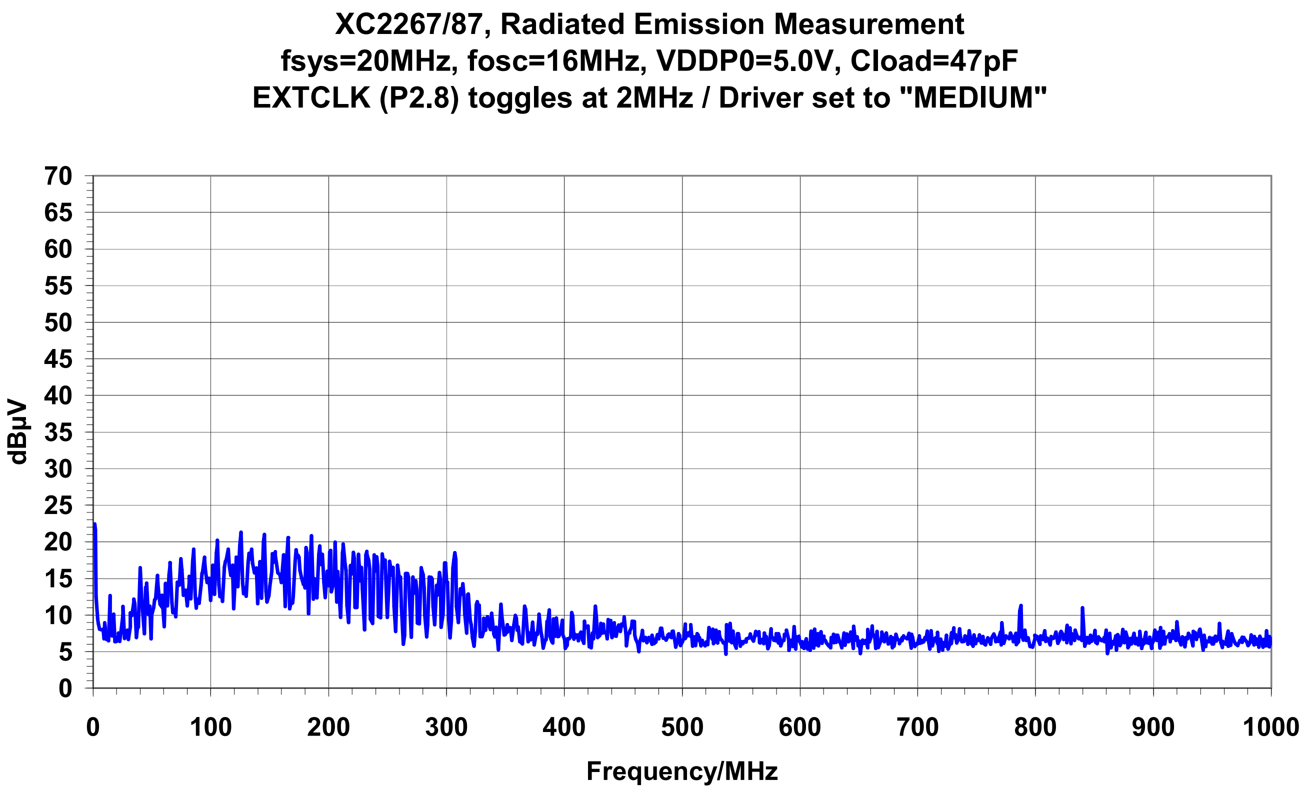

Figure 128: Emission Spectrum for MEDIUM/2MHz/47pF/5.0V/Radiated

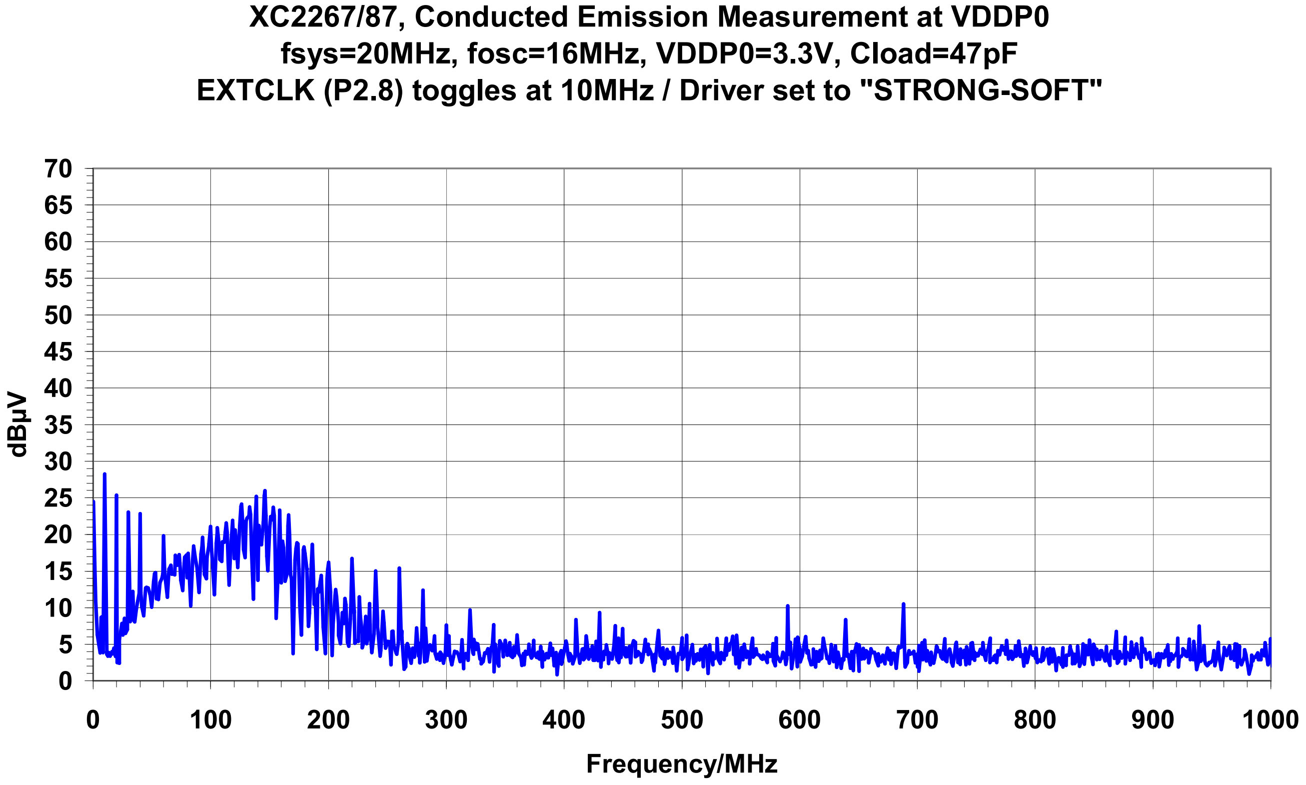

Figure 129: Emission Spectrum for STRONG-SOFT/10MHz/47pF/3.3V/Conducted

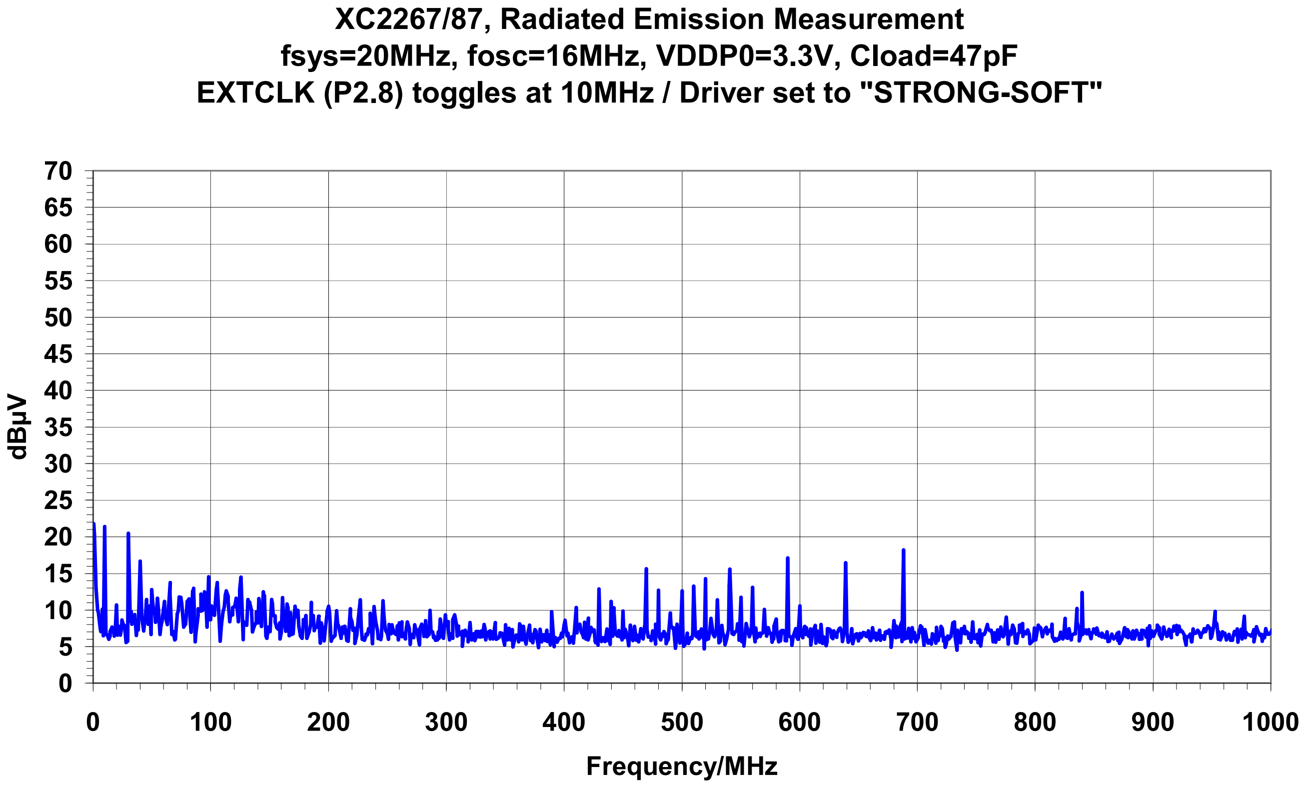

Figure 130: Emission Spectrum for STRONG-SOFT/10MHz/47pF/3.3V/Radiated

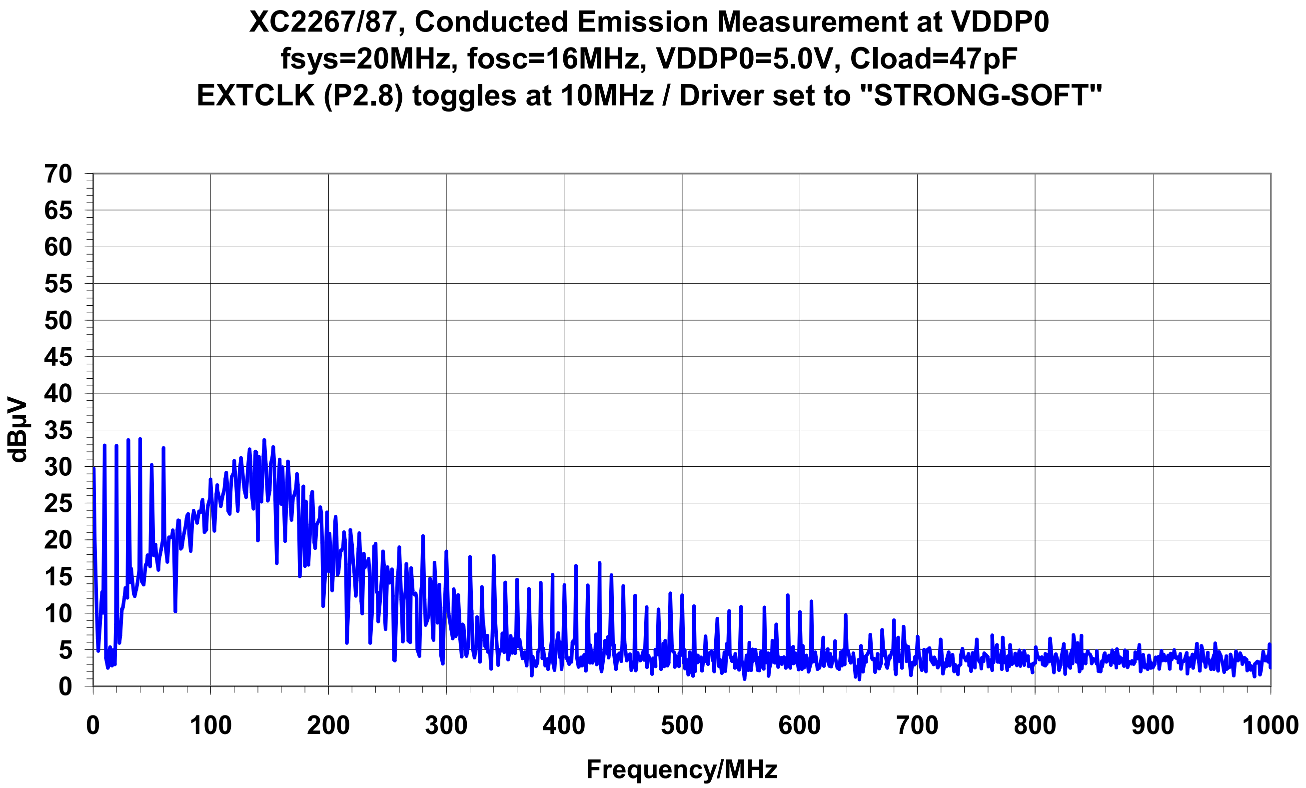

Figure 131: Emission Spectrum for STRONG-SOFT/10MHz/47pF/5.0V/Conducted

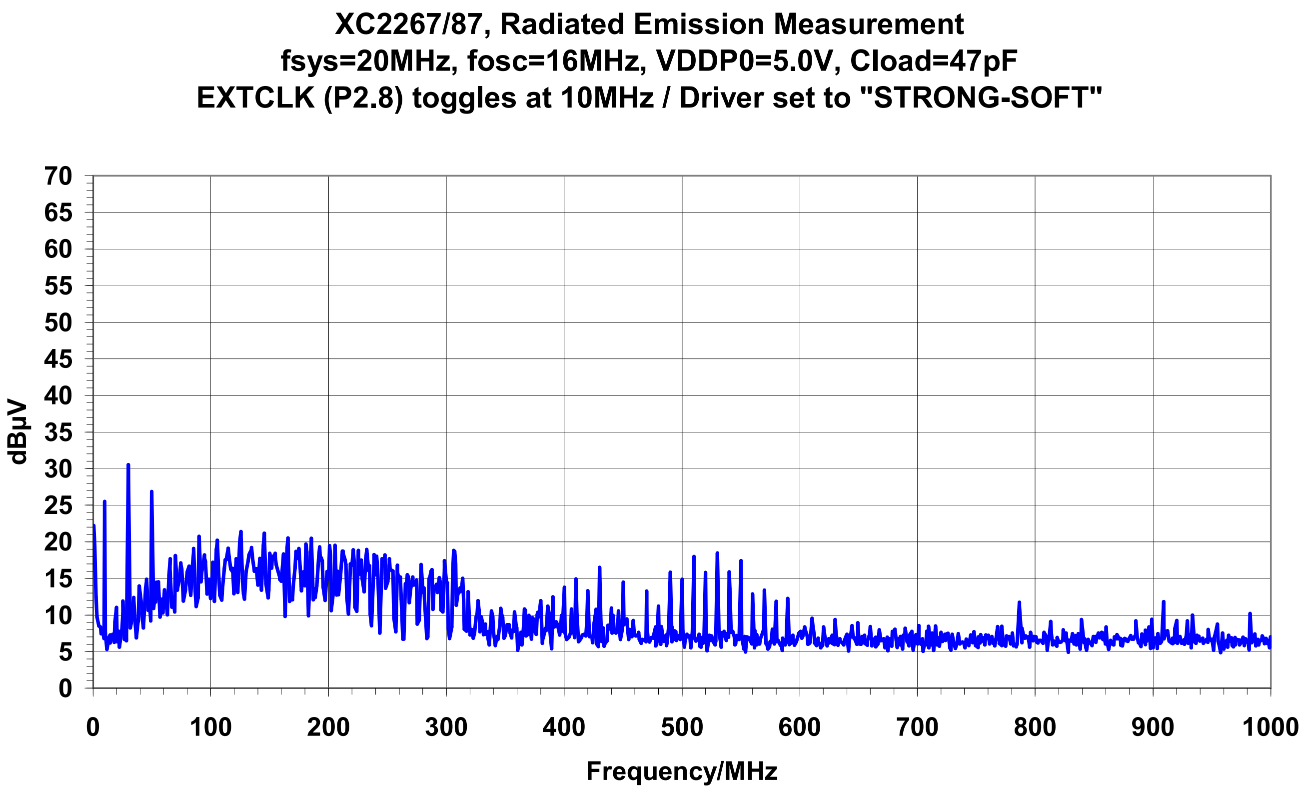

Figure 132: Emission Spectrum for STRONG-SOFT/10MHz/47pF/5.0V/Radiated

XC2267/87, Conducted Emission Measurement at VDDP0
fsys=20MHz, fosc=16MHz, VDDP0=3.3V, Cload=47pF
EXTCLK (P2.8) toggles at 10MHz / Driver set to "STRONG-MEDIUM"

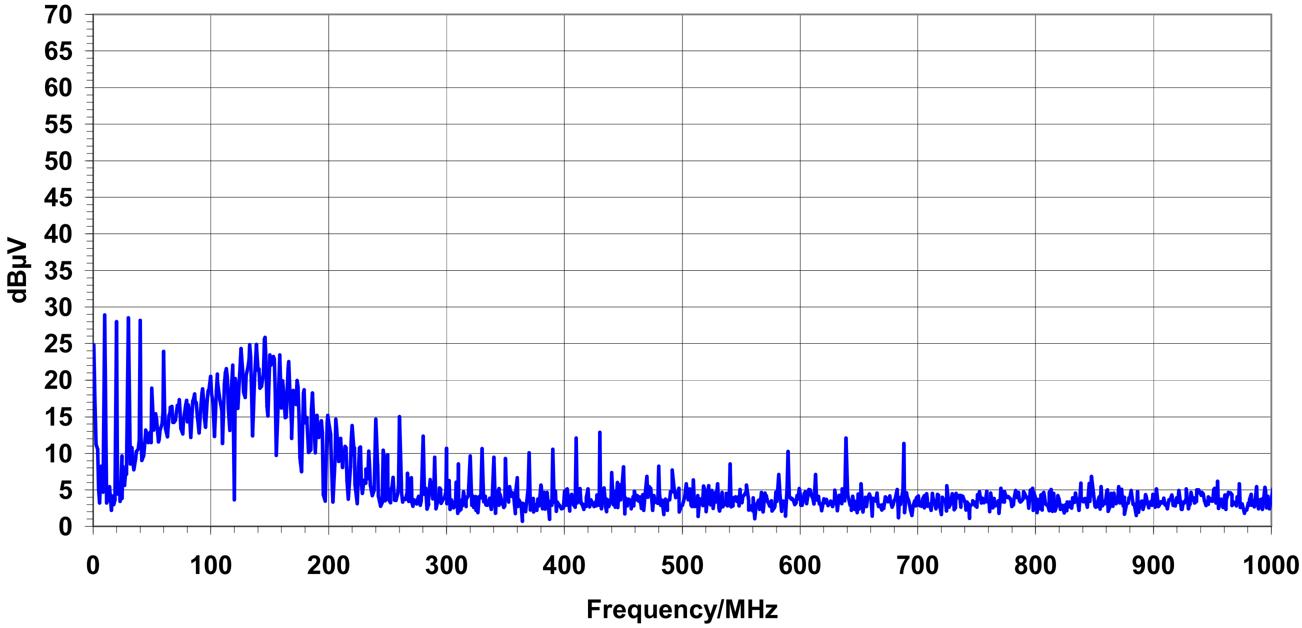

Figure 133: Emission Spectrum for STRONG-MEDIUM/10MHz/47pF/3.3V/Conducted

XC2267/87, Radiated Emission Measurement
fsys=20MHz, fosc=16MHz, VDDP0=3.3V, Cload=47pF
EXTCLK (P2.8) toggles at 10MHz / Driver set to "STRONG-MEDIUM"

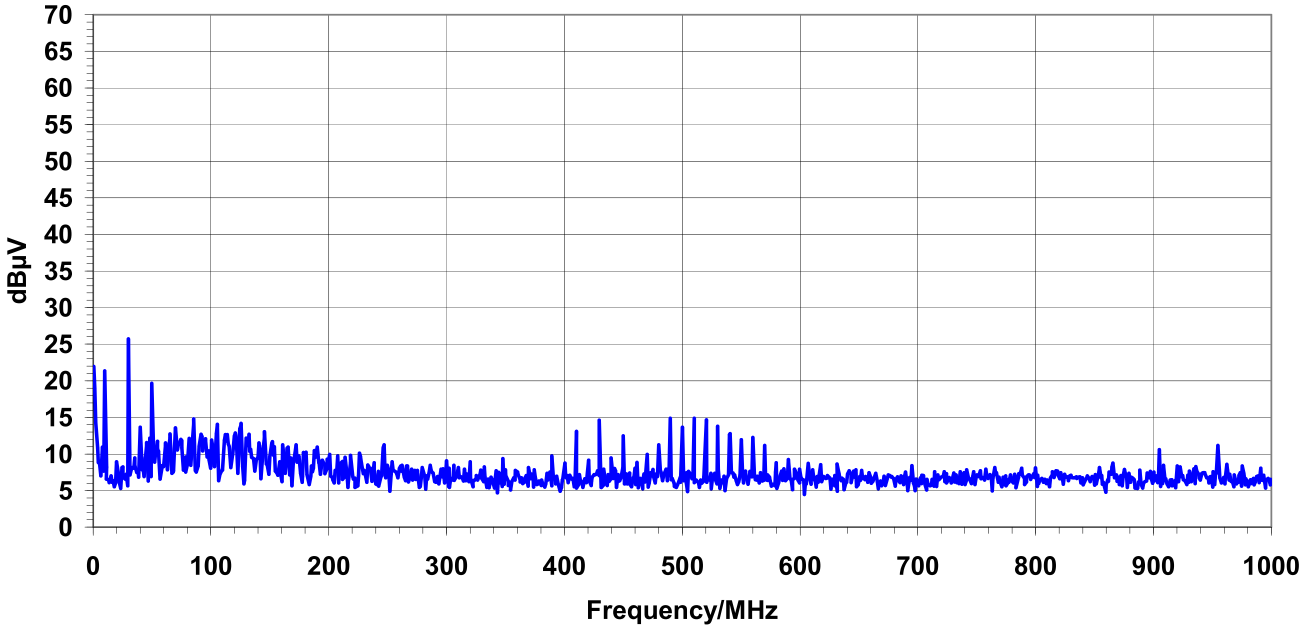

Figure 134: Emission Spectrum for STRONG-MEDIUM/10MHz/47pF/3.3V/Radiated

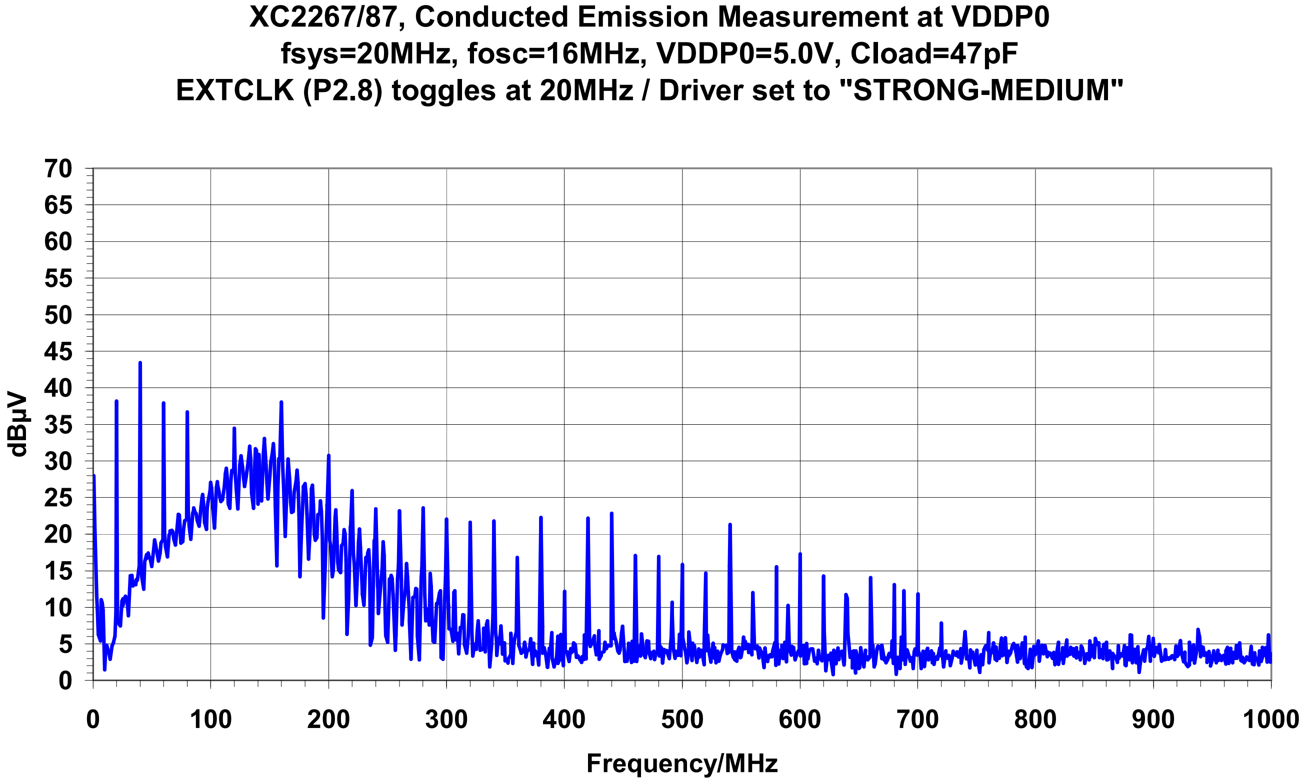

Figure 135: Emission Spectrum for STRONG-MEDIUM/20MHz/47pF/5.0V/Conducted

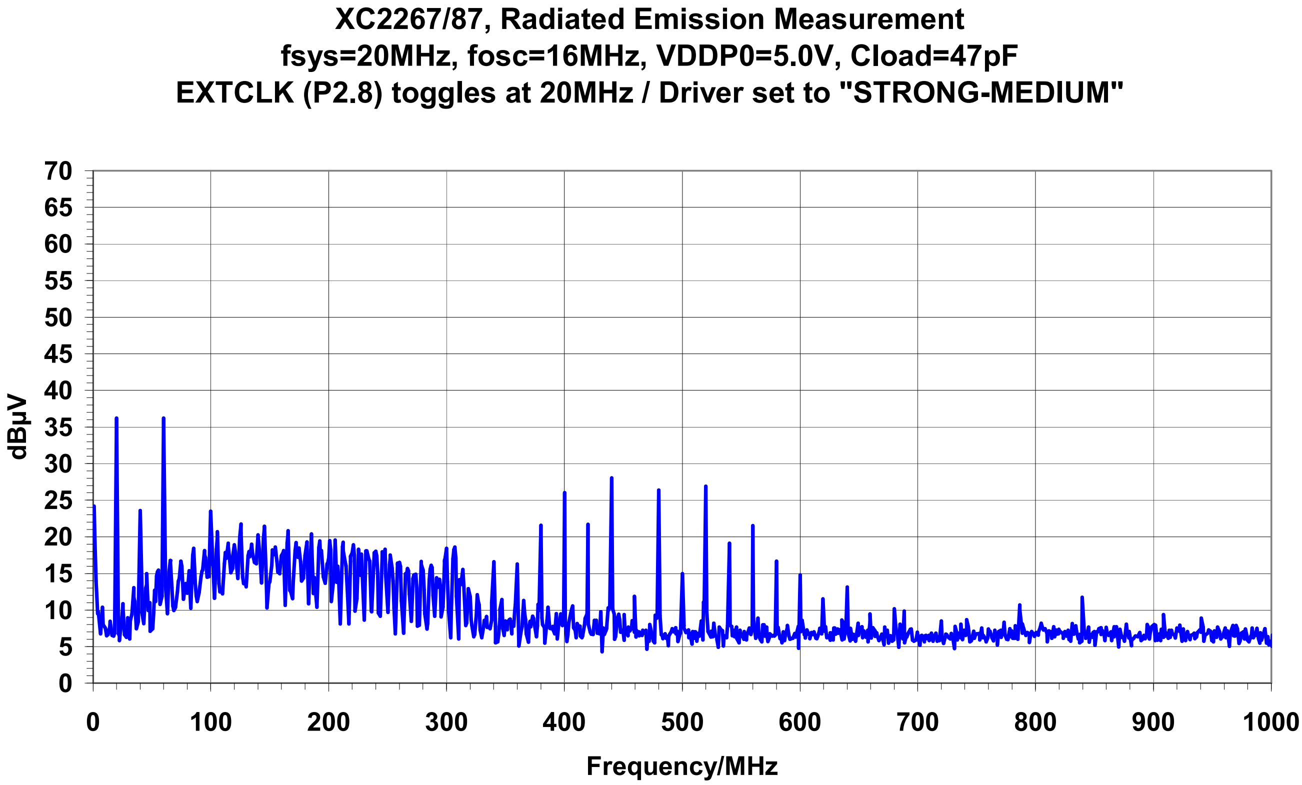

Figure 136: Emission Spectrum for STRONG-MEDIUM/20MHz/47pF/5.0V/Radiated

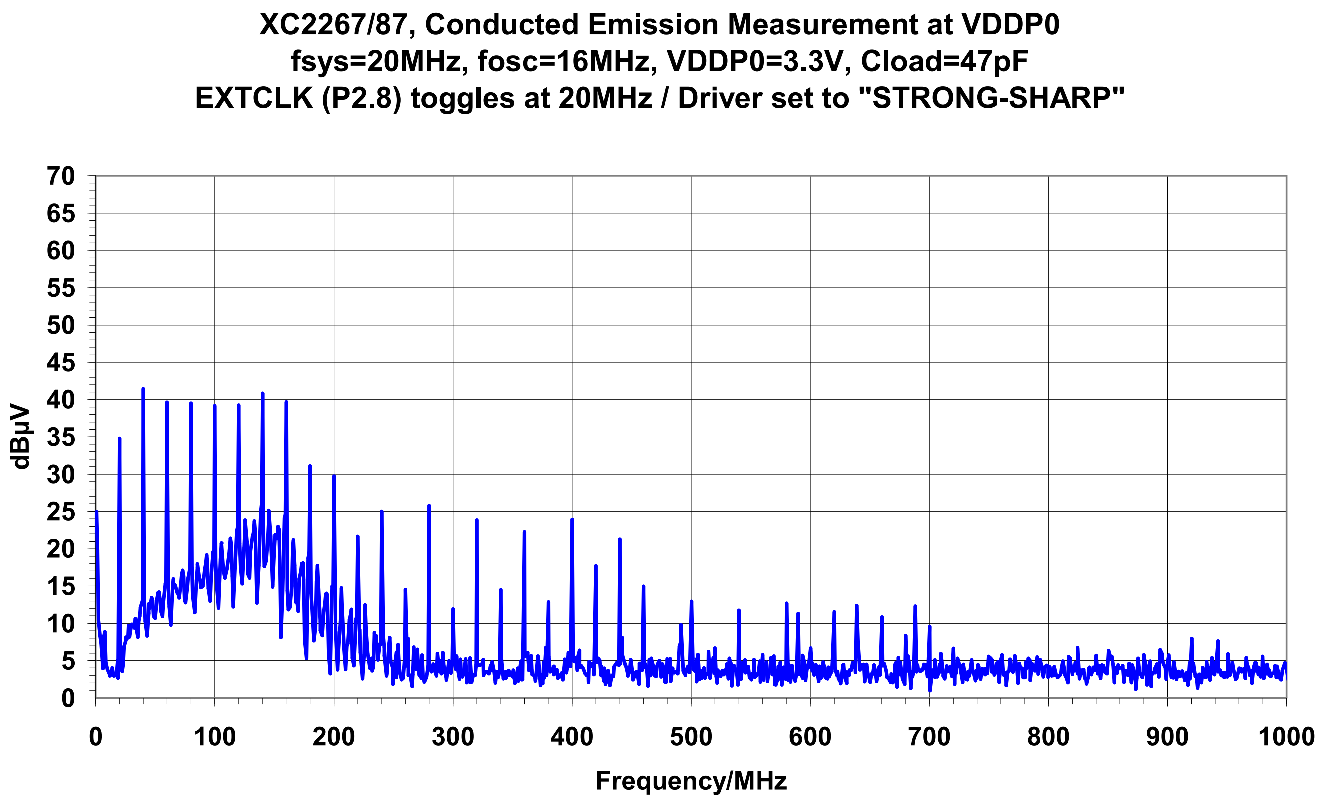

Figure 137: Emission Spectrum for STRONG-SHARP/20MHz/47pF/3.3V/Conducted

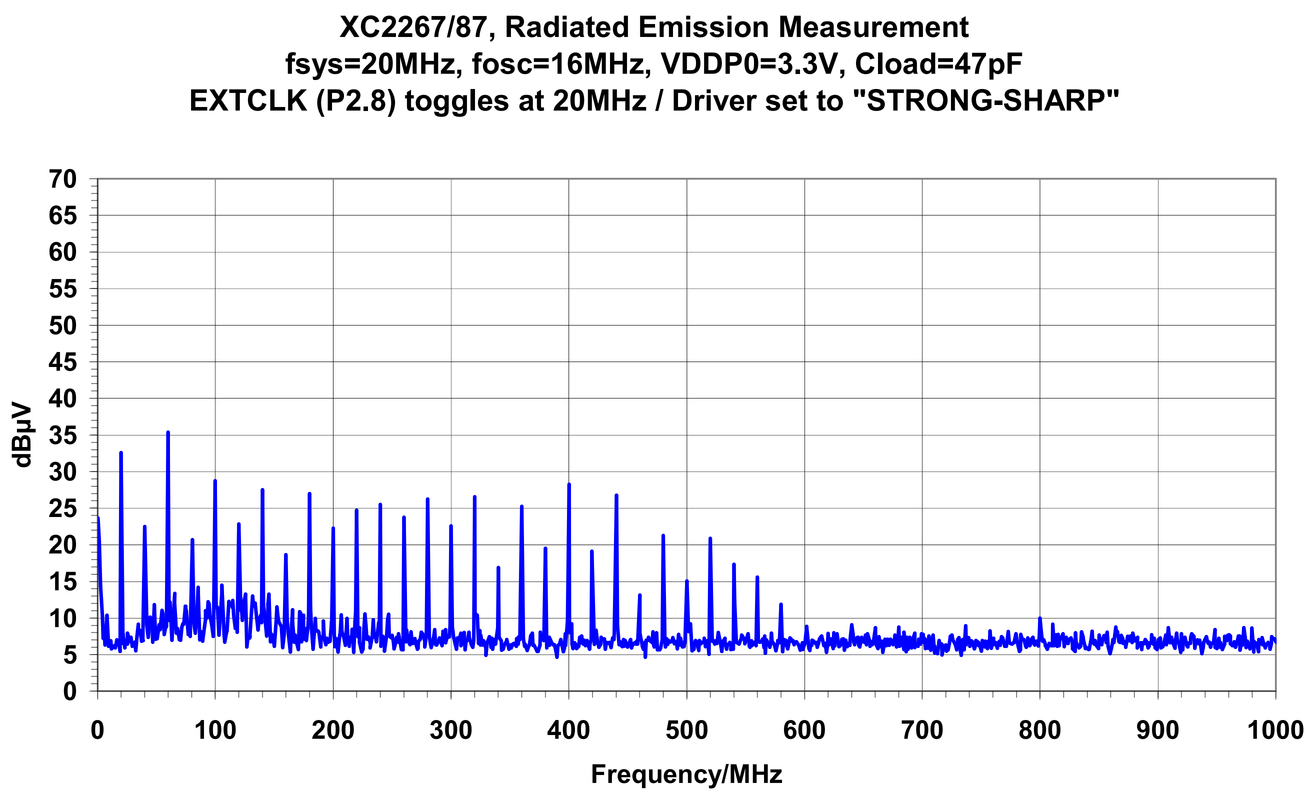

Figure 138: Emission Spectrum for STRONG-SHARP/20MHz/47pF/3.3V/Radiated

XC2267/87, Conducted Emission Measurement at VDDP0
fsys=40MHz, fosc=16MHz, VDDP0=5.0V, Cload=47pF
EXTCLK (P2.8) toggles at 40MHz / Driver set to "STRONG-SHARP"

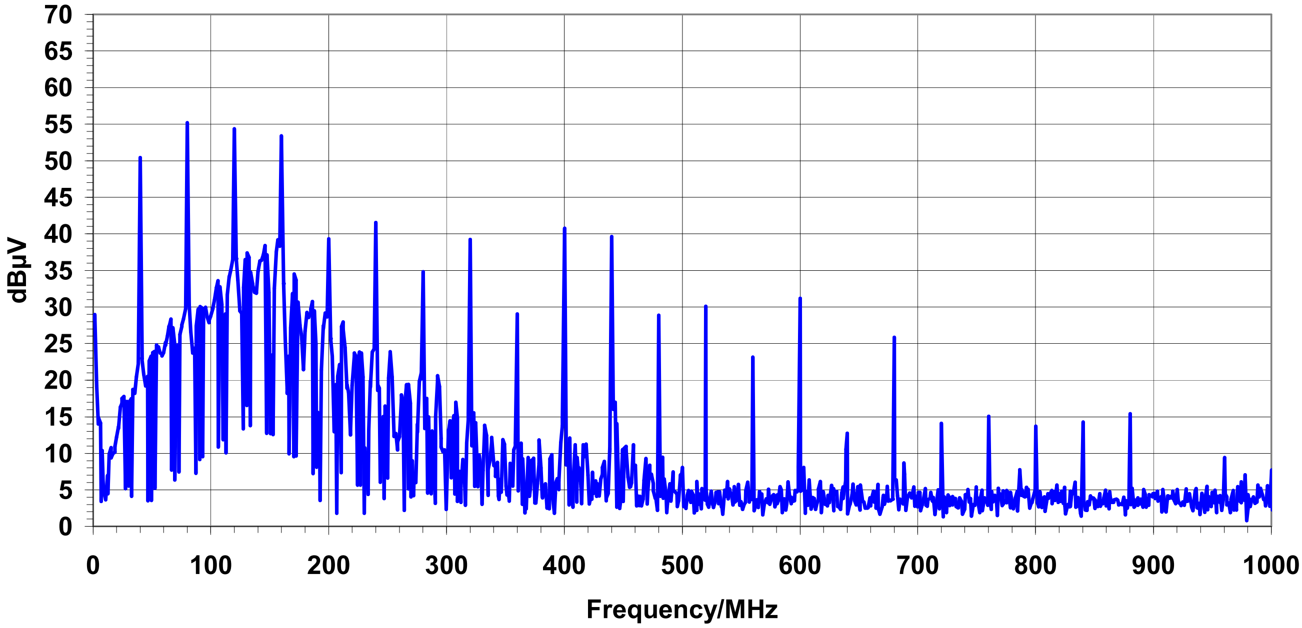

Figure 139: Emission Spectrum for STRONG-SHARP/40MHz /47pF/5.0V/Conducted

XC2267/87, Radiated Emission Measurement
fsys=40MHz, fosc=16MHz, VDDP0=5.0V, Cload=47pF
EXTCLK (P2.8) toggles at 40MHz / Driver set to "STRONG-SHARP"

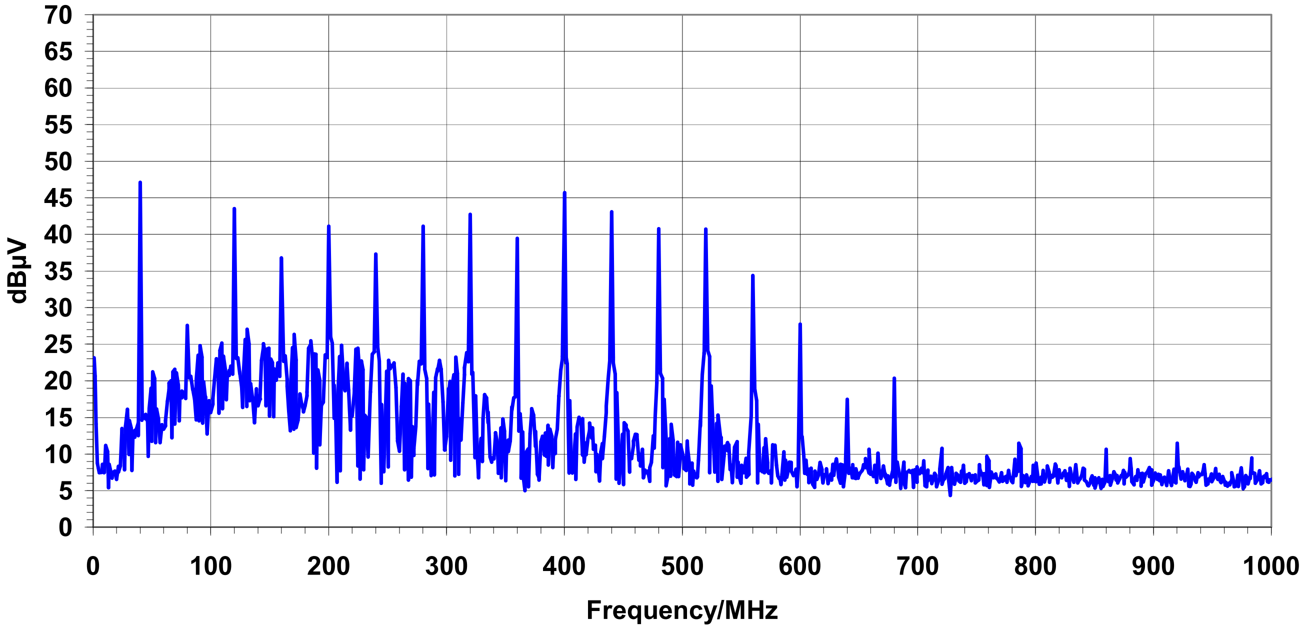

Figure 140: Emission Spectrum for STRONG-SHARP/40MHz/47pF/5.0V/Radiated

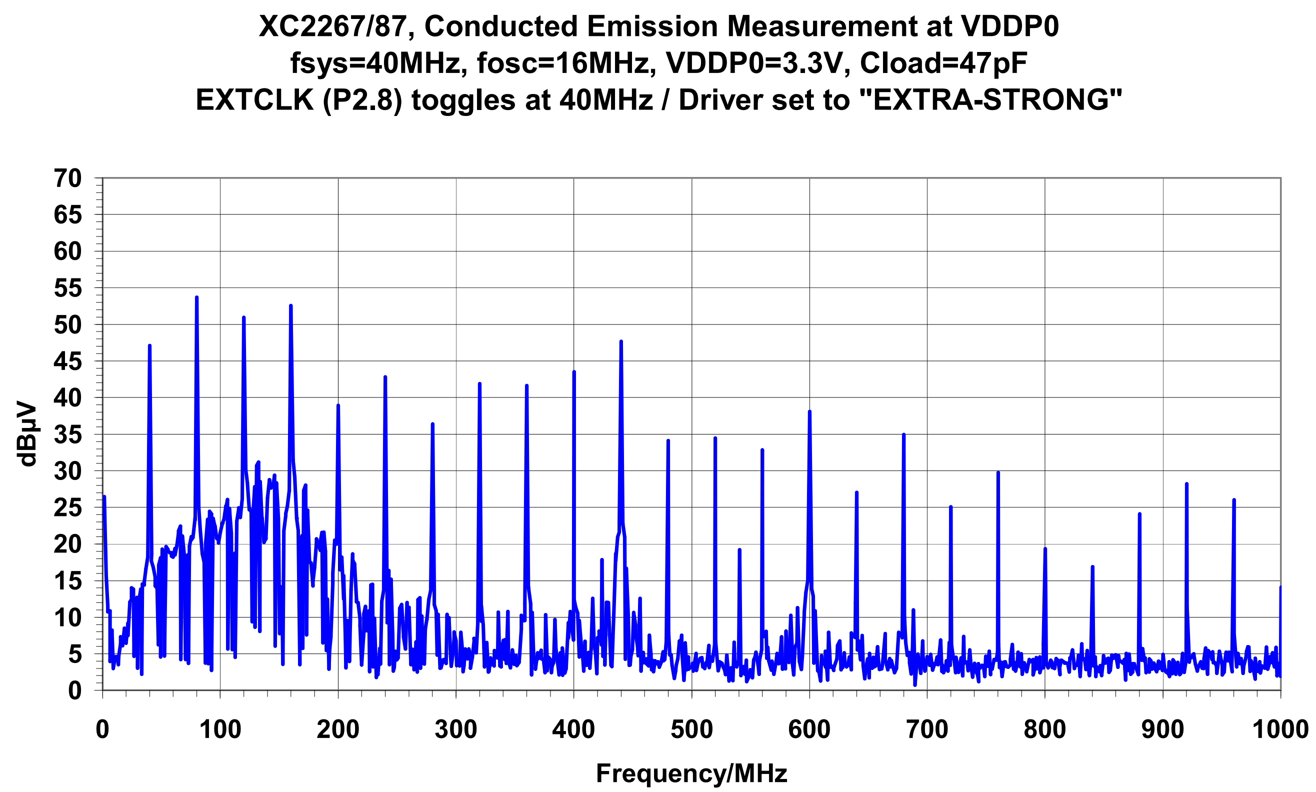

Figure 141: Emission Spectrum for EXTRA-STRONG/40MHz/47pF/3.3V/Conducted

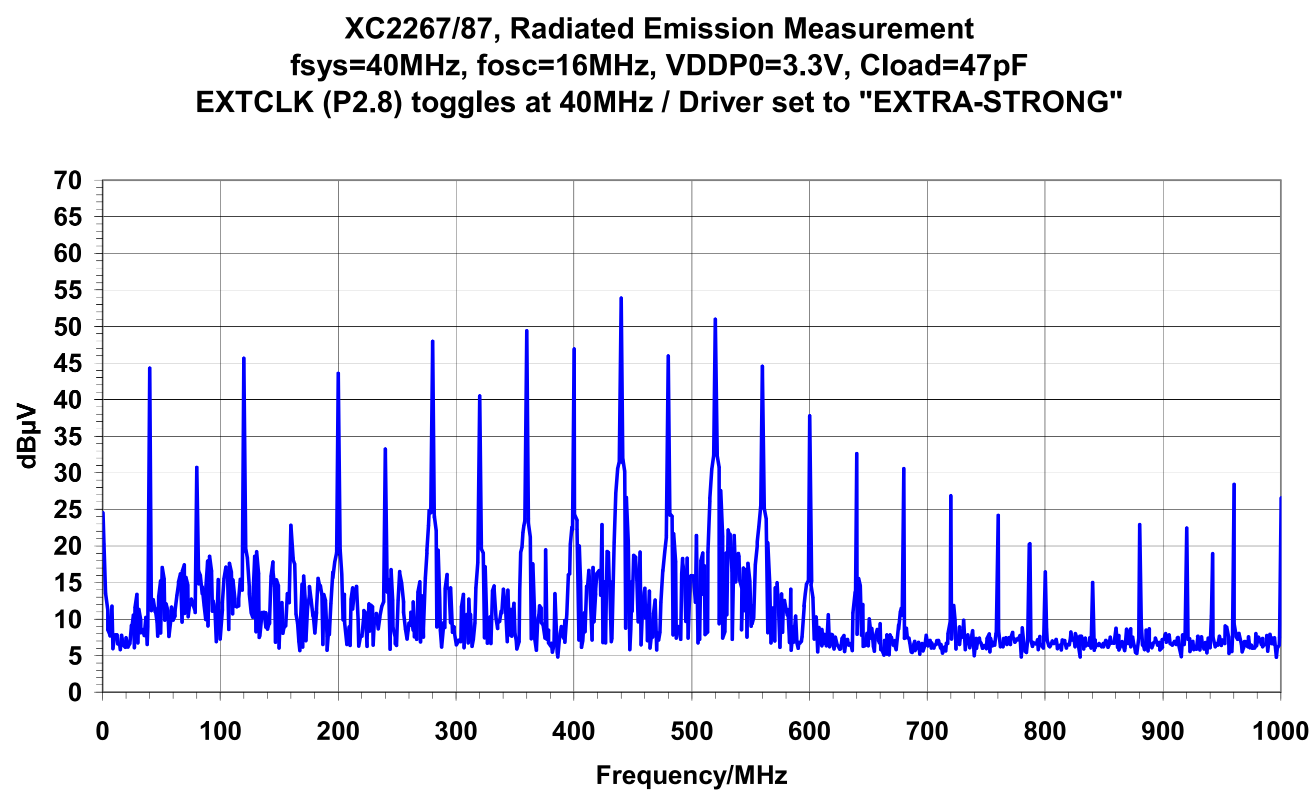

Figure 142: Emission Spectrum for EXTRA-STRONG/40MHz/47pF/3.3V/Radiated

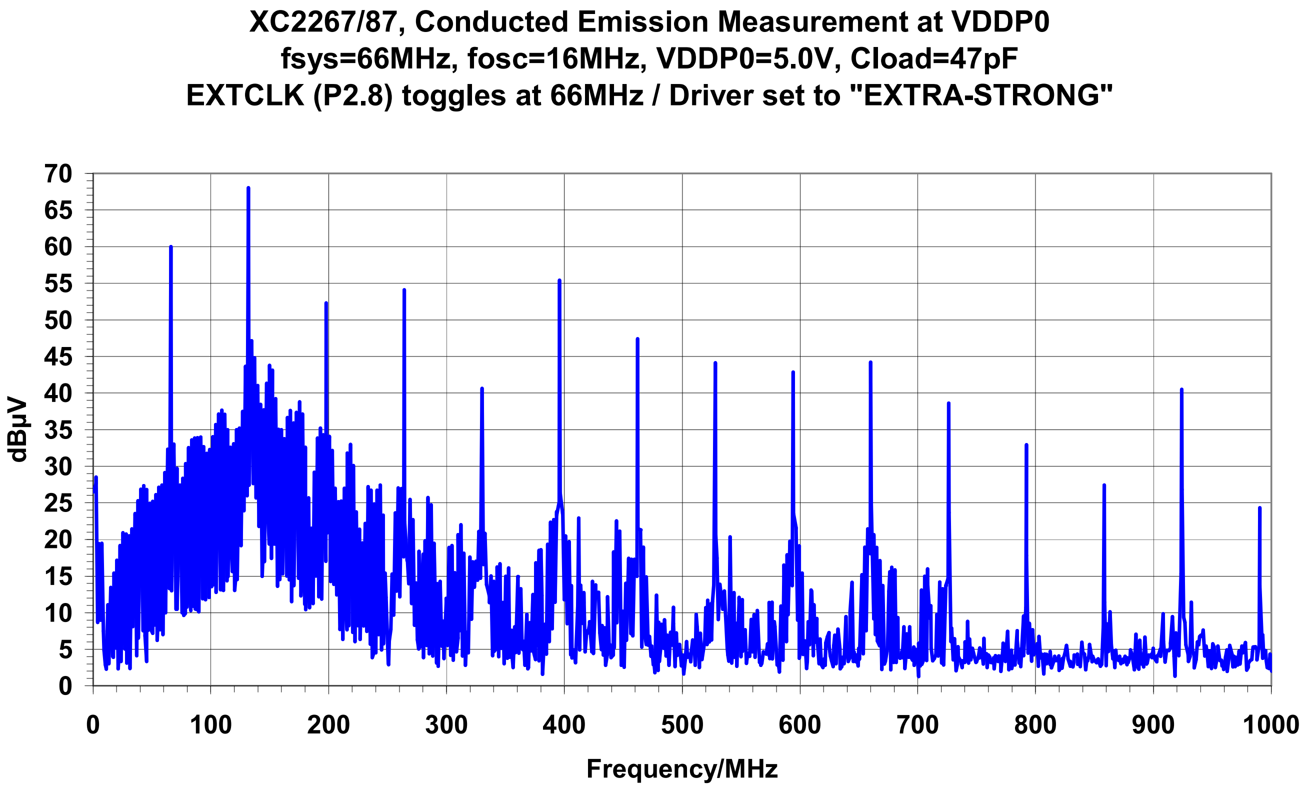

Figure 143: Emission Spectrum for EXTRA-STRONG/66MHz/47pF/5.0V/Conducted

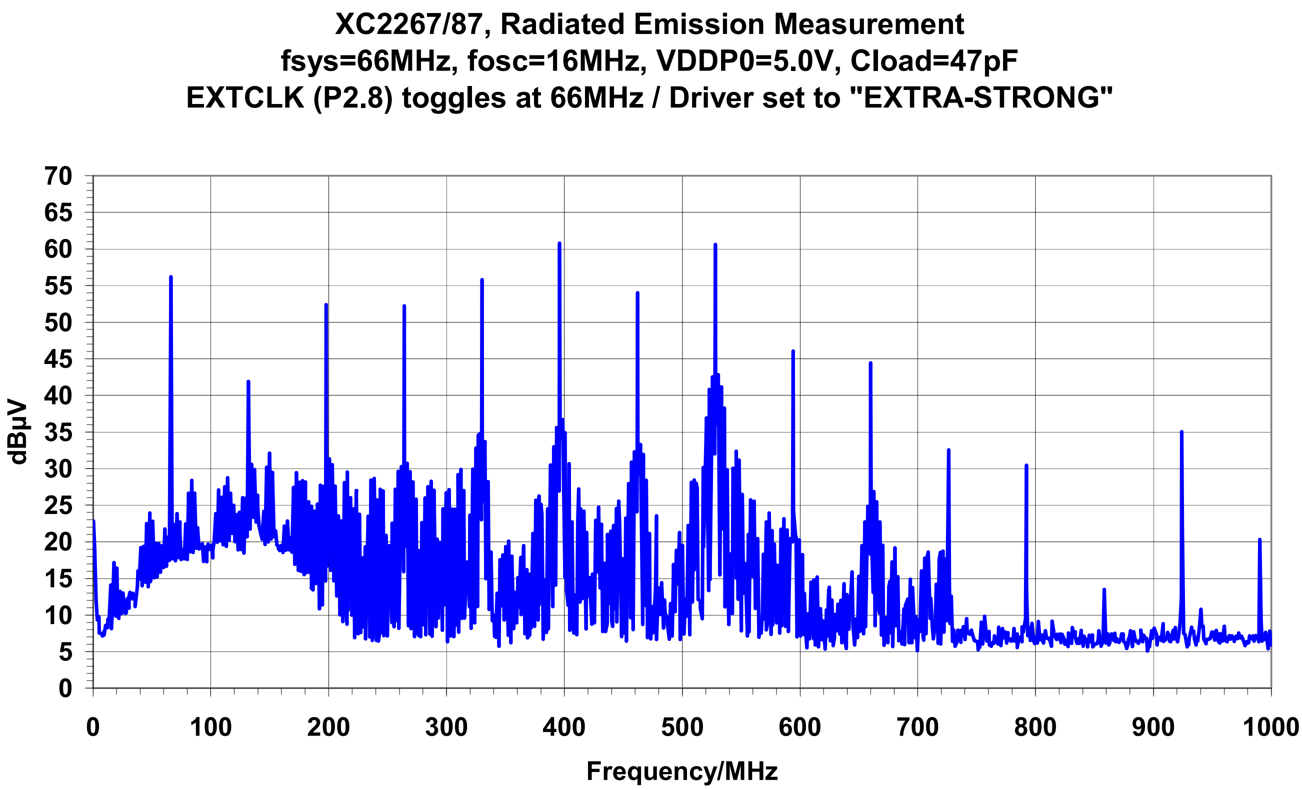

Figure 144: Emission Spectrum for EXTRA-STRONG/66MHz/47pF/5.0V/Radiated

Annex C: Glossary

C_{load}	Load Capacitor	Ideal capacitive load connected to an output driver.
di/dt		Dynamic current over time
EMC	Electromagnetic Compatibility	The ability of an electrical device to function satisfactorily in its electromagnetic environment (“Immunity”) without having an impermissible effect on its environment (“Emission”).
EME	Electromagnetic Emission	→ EMC
EXTCLK	System Clock Output	Strong output driver for the system clock.
GND	Ground	Ground reference of the power supply.
PI	Power Integrity	Good PI means a clean power supply system which is not polluted by switching noise.
SI	Signal Integrity	Good SI means proper signal waveform to fulfill the required data communication.
T_A	Ambient Temperature	Temperature in the direct environment of the IC.
t_F	Fall Time	Time of the falling edge of a signal measured between 10% and 90% of the high level.
t_R	Rise Time	Time of the rising edge of a signal measured between 10% and 90% of the high level.
VDD		Power supply voltage in general.
VDDI		Core supply voltage = 1.5V nominal.
VDDP0		Pad supply voltage = 5.0V or 3.3V nominal.
VSS		→ GND

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