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AP16091

XC164CS

Design Guidelines for XC164CS Microcontroller Board Layout

Microcontrollers

Never stop thinking

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AP16091

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Page	Subjects (major changes since last revision)
1,8,9	Figure1 and Figure 4 updated, Figure 5 inserted

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1 Overview

The XC164CS is a 16-Bit microcontroller in TQFP 100-pin package, which requires a carefully designed PCB regarding electromagnetic compatibility. In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP2426), which gives general design rule information for PCB design, some product-specific recommendations and guidelines for XC164 are discussed here.

1.1 General Information

The microcontroller has two supply domains (2.5V for Core / 5.0V for I/O Pad and ADC), which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain should be made with different traces/planes on a supply layer.

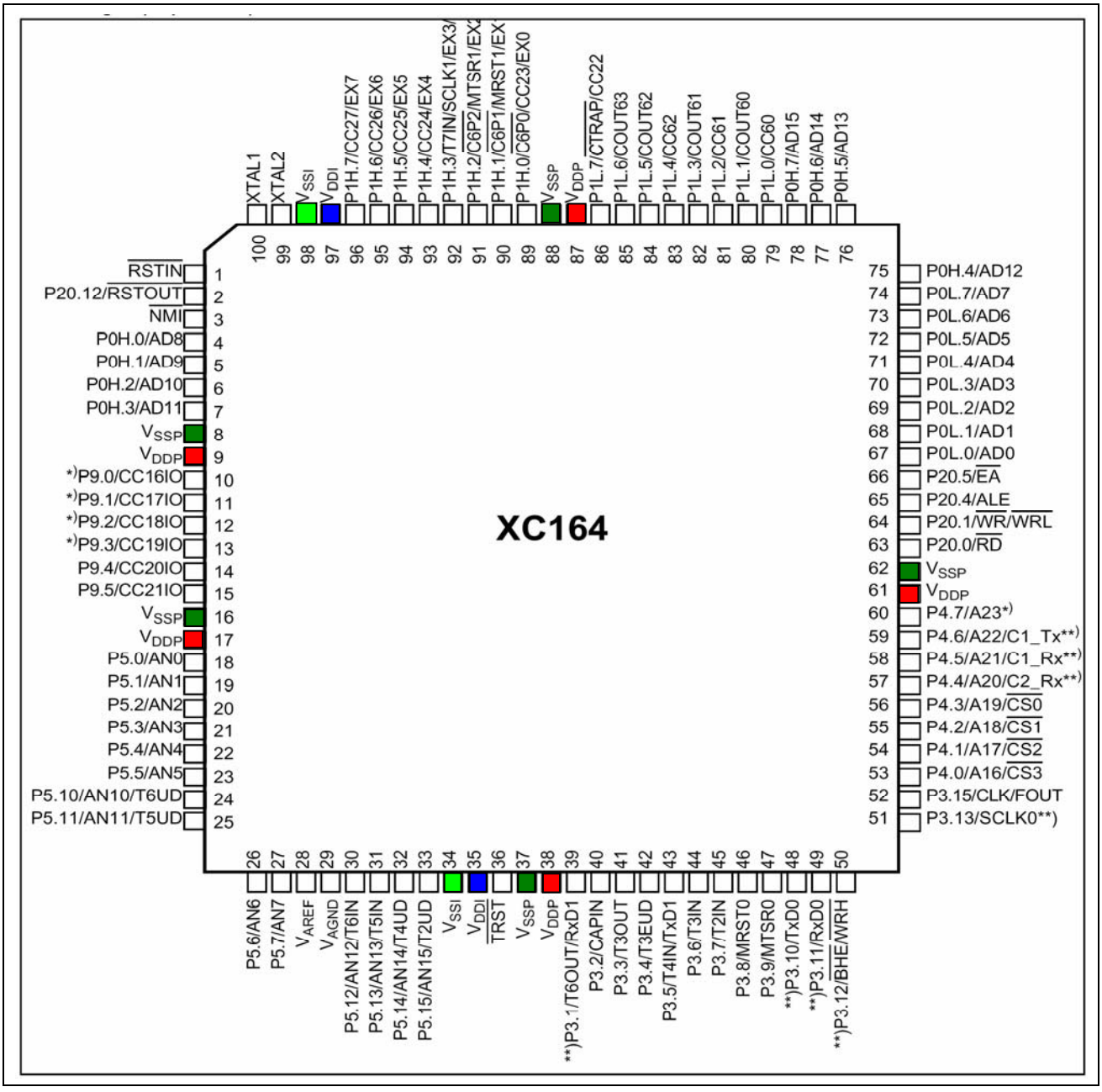

Figure 1 Pinout of XC164

2 PCB Design Recommendations

The layout recommendations are valid for a 4-layer PCB with a GND plane. Following topics are discussed:

- power supply connection from voltage regulator to microcontroller pins including decoupling capacitors,
- oscillator circuit isolation,
- system clock operation,
- layout.

2.1 Power Supply Decoupling Concept

An optimal noise decoupling configuration relies on the fact that the supply current must be forced to flow through the decoupling capacitors, i.e. the capacitors need to be placed directly on the VDD/VSS traces which lead to the micrcontroller´s supply pins. The “hot side” of the capacitors are connected to the supply pins, the “cold side” is connected to the GND plane and to the VDDI (2.5V) or VDDP (5.0V) traces coming from the voltage regulators. Figure 4 shows the required layout structures to realize this configuration. All decoupling capacitors should be placed on the same solder side where the microcontroller is mounted to avoid via hole inductances in the decoupling path. The connection traces to the voltage regulators may be routed in an inner layer. As far as possible, a solid GND plane should be available in an inner layer.

2.2 Oscillator Decoupling Concept

The oscillator switching noise is prevented from being coupled into the GND plane by providing a local VSS system to which the XTAL capacitors and crystal ground are connected. This local VSS is taken from pin 98 (VSSI). Figure 4 shows a sample layout of the local oscillator VSS system.

2.3 System Clock Routing Concept

Operation of the system clock (CLOCK; P3.15) might become critical if not porperly observed. Its I/O driver is basically designed to drive a 50pF load with 40MHz system clock frequency. Connected on-board traces and - even worse - connector cables lead to significantly increased noise emission.

A countermeasure on PCB layout is the introduction of a 180Ω resistor in the CLKOUT trace (eventually followed by a small grounded capacitor). The CLKOUT trace should be routed on an inner PCB layer as stripline to avoid radiation. If the system clock drives a cable, care should be taken on the capacitive load. A separate driver circuit should be provided. A further countermeasure can be taken by software. CLKOUT should be driven as weak as possible. Using the output driver slew rate control features through the special function registers can reduce the driver strength and increase the edge timing. Figure 2 shows that up to 20dB emission reduction can be obtained by using this driver scaling feature.

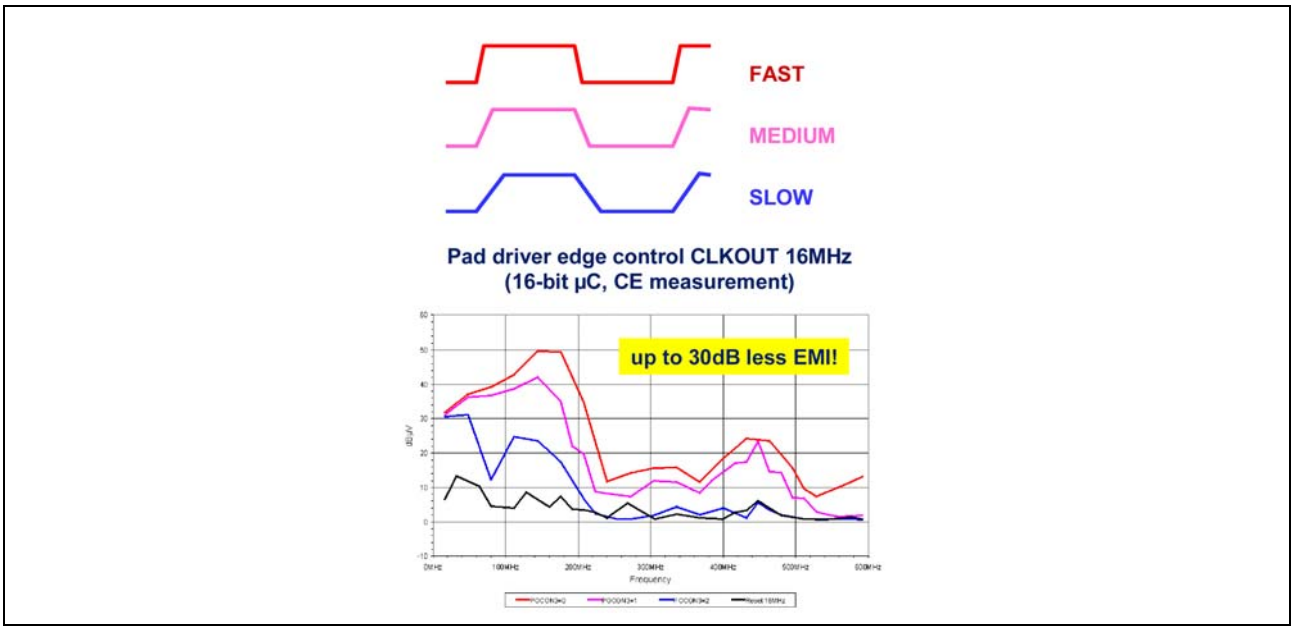

Figure 2 Emission reduction by slew rate control settings for output drivers

POCON*
Port Output Ctrl. Reg.* ESFR (F0xx$_H$/yy$_H$) Reset Value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDM3N				PDM2N				PDM1N				PDM0N			
rw				rw				rw				rw			

Field	Bit	Type	Description
PDMxN	[3:0], x = 0 [7:4], x = 1 [11:8], x = 2 [15:12], x = 3	rw	**Port Driver Mode, Nibble x** **Code, Driver strength[1], Edge Shape[2]** 0000 Strong driver, Sharp edge mode 0001 Strong driver, Medium edge mode 0010 Strong driver, Soft edge mode 0011 Weak driver, Standard edge[3] 0100 Medium driver, Standard edge[3] 0101 Reserved, do not use! 0110 Reserved, do not use! 0111 Reserved, do not use! 1xxx Reserved, do not use!

1) Defines the current the respective driver can deliver to the external circuitry.
2) Defines the switching characteristics to the respective new output level. This also influences the peak currents through the driver when producing an edge, i.e. when changing the output level.
3) No additional edge shaping can be selected at this driver level.

Table 7-1 Port Output Control Register Allocation

Control Register	Address	Controlled Pins (by POCONx.y-z)[1]				Notes
		.15-12	.11-8	.7-4	.3-0	
POCON20	F0AA$_H$ / 55$_H$	P20.12, RSTOUT	---	P20.5-4, ALE	P20.1-0, WR, RD	–
POCON9	F094$_H$ / 4A$_H$	---	---	P9.5-4	P9.3-0	–
POCON4	F08C$_H$ / 46$_H$	---	---	P4.7-4	P4.3-0	–
POCON3	F08A$_H$ / 45$_H$	P3.15-12	P3.11-8	P3.7-4	P3.3-1	–
POCON1H	F086$_H$ / 43$_H$	---	---	P1H.7-4	P1H.3-0	–
POCON1L	F084$_H$ / 42$_H$	---	---	P1L.7-4	P1L.3-0	–
POCON0H	F082$_H$ / 41$_H$	---	---	P0H.7-4	P0H.3-0	–
POCON0L	F080$_H$ / 40$_H$	---	---	P0L.7-4	P0L.3-0	–

1) x denotes the port number, while y-z represents the bitfield range.

Figure 3 Slew rate settings for output drivers

Route critical signals with adjacent ground reference to use as few as possible vias (no reference layer change!). Route them as short as possible. Routing ground on each side can help to reduce coupling to the other signals.

For unused **"Output, Supply, Input and I/O"** pins, the following points must be considered:

1. Supply Pins (Modules) :	- See product specification.
2. I/O-Pins:	• Must be configured as output and driven to static low in the weakest driver mode. • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering).
3. Input Pins with internal pull device:	• For pins with alternate function see product specification to define the necessary logic level. • Must be configured as Pull-down and should activated static low (exception: if the product specification requires high level for alternate functions, then: pull&static high). • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering).

2.4 Layout

A power-plane/grounding concept example for XC164CS with TQFP-100 package can be seen in Figure 4. This layout example shows two supply domains (2.5V, 5.0V), where 2.5V is the core supply, 5.0V is the pad supply voltage. All supply connections are made on the power layer.

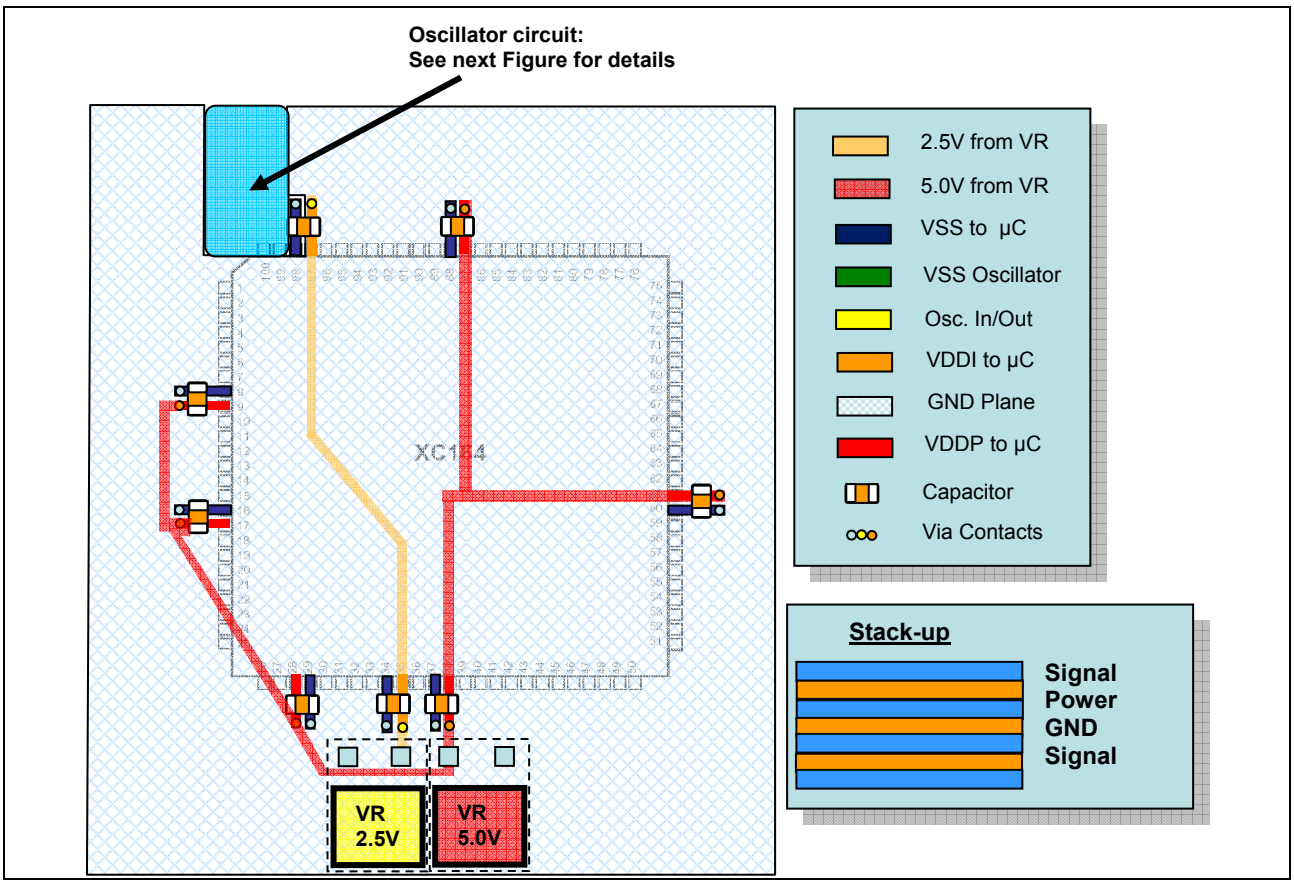

Figure 4 Layout proposal for supply domain routing and decoupling capacitor placement

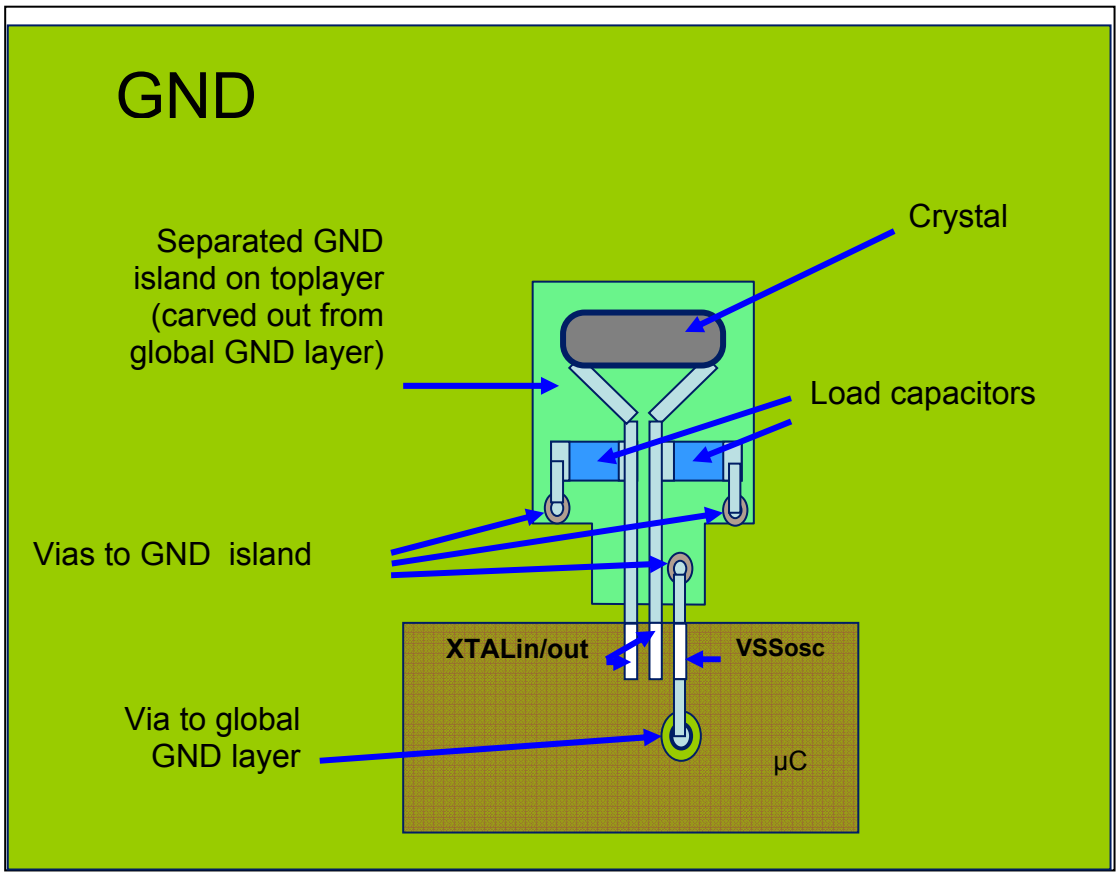

Figure 5 Layout proposal oscillator circuit

The ground system must be separated into two groups:

- Ground for oscillator,
- Ground for digital supply.

A target inductance value of <1.5nH (VDDI), <1.5nH (VDDP) for the connection of decoupling capacitors to the supply pins is required.

Use inductances at regulator output and multilayer ferrite chip beads on supply paths at the branching to the supply pins of IC. Figure 6 shows the benefit of ferrite beads used on supply path to IC pins (measured without any decoupling capacitors). While the emission on the IC side is the same as without ferrites, the emission on the regulator side decreases considerably up to frequencies of 500MHz. Figure 7 shows the characteristics of the ferrite used.

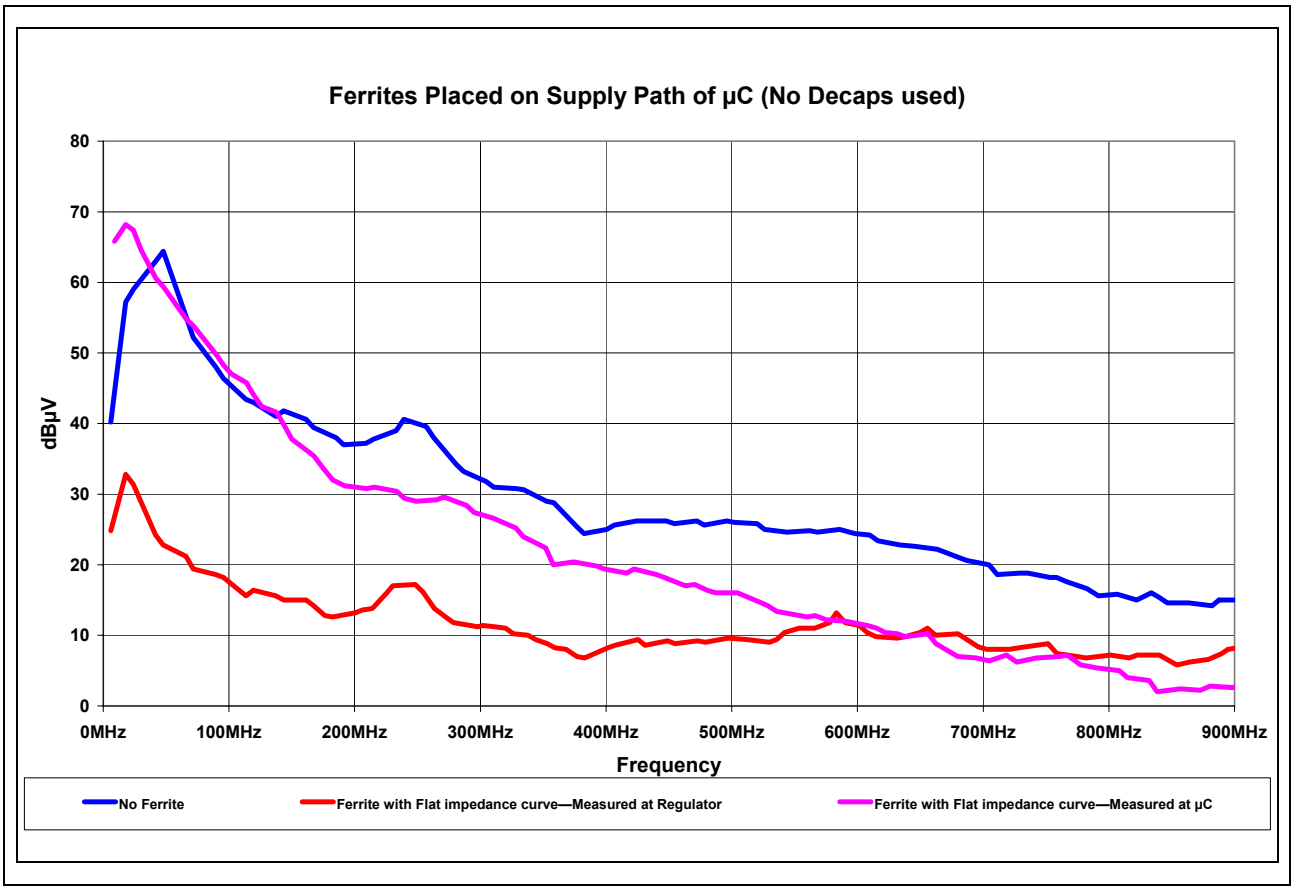

Figure 6 The effect of the ferrites at supply pins of IC

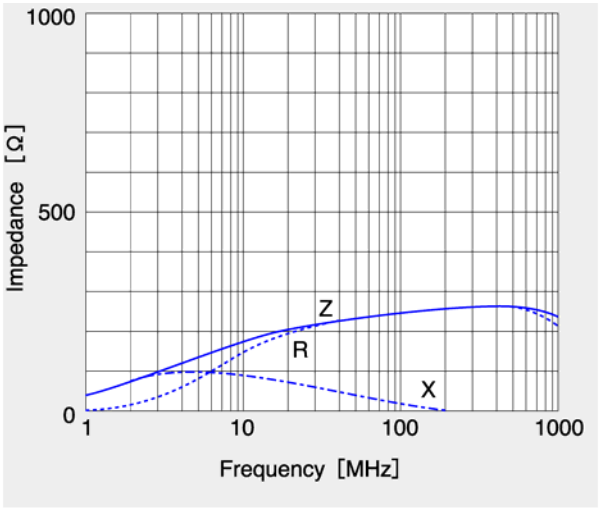

Figure 7 Impedance Characteristics of the multilayer ferrite chip bead

2.4.1 Decoupling Capacitor List

- Type of capacitors:
  - 47nF or 100nF, X7R Ceramic Multilayer (low ESR and low ESL)
- All supply pins should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All capacitors must be placed as close as possible to the related supply pin pair.
- Decoupling capacitor list for layout proposal:
  - Total = 8 x 100nF or (2x100nF and 6x47nF)

Capacitor	Type	Supply	Pins
100nF	X7R	VDDI	97/98
100nF	X7R	VDDI	35/34
47nF or 100nF	X7R	VDDP	9/8
47nF or 100nF	X7R	VDDP	17/16
47nF or 100nF	X7R	VDDP	28/29F
47nF or 100nF	X7R	VDDP	38/37
47nF or 100nF	X7R	VDDP	61/62
47nF or 100nF	X7R	VDDP	87/88

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