

AP16033

C16x

Connecting a Fast External A/D Converter on the CAPCOM-Unit

Microcontrollers



Never stop thinking.

Revision History:		2004-02	V 1.0
Previous Version:		-	
Page	Subjects (major changes since last revision)		
All	Updated Layout to Infineon Corporate Design, updated release to 1.0, Content unchanged!		

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Edition 2004-02

**Published by
Infineon Technologies AG
81726 München, Germany**

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1 Triggering of the ADC

There are particular fast A/D converters (ADC) which are providing a result after three 800ns-cycles and then continuously every 800ns-cycle.

In order to use this ADC the signal as followed has to be generated:

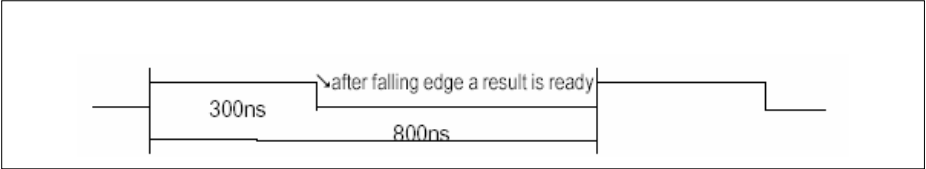


Figure 1 ADC Signal

This signal will be generated with the CAPCOM unit by using the 50ns shift of each channel as followed (see also ApNote "Generation of High Resolution PWM Signals");

There are two internal scanners (parallel running) for the CAPCOM unit for the lower

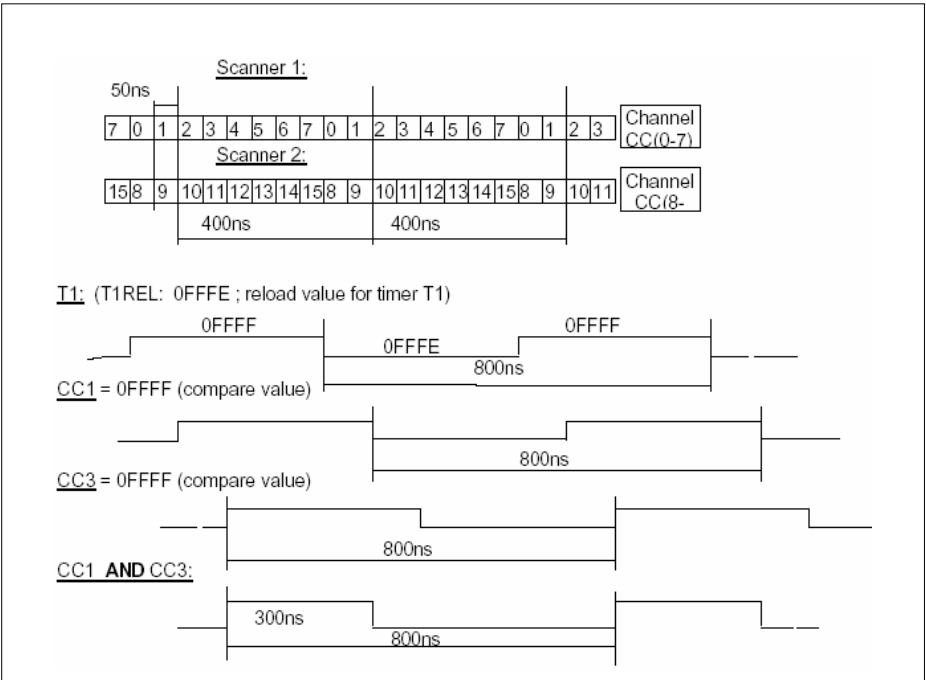


Figure 2 The Scanner 1 (0-7) and the Scanner 2 (8-15)

2 Data transfer of the ADC result

2.1 The Hardware Solution

The external ADC will provide a result after three cycles and then continuously every cycle. After each 800ns cycle there have to be an (external) interrupt to trigger the PEC and transfer the ADC result (8 Bit from a Port) to a location RAM (intern or extern).

The external Interrupt will be generated as followed:

⇒ with the falling edge of CC3 channel.

Now the timing of PEC transfer can be fine tuned by selecting the Capture channel for generating the PEC.

Example: Have the interrupt request flag (IR) set at the beginning at each cycle.

As the previous page shows, the falling edge (CC1) will be generated when the scanner finished channel CC1/CC9. There are additional delays before the Port-pin will actually change its level:

Compare match to Output: 100ns ①

plus the delay , depending on external Port-load (<50ns @100nF Port-load) ④

→ $100\text{ns} + \sim 50\text{ns} = \sim 150\text{ns}$

For the input Capture of signals is only one delay to add on: Sample Pin to Capture IR Setting: 100ns ③

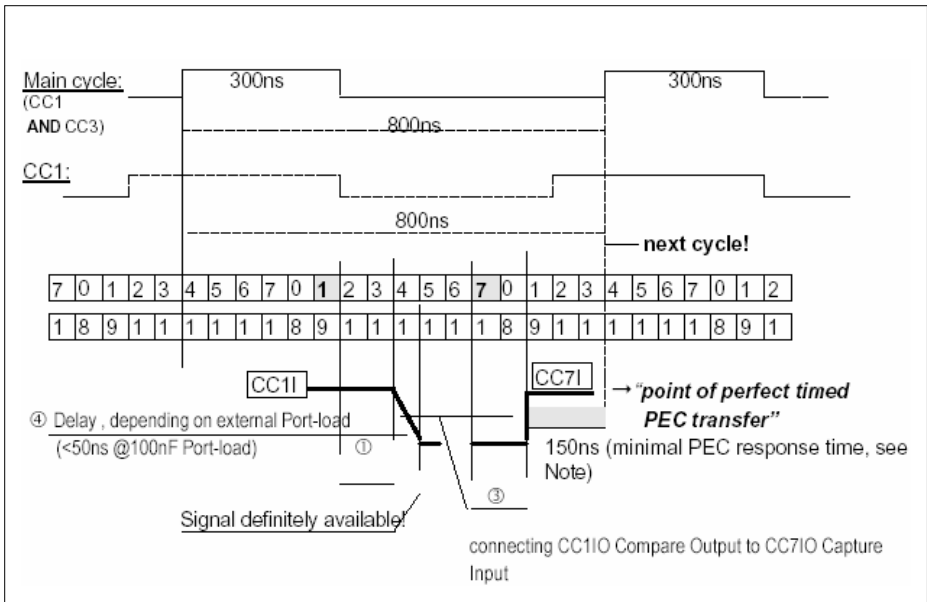


Figure 3 Hardware Solution

As shown in this example, the Interrupt flag CC7IR is set before the next cycle begins!

Now it can be "fine tuned" (by changing the Capture Input Channel) in respect of additional delays caused by the hardware and/or software.

Note: Now you have to add up only the PEC response time as is described in the User's Manual to get the timing for the transfer of the results.

For example: The worst case PEC response time during internal ROM program execution adds to 9 state times (450ns @ 20 MHz CPU clock).

The minimal response is 150ns, this 150ns can be incorporated in the "fine tuning", too.

2.2 The Software Solution

With the following sketch is it an easy way to determine the appropriate Compare Channels for generating the interrupt to trigger the PEC-transfer. Please note that you have to start at the point where do you wish to have the PEC-transfer scheduled ("point of perfect timed PEC transfer").

Data transfer of the ADC result

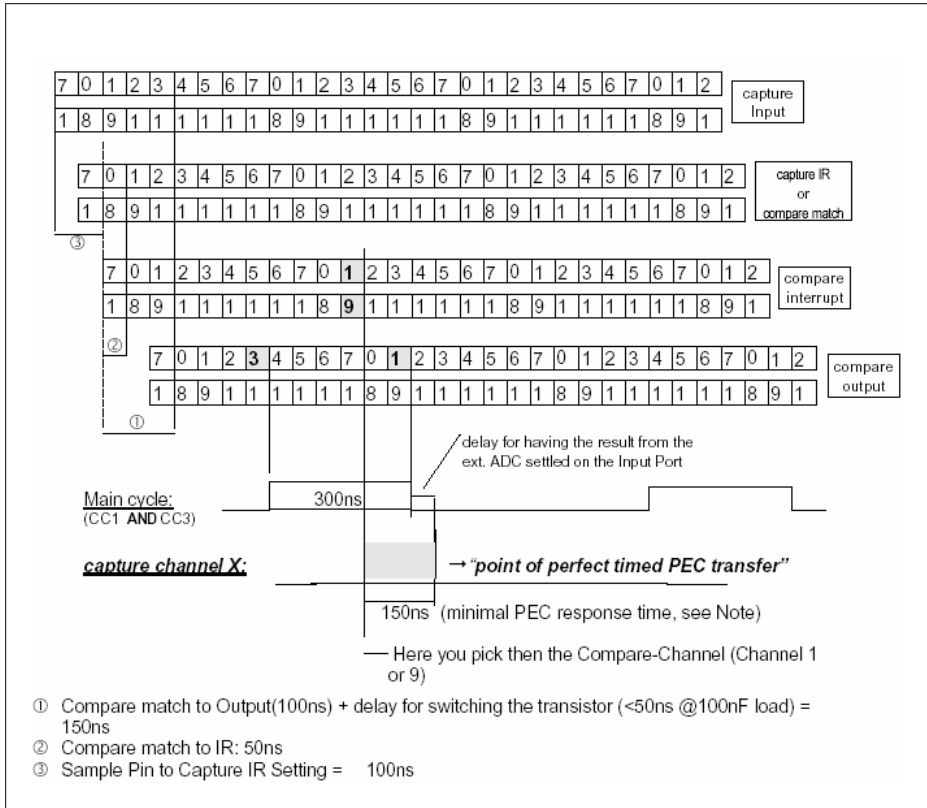


Figure 4 CAP/COM Scan Mechanism Overview

Now it can be “fine tuned” (by changing the Compare-Channel) in respect of additional delays caused by the hardware and/or software.

Note: Now you have to add up only the PEC response time as is described in the User’s Manual to get the timing for the transfer of the results.

For example: The worst case PEC response time during internal ROM program execution adds to 9 state times (450ns @ 20 MHz CPU clock).

The minimal response is 150ns, this 150ns can be incorporated in the “fine tuning”.

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