XC800 Family

AP08110

Design Guideline for XC82x and XC83x Board Layout

Application Note

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Microcontrollers

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XC82x and XC83x
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Page	Subjects (major changes since last revision)
–	First release.

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1 Overview

The XC82x and XC83x are low pin count products of the XC800 Family from Infineon. Because of the minimum number of supply pins, special care with the layout needs to be taken with these products. The correct board layout will help achieve the best ADC performance and EMC behaviour, as well as ensuring the robustness of the RTC-XTAL oscillator.

This document should be read in conjunction with the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule information for PCB design. This application note discusses product specific recommendations and guidelines for the XC82x and XC83x products.

1.1 General Information

The microcontroller has just two supply pins (VDDP and VSSP) to which all internal modules are connected. These are the embedded voltage regulator, the port pins, the ADC module and the RTC-XTAL oscillator in the XC83x.

The performance of the ADC and the robustness of the RTC-XTAL oscillator will be reduced, if core supply noise or pin activity noise are not properly de-coupled.

Proper de-coupling can be achieved by separating the ground traces in analog, digital and oscillator groups. A star point connection should be considered at the pad of the VSSP pin. The ADC reference voltage can be configured as an internal 1.2 V reference, or it can be connected to the VDDP. In the latter case, supply noise directly influences the ADC performance.

The RTC-XTAL oscillator can be disturbed by noise injection from neighboring active pins driving high frequency signals from I^2C, PWM or the LED and Touch Sense unit. Proper PCB layout will reduce the capacitance between those traces to a minimum.

This application note includes layout recommendations for optimized ADC performance and robust RTC-XTAL oscillator operation.

2 Power Supply De-coupling and Improved ADC Performance

There are two different reasons why microcontrollers can cause noise at the power supply. Firstly the synchronous clocked logic functions lead to peak current at the MCU clock frequency. Secondly, pulse pattern and clock output at any port pin will draw current at the pulse pattern's frequency. De-coupling capacitors are intended to buffer the charge needed to feed the required current pulses.

Of course noise at the power supply lines might also disturb the microcontroller. This noise can be filtered by the same de-coupling capacitor. **Figure 1** shows the recommended PCB layout of the de-coupling capacitors.

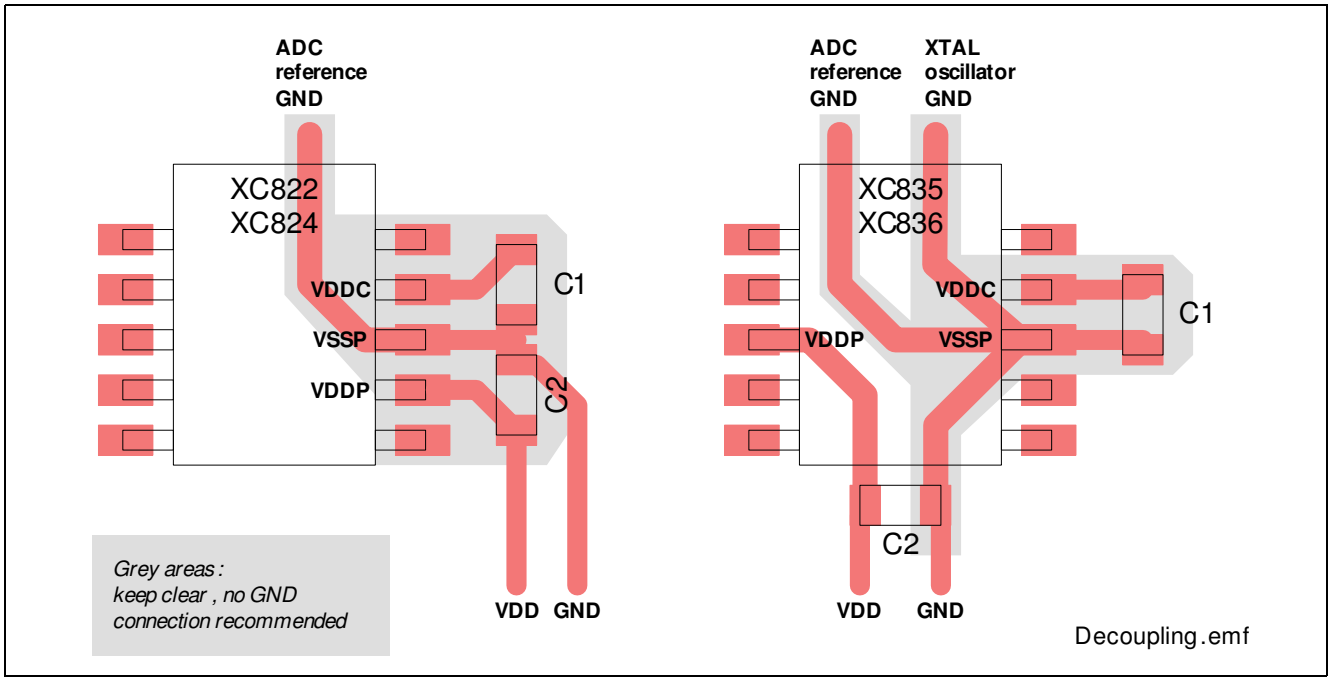

Figure 1 Decoupling Capacitor for Power Supply

The noise of the power supply (VDD and GND) is filtered by the capacitor C2 and provided at the power supply pins VDDP and VSSP.

The core supply pin VDDC is connected to capacitor C1 in order to reduce noise at the ground connection which is caused by the synchronous logic clocked at the MCU frequency. C1 should be set in the range of 220 nF to 470 nF, and C2 in the range of 68 nF to 220 nF. Capacitors with low ESR (type X7R for example) are recommended.

A star configuration at the VSSP pin is the least noisy connection for the ADC reference ground. This connection is best coupled to the ADC's reference voltage ground potential. This is important for minimizing ADC errors.

It must be ensured that the de-coupling capacitors C1 and C2 are placed as close to the pins as possible. It is also important to connect the power supply GND and VDD only at those traces shown in Figure 1. Any additional connection will bypass the decoupling capacitor and will therefore reduce it's effectiveness. The grey areas shown in the figures should be kept clear of any GND connections and GND planes.

The ADC reference GND connection is intended to be utilized in common mode with the ADC's input pins. Any additional connection to the power supply GND will cause supply noise to be injected to the ADC's reference GND.

3 RTC-XTAL Oscillator Pins (XC835 and XC836 only)

The XC83x RTC-XTAL oscillator is designed for low power consumption. As a result, the high impedance input of the crystal oscillator is sensitive to noise. This noise might be caused by port activity from the PWM or I^2C data as well as other periodic port signals. The correct PCB layout will help ensure precise operation of this oscillator.

The RTC-XTAL oscillator signals RTC-XTAL3 and RTC-XTAL4 should not be routed in parallel to any GPIO signals on the PCB, because of the potential parasitic capacitances between the traces. A star configuration should be used for the GND connection. See **Figure 2** for the recommended PCB layout.

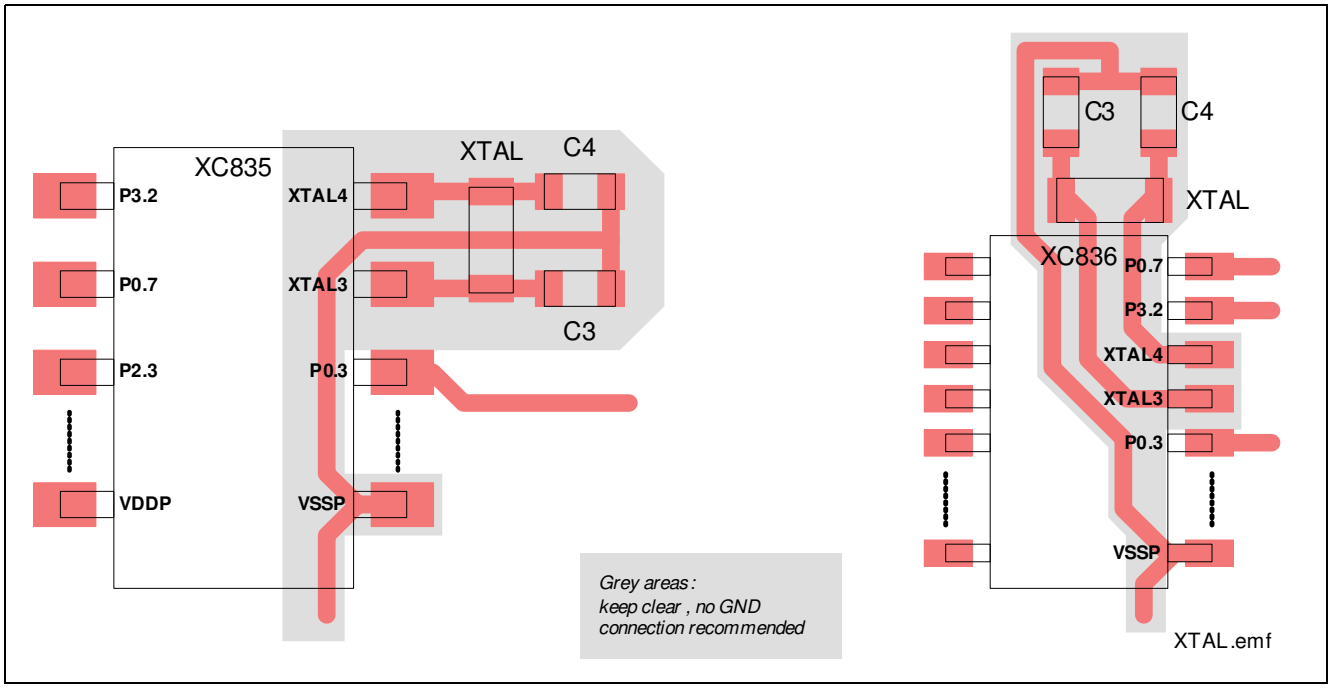

Figure 2 RTC-XTAL and Capacitor Connection

The filter capacitors C3 and C4 should connect directly to the VSSP pin without any additional GND connection. In this arrangement, noise at VSSP is in common mode with the crystal circuitry and does not influence the oscillator's performance or robustness.

The recommendations described in **Chapter 2** are also valid here. Please refer to **Figure 1** for placement of the supply de-coupling capacitor.

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