AP08064

XC866/886/888

Safeguarding the Microcontroller under Out-of-Spec Noise Conditions

8bit

Microcontrollers

Never stop thinking

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XC866/886/888

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Page	Subjects (major changes since last revision)

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1 Overview

When the XC866/886/888 is operated under out-of-spec high noise conditions, in a worst case scenario, it might malfunction though the probability is very low.

Table 1 and Table 2 show extracts of the devices' data sheets on operating condition parameters and input/output characteristics respectively. Out-of-spec high noise conditions refers to these parameter limits being exceeded.

This application note describes the failure mechanisms and the measures that can be taken to further reduce the probability that such a malfunction might occur.

There are altogether two known failure mechanisms:

- Noise on XTAL1/2
- Noise on V_{DDC}

Table 1 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		min.	max.		
Digital power supply voltage	V_{DDP}	4.5	5.5	V	5V devices
Digital power supply voltage	V_{DDP}	3.0	3.6	V	3.3V devices
Digital ground voltage	V_{SS}	0		V	
Digital core supply voltage	V_{DDC}	2.3	2.7	V	
Ambient temperature	T_A	-40	85	°C	SAF-XC8...
		-40	125	°C	SAK-XC8...

Table 2 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions Remarks
		min.	max.		
V_{DDP} = 5V Range					
Input Hysteresis on port pins[1)]	HYS CC	0.08 × V_{DDP}	–	V	XC866 devices
		0.07 × V_{DDP}	–	V	XC886/888 devices
Input Hysteresis on XTAL1[1)]	$HYSX$CC	0.07 × V_{DDC}	–	V	

Table 2 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions Remarks
		min.	max.		
V_{DDP} = 3.3V Range					
Input Hysteresis on port pins[1)]	HYS CC	0.03 × V_{DDP}	–	V	
Input Hysteresis on XTAL1[1)]	$HYSX$CC	0.07 × V_{DDC}	–	V	

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2 Noise on XTAL1/2

The XTAL1 pin supplies the external oscillator input to the XC866/886/888. High noise on XTAL1/2 distorts the external oscillator input and might cause the PLL to lose its lock to the oscillator, resulting in a PLL loss-of-lock condition. The PLL is especially more sensitive to input noise variation under cold temperature (-40°C).

The XC866/886/888 can be made less susceptible to noise by having the following measures in place:

- Optimized external oscillator and foot point capacitors, where the capacitors are as large as possible, for example more than 20 pF for a 8 MHz crystal.
- An optimized printed circuit board (PCB) layout, for example short traces between external oscillator and chip.

Note: If the internal on-chip oscillator is used instead of an external oscillator, noise on XTAL1/2 pins will not result in a PLL loss-of-lock condition nor the subsequent failure scenario.

2.1 Corruption of Program Counter (PC)

From the time PLL detects the loss-of-lock until the time user software performs a loss-of-lock recovery, the system might -- under worst case conditions (for example, at cold temperature) -- run at a higher frequency than specified.

The higher frequency might cause the CPU to fetch code wrongly from the P-Flash, which might in turn result in a corrupted program counter (PC). Therefore, it is recommended that the user software enables PLL NMI (register bit NMICON.NMIPLL = 1) and disconnects the oscillator (set register bit PLL_CON.OSCDISC to 1) once the NMI routine is entered upon a PLL loss-of-lock. Disconnecting the oscillator forces the system to run at the much lower base frequency (10 to 80 MHz) further divided by the K factor.

2.1.1 Unexpected Program Flow

If the PC is corrupted, it might jump to a random piece of code residing in the program memory space and execute the code from there, thus causing the device to enter an unexpected program flow. The Watchdog Timer (WDT) should always be enabled in the user application such that in the event of an unexpected program flow, the WDT will time out and trigger a WDT reset.

In the worst case scenario, the part of the code preceding a Flash erase routine call might be entered. If registers R0-R7 contain non-zero values at this time, the Flash banks and sectors that are selected by these registers and not protected from erase by hardware, will be erased.

To avoid the destruction of Flash contents during such an unexpected program flow, the Flash Erase/Program routines inside the boot ROM include a check for PLL loss-of-lock

(only valid for XC88x devices). In the event of PLL loss-of-lock and the Flash Erase/Program routine being accidentally called, the flash content will still be safe, as the Erase/Program operation will not be started.

Note: For the XC88x devices, the program and erase will not proceed as expected if the PLL NMI flag NMISR.NMIPLL is set. It is important to ensure that the PLL is locked and the PLL NMI flag is cleared before calling the program and erase subroutines.

To increase the level of protection (especially for XC866 devices) the flash hardware protection can be used.

2.1.1.1 Enable Flash Hardware Protection

Two hardware protection modes are provided for Flash to protect against unauthorized code readout and Flash program/erase.

In mode 0, P-Flash is protected from program and erase while D-Flash can only be erased by having the user software to set register bit MISC_CON.DFLASHEN each time before an erase operation.

In mode 1, both the P-Flash and D-Flash are protected from program and erase.

In either modes, selecting the Flash that is protected from program and erase for erase will have no effect.

3 Noise on V_{DDC}

High noise on V_{DDC} pin might cause disturbance on the device's internal logic. For example, the Flash or memory read circuitry or peripherals such as the ADC might be disturbed. Corruption of registers might also occur.

The XC866/886/888 can be made less susceptible to noise by having the following measures in place:

- A large V_{DDC} stabilizing capacitor in the range of 220 nF or more between V_{DDC} and V_{SSC}.
- An optimized PCB layout, for example short traces between capacitor, V_{DDC} and V_{SSC} pins.

3.1 Corruption of Program Counter (PC)

The disturbance of the Flash or memory read might also corrupt the PC and cause the device to enter an unexpected program flow. The consequences and measures to be taken are similar to those described for the PLL Loss-of-Lock (see **Section 2.1.1** and **Section 2.1.1.1**).

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