



Microcontrollers

ApNote

AP0845

Changing from the C517A-LxM to the C509-LM

This document describes things that must be considered when changing from the ROMless P-MQFP C517A-LxM to the ROMless P-MQFP C509-LM. The C509 has several features that the C517A does not have. This document does not describe all of the advantages and additional features of the C509. This document only focuses on the differences which will produce incompatibilities when switching from the old C517A to the C509.

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1 Introduction.....3

2 Major Differences3

2.1 C509 has One Fewer Clock Prescaler.....3

2.2 Timer Prescalers.....3

2.3 A/D Converter Prescalers4

2.4 MDU-Error Flag Mechanism5

2.5 Normalizing with the MDU6

2.6 Slowdown Mode Errata.....6

2.7 C509 has more Power and Ground Pins6

2.8 PRGEN Pin.....7

3 Minor Differences (for your reference)7

3.1 External Data Space.....7

3.2 Vcc Minimum Value.....7

3.3 Different Current Consumption7

AP0845 ApNote - Revision History		
Actual Revision : Rel.02		Previous Revision: Rel.01
Page of actual Rel.	Page of prev. Rel.	Subjects changed (since last release)
7		Added 2.8 PRGEN Pin

1 Introduction

This document is intended to aid those who intend to switch from the ROMless P-MQFP C517A-LxM to the ROMless P-MQFP C509-LM. The P-MQFP versions of the C517A-LxM have been discontinued and the closest P-MQFP replacement for the device is the C509-LM. If switching to the P-LCC package is an option, then the C517A-LN might also be considered.

2 Major Differences

There several major differences between the C517A and the C509 that should definitely be accounted for while changing to the C509-LM.

2.1 C509 has One Fewer Clock Prescaler

The standard 8051 type microcontroller (including the C517A) has a 1:12 ratio between instruction cycles and external oscillator cycles. So for every 12 external oscillator periods, one instruction cycle is executed by the microcontroller. The C509 has one less prescaler on the oscillator circuitry so it has a 1:6 instruction to oscillator cycle ratio. This means that with the same external oscillator, the C509 will operate with double the performance of the C517A.

To ensure ensure compatibility to the C517A, the C509 must be operated with an external oscillator that is $\frac{1}{2}$ that of the C517A. The maximum operating frequency of the C509 is limited to 16 MHz. This is equivalent to the C517A operating at 32 MHz.

2.2 Timer Prescalers

The C509 was developed as a higher performance upgrade to the C517A. It was developed so that C517A users could easily switch to the C509 to gain more performance with minimal software changes and without increasing the oscillator frequency. However, since the instruction cycle time (which is the time base for the timers) of the C509 was decreased by a factor of two, all of the timers will operate twice as fast. One of the goals of the C509 was to increase the CPU performance while keeping the timers operating at the same frequency as they were in the C517A.

To get around this problem several new bits were introduced into unused SFR locations. These bits by default are set so that the timers and counters are slowed down by a factor of 2. This allowed the C517A users to switch to the C509 and use the same external oscillator and get increased CPU performance while making little or no changes to their timer software.

The goal of this document is somewhat different. The goal of this document is to ensure compatibility not to increase performance. The best way to ensure compatibility is to make sure that instructions in the C509 take the same amount of time as they did in the C517A. This is done in section 2.1 by decreasing the external oscillator frequency by a factor of 2. It is also important that the timers operate at the same speed as they did in the C517A. To do this you must undo the effects of the extra bits in the SFRs so that the timers are not

operating at $\frac{1}{2}$ the required frequency. So, after decreasing the oscillator frequency as described in section 2.1, the only thing left to do is add some initialization code so that the timers operate at the expected frequencies. The following table lists the timers and bits that require modification in the start-up code:

Timer	Extra Prescaler Bit(s)	Reset Value	Value for Compatibility
Clock Output Pin (P1.6/CLKOUT)	SYSCON.7 (CLKP)	1	0
Timer 0	PRSC.0 (T0P0)	1	0
	PRSC.1 (T0P1)	0	0
Timer 1	PRSC.2 (T1P0)	1	0
	PRSC.3 (T1P1)	0	0
Timer 2	PRSC.4 (T2P0)	1	0
	PRSC.5 (T2P1)	0	0
USART (Serial Channel 0)	PRSC.6 (S0P)	1	0
UART (Serial Channel 1)	S1CON.6 (S1P)	1	0
Watchdog Timer	PRSC.7 (WDTP)	1	0
Compare Timer	CTCON.6 (CTP)	1	0
A/D Converter*			

* The A/D Converter has additional timing differences. See Section 2.3 for details.

So to ensure timing compatibility with the C517A in addition to using an oscillator that is $\frac{1}{2}$ the frequency, the SFR bits in the table above should also be cleared.

2.3 A/D Converter Prescalers

The A/D converter of the C509 has been enhanced. The C509 A/D converter gives you the ability to individually program the clock prescalers for the conversion time and the sample time. The C517A has only one selectable prescaler for A/D converter and it is used to adjust the total conversion time. The new C509 A/D converter is much more flexible.

The C517A had only one prescaler selection bit (ADCL in the ADCON1 register) for adjusting the total conversion time. The C509 has 4 prescaler selection bits (ADCL1, ADCL0, ADST1 and ADST0 in the ADCON1 register) for adjusting the conversion time and the sample time.

C517A Register: ADCON1 Address: 0xDC Rest Value: 0XXX0000B

ADCL	-	-	-	MX3	MX2	MX1	MX0
.7	.6	.5	.4	.3	.2	.1	.0

C509 Register: ADCON1 Address: 0xDC Rest Value: 01000000B

ADCL1	ADCL0	ADST1	ADST0	MX3	MX2	MX1	MX0
.7	.6	.5	.4	.3	.2	.1	.0

The bit ADL0 (ADON1.6) in the C509 has the equivalent function of the bit ADCL (ADCON1.7) in the C517A if the other 3 prescaler bits (ADCL1, ADST1 and ADST0) are programmed to zero. The table below shows how the bits in the C509 should be set to mimic the timing of the C517A (assuming that the C509 is running at ½ the oscillator frequency as described in section 2.1).

C517A Setting	Equivalent C509 Setting			
ADCL	ADCL1	ADCL0	ADST1	ADST0
0	0	0	0	0
1	0	1	0	0

To make the C509 A/D converter timing behave the same as the C517A, software modification is required. Also, notice that the reset value of the ADCL bit in the C517A is 0, but the reset value of the ADCL0 bit is 1. For more information see Chapter 6.6 in the C509 Users Manual. The latest version of the C509 Users Manual can be found on the web at :

<http://www.infineon.com/micorcontrollers>

2.4 MDU-Error Flag Mechanism

The DB-step of the C509 has an errata with the error flag mechanism. This is an errata and may be fixed in future revisions of the device.

The error flag is used to indicate that the MDU has been tampered with while in the performing an operation. This flag is not functional in the DB-step of the C509. This flag is set when any of the registers MD0-MD5 or ARCON are read or written to while a multiply, divide, normalize or shift operation is underway. To correct for this problem your software

should insure that these registers are undisturbed (including potential disruptions from interrupts) until the calculations are complete.

You should check to see if the current step of the device still has this errata.

The errata sheets can be found on the web at:

<http://www.infineon.com/products/micro/applicat/3413.htm>

2.5 Normalizing with the MDU

The MDU of the DB-step of the C509 has an errata when performing normalizing operations. This errata may be fixed in future steps. The MDOV flag in the ARCON SFR (address 0xEF) is used for detection of the MSB MD3.7 in the SFR MD3 (address 0xEC). The MOV flag is not always set when it should be.

To work around this problem, the bit MOV should be set by software after the normalize operation if bit MD3.7 was set prior to the normalize operation.

You should check to see if the current step of the device still has this errata.

The errata sheets can be found on the web at:

<http://www.infineon.com/products/micro/applicat/3413.htm>

2.6 Slowdown Mode Errata

The power saving Slowdown mode is not available on the C509 DB-step. This is an errata and may be fixed in future steps. If your software enables slowdown mode, then you will need to make modifications.

You should check to see if the current step of the device still has this errata.

The errata sheets can be found on the web at:

<http://www.infineon.com/products/micro/applicat/3413.htm>

2.7 C509 has more Power and Ground Pins

The C509 has 4 pairs of power and ground pins (5 pairs if you count the analog reference and ground). The C517A has only 2 pairs of power and ground pins (3 pairs if you count the analog reference and ground).

The extra power and ground pins are all located at pins that are N.C. (No Connection) on the C517A. The extra power and ground pins are also internally connected, so the C509 will operate if it is only fed from the 2 power pairs that the C517A use.

THE C509 WILL WORK ON A C517A PCB IF THE C517A PINS 28, 29, 88 and 89 (MARKED N.C.) ARE NOT CONNECTED ON THE PCB.

2.8 PRGEN Pin

The PRGEN pin (pin 25) on the C509 controls the activation of the bootstrap loader. For compatibility to the C517A, this pin should be tied to Vss. Pin 25 on the C517A is marked N.C.

3 Minor Differences (for your reference)

There are several other minor differences which are likely not to effect most existing designs. However, these items should be checked just to make sure that no software or hardware changes are needed.

3.1 External Data Space

The C517A has 2k of XRAM. When the XRAM is enabled, the external address range from 0xF800 to 0xFFFF is not available for external data memory.

The C509 has 3k of XRAM. As a result, if XRAM is enabled, addresses from 0xF400 to 0xFFFF cannot be used to for external data memory. This difference will only be apparent for C517A users who use XRAM and external data memory from address 0xF400 to 0xF7FF.

3.2 Vcc Minimum Value

The minimum value for Vcc on the C509 is 5V - 5% (or 4.75V). The minimum value for Vcc on the C517A is 5V – 15% (or 4.25V).

3.3 Different Current Consumption

The current consumption of the C509 very similar to that of the C517A. It is slightly lower in Active Mode and slightly higher in Idle Mode. The following table shows the difference in the maximum current consumption formulas for the ROM and ROMless devices:

Mode	Device	Formula
Active	C517A	$1.4 * f_{osc} + 4.0$
	C509	$3.1 * f_{osc} + 0.2$
Idle	C517A	$0.7 * f_{osc} + 3.6$
	C509	$1.8 * f_{osc} + 1.8$

All fosc values are in MHz. Results are in mA.

The table above can be a little misleading. You must remember that the C509 operates with ½ the oscillator frequency of the C517A. When you take this into account the current consumption values are very close.