Microcontrollers

ApNote AP0843

Changing from the 80C537-N to the C517A-LN

This Application Note describes things that must be considered when changing from the ROMless P-LCC 80C537-N to the ROMless P-LCC C517A-LN. The C517A has many more features such as XRAM and more PWM capabilities. This document does not describe all of the advantages and additional features of the C517A. This document only focuses on the differences which will produce incompatibilities when switching from the old 80C537 to the new C517A.

Author: M. Copeland / Microcontroller Applications

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AP0843 ApNote - Revision History		
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1 Introduction

This ApNote is intended to aid those who intend to switch from the old ROMless PLCC 80C537-N to the new C517A-LN. Switching from the 80C537 to the C517A is not difficult, however some people may become confused since this represents a two step jump as shown in Figure 1.

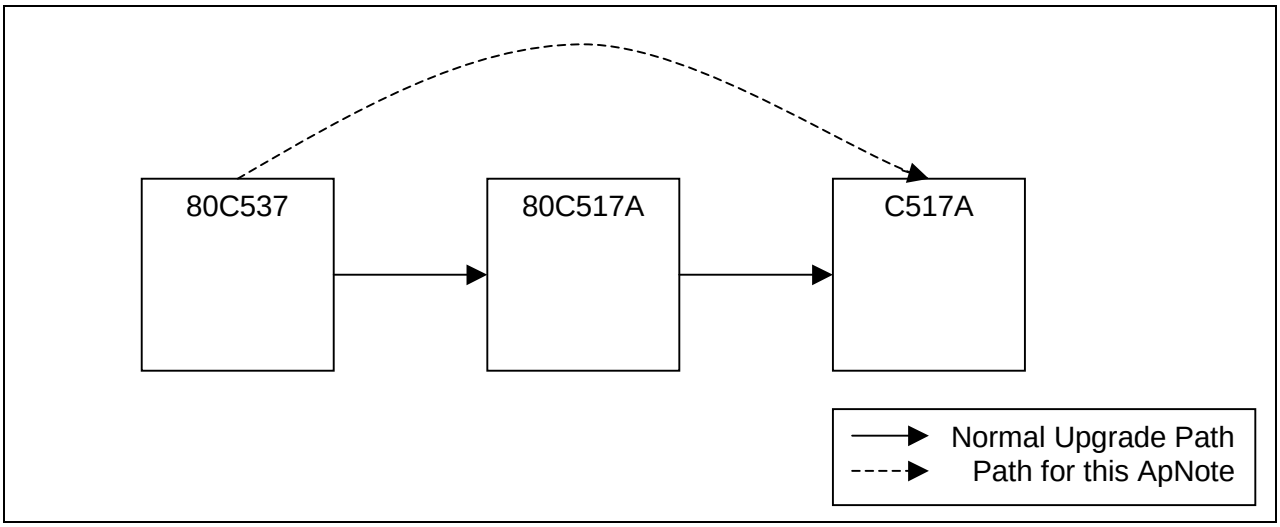


Figure 1:
Upgrade Paths

The 80C537 was introduced first. Some time later, the enhanced 80C517A was introduced, however the 80C537 continued to be produced so nobody was forced to upgrade. The differences between the 80C517A and the C517A-LN are relatively minor. This ApNote is concerned with the slightly more difficult upgrade from the 80C537 to the C517A-LN.

2 Major Differences

There are a couple major differences between the 80C537 and the C517A-LN should definitely be checked before using the C517A-LN.

2.1 Hardware Powerdown Mode of the C517A-LN

The C517A-LN has a hardware powerdown mode. This new feature allows an external device to place the C517A into a powerdown mode. A low level on pin 60 (/HWPD) will cause the hardware powerdown mode to become active. The /HWPD pin does not have an internal pull-up resistor, so if the pin is left floating, there is a high likelyhood that the hardware powerdown mode will become actived (perhaps intermittantly).

To ensure complete compatibility to the 80C537, pin 60 of the C517A must be tied to Vcc. Unfortunately pin 60 on the 80C5x7 is normally tied to Vss. So if you tried to directly replace an 80C537 with a C517A-LN, the device will remain in powerdown mode. In order to use the C517A as a replacement the PCB will need to be altered so that pin 60 is tied to Vcc instead of Vss (see Figure 2).

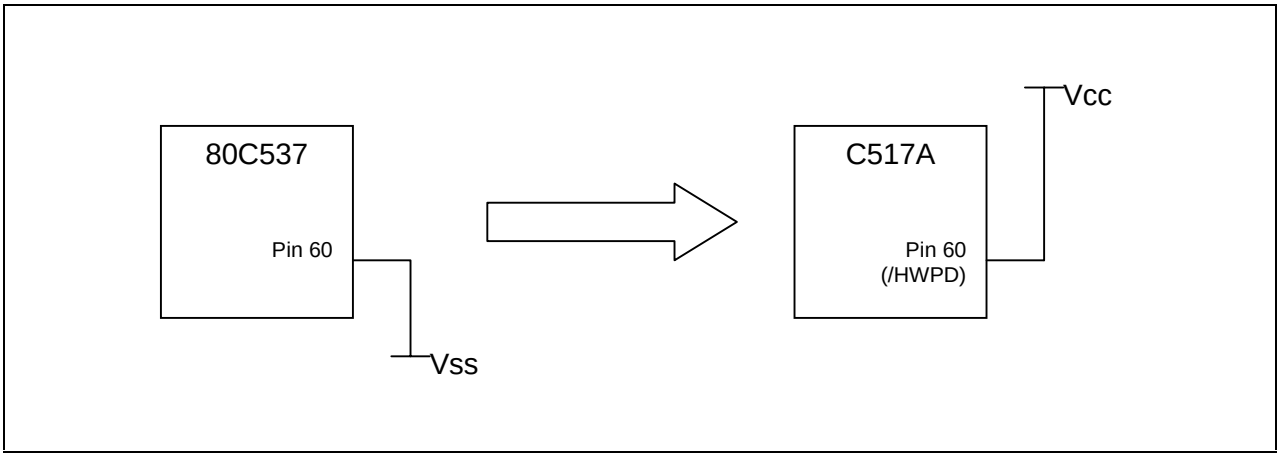


Figure 3:
Pin 60 (/HWPD) MUST be tied to Vcc

2.2 New 10-Bit A/D Converter

The C517A has a new faster 10-bit A/D converter. The old 80C537 has an 8-bit A/D converter. To get more than 8-bits of accuracy from the A/D converter you could “zoom-in” on the voltage by adjusting the reference voltage using the DAPR register. Writing to the DAPR register would also cause the A/D conversion to start. To get high resolution A/D conversion with the old 80C537, you would need to do two conversions. The first conversion would tell you the value with an 8-bit resolution. The reference voltage could then be adjusted and a more accurate reading could be made.

With the new C517A, the DAPR (at address 0xDA) register has been replaced by the ADDATL register (also at address 0xDA) which contains the least significant 2-bits of the conversion. Writing any dummy value to the ADDATL register will cause the conversion to begin. The most significant 8-bits of the conversion are located in the register ADDATH (at address 0xD9) which is located at the same address as the old ADDAT register in the 80C537.

The new 10-bit A/D converter is functionally compatible to the old A/D converter as long as you were writing a 0x00 to the DAPR register to start the A/D conversion. However if you were using the “zoom-in” feature by using DAPR to adjust the reference voltage, then you will probably need to adjust your software so that the C517A can be used.

2.3 New Capacitor Values for the Crystal Oscillator Circuit

When using a crystal oscillator as the clock for the 80C5x7, it is recommended that the external capacitors (connected between the crystal outputs and ground) be 30 pF ± 10 pF. The recommended capacitor values for the C517A is 20 pF ± 10 pF.

2.4 4-bit (or more) Shift Operation using the MDU

The MDU of the 80C537 and C517A allows you to do a 4 bit (or more) shift (right or left) operation. The shift operation is initiated by writing to the ARCON register. In the 80C537 the result of the shift operation (stored in the MD0-3 registers) could be read by the instruction that followed the write to the ARCON register as demonstrated in the following assembly code:

80C537:

```
•
•
•
        MOV     ARCON, #0x04        ;Start the 4 bit Shift Operation
        MOV     R0, MD0             ;Start using the result
•
•
•
```

The C517A requires at least one machine cycle delay between the time the ARCON register is written to and the time the result is read. This delay can be achieved by placing one instruction between the instruction that writes to ARCON and the instruction that reads the result. The inserted instruction can be any valid instruction (including a NOP). The following example shows one way to modify the code above to work with the C517A:

C517A-LN:

```
•
•
•
        MOV     ARCON, #0x04        ;Start the 4 bit Shift Operation
        NOP                         ;Delay 1 machine cycle
        MOV     R0, MD0             ;Start using the result
•
•
•
```

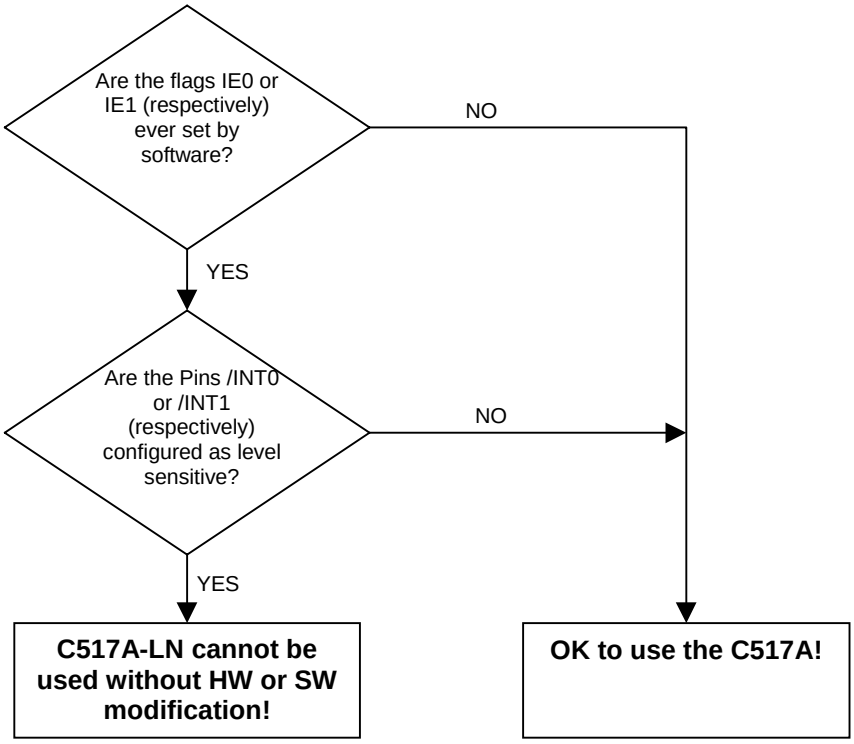
If a C compiler that utilizes the MDU of the C517A-LN is used, the assembly listing should be generated and checked to insure that the one instruction delay is present. If the C compiler calls a library function that uses the MDU, then the compiler vendor should verify that the code will be valid for the C517A-LN. **The Keil C51 compiler WILL work with both devices!**

3 Minor Differences (for your reference)

There are several other minor differences which are likely not to effect most existing designs. However, these items should be checked just to make sure that no software changes are needed.

3.1 Software Generated External Interrupts

The 80C537 and C517A have 6 external interrupt pins. Two of these external interrupt pins (/INT0 and /INT1) can be configured to be either level sensitive or falling edge triggered. The external interrupt flags (IE0 and IE1) can also be set by software to cause the ISRs for /INT0 and /INT1 to be executed. In the 80C537 software could cause external interrupts when the pins /INT0 and /INT1 were configured as level sensitive or falling edge triggered. The C517A only allows external interrupts 0 and 1 to be generated by software when the pins /INT0 and /INT1 are configured as falling edge triggered. The flowchart below is an easy way to tell if this change will effect you:

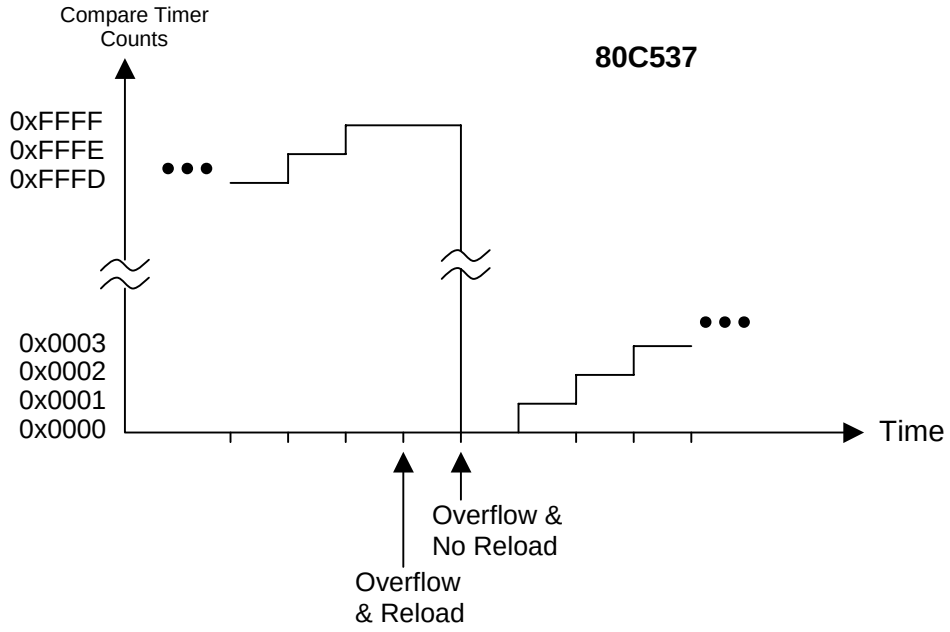


3.2 USART

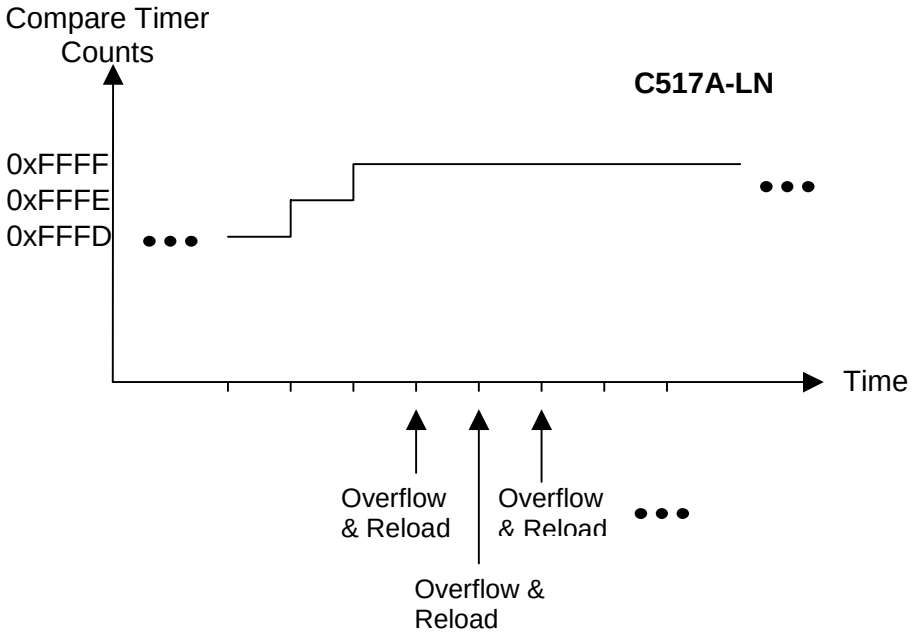
The USART of the C517A is functionally equivalent to the USART of the 80C537 with the exception of one small detail which will probably not effect many (or any) users. The delay from the time that SBUF is written to until the “start-bit” appears at the TxD pin can be up to one bit-time longer in the C517A than the 80C537.

3.3 Compare Timer Reload Behavior

The 16 bit compare timer of the 80C537 and C517A can be reloaded with a 16 bit value (stored in the CTREL registers) after the timer overflows. This reload value can be any 16 bit number. In the 80C537, if the reload value was set to 0xFFFF (an unusual condition), the timer would take on the following values:



The C517A does a much better job at maintaining its count value when the reload value is 0xFFFF:



This change will probably not effect many users, but should be kept in mind.

3.4 Lower Current Consumption

The C517A-LN uses less current! The following table shows the difference in the maximum values for Icc between the 80C537 and the C517A at 16 MHz:

	C517A-LN	**80C537**	**Difference**
Active Mode	26.4	52.3	**25.9**
Idle Mode	14.8	19	**4.2**
Active Mode with Slowdown	12.5	19	**6.5**
Power-Down Mode	0.050	0.050	**0.0**

3.5 New Oscillator Watchdog Circuit

The C517A has a new oscillator watchdog circuit. The new circuit is functionally equivalent to the old 80C537 circuit. The new oscillator watchdog holds the device in reset up to 1 ms longer than the 80C537 if a temporary crystal failure is detected. This additional time is used to make sure that the external crystal has time to stabilize before the device is released from reset. The new oscillator watchdog resets the device if the frequency drops below 600 kHz. The old 80C537 oscillator watchdog reset the device if the frequency dropped below 300 kHz.

The new internal RC oscillator that feeds the oscillator watchdog is also used during reset to provide a “Fast Internal Reset after Power-On”. This ensures that the microcontroller

has achieved a proper reset state after a maximum of 34 µsec after power has been applied to the device.