

AP0803620

XC866

Optimized Space Vector
Modulation and Over-modulation
with the XC866

Microcontrollers



Never stop thinking.

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Page	Subjects (major changes since last revision)		
Many	Updated for the XC866		
SW	Updated for the XC866, Uses DAvE and C/Assembly mix		

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1 Introduction

This Application Note shows how the CAPCOM6 module found in many Infineon 8, 16 and 32-bit microcontrollers can be used to implement space vector modulation for three-phase voltage control inverter applications. A simple algorithm for overmodulation is also demonstrated. The algorithms of this application note are implemented on the Infineon XC866 8051 based 8-bit microcontroller.

Space Vector Modulation (SVM) is a method of producing 3-Phase sinusoidal voltages. The primary use for SVM is in motor control applications (mainly for induction and brushless DC motors). However SVM can also be used in Uninterruptible Power Supply (UPS) applications. SVM is popular because it generates higher voltages with low total harmonic distortion than traditional sinusoidal PWM techniques. Another advantage of SVM is that it works very well with field oriented (vector control) schemes for motor control.

Figure 1 shows a typical motor control application where this Application Note could be useful.

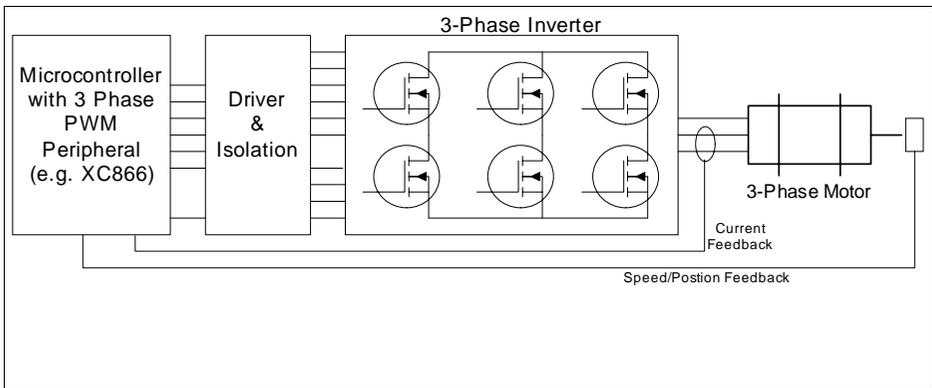


Figure 1 Typical Motor Control Application

2 Sinusoidal Voltage Generation & Capture/Compare Units

The capture/compare units of Infineon 8, 16 & 32-bit microcontrollers (CAPCOM6) are designed to control many types of motors. For controlling 3-phase motors, the capture/compare unit can be used to generate the 6 PWM signals needed to drive a 3-phase inverter, including the necessary dead-time needed to eliminate shoot-through current on each phase.

PWM can be used to create a sinusoidal voltage by creating a fixed frequency signal and adjusting the duty cycle. If the duty cycle varies sinusoidally, so will the output voltage. It is always assumed that the inductance of the motor will filter the PWM into a smooth signal as shown in Figure 2.

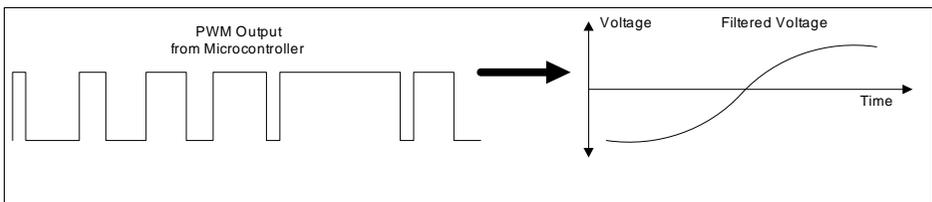


Figure 2 Using PWM to Create Sinusoidal Voltages

Capture/Compare units are designed to create variable duty cycle PWM signals. Actually it is only the “compare” feature of a Capture/Compare unit that is used for PWM generation. The Capture/Compare unit contains a timer and several compare registers. When the timer value is the same as the compare register value, an output pin is either pulled high or low. So the duty cycle of the output signal follows the compare value linearly. The CAPCOM6 unit has 3 compare registers and a timer that can count up from 0 to any specified 16-bit “period” value. When the timer reaches the period value, it reverses direction and counts down to 0. This is useful for generating center aligned PWM as shown in Figure 3.

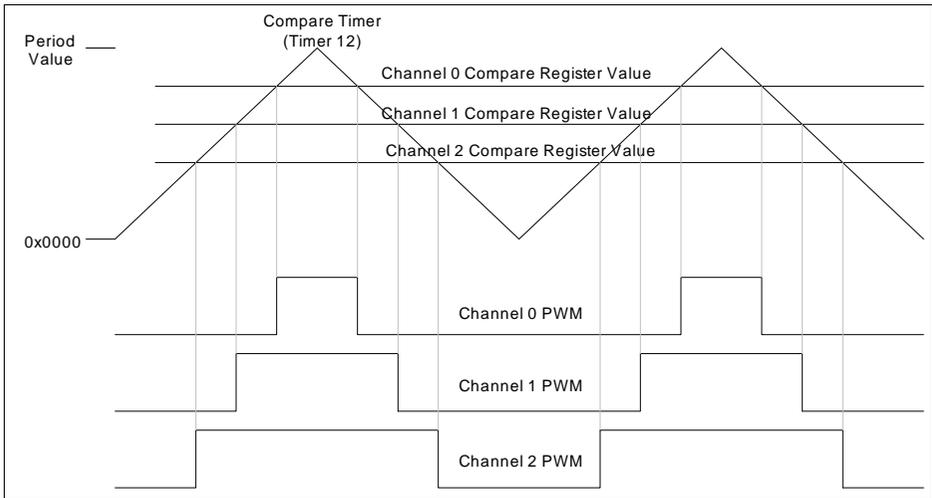


Figure 3 Center Aligned PWM Produced the CAPCOM6 Unit

To aid in 3-phase inverter control, the CAPCOM6 modules are capable of producing 6 compare outputs. For each of the 3 Compare Channels there are 2 output pins. The pins are often labeled CCx and COUTx (where x = 0, 1, 2). The polarity of each of the six pins is individually programmable. In addition to this, a programmable amount dead-time can be automatically inserted to delay the passive to active transition of both pins. This prevents shoot-through current which can destroy the inverter. Figure 4 shows how a single CCx and a COUTx pin can be used to control one phase of an inverter.

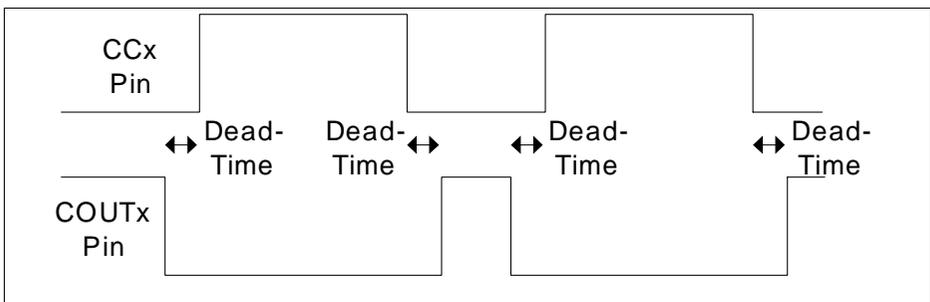


Figure 4 Dead-Time Generation (CCx and COUTx with opposite polarity)

3 Methods for Producing Sinusoidal Voltages

The following sections describe different methods of generating three phase sinusoidal voltages. Section 3.1 briefly describes a simple method for generating sinusoidal voltages using sinusoidal duty cycles. This method has been around for quite some time and has been the subject of other application notes. The biggest disadvantage to this method of voltage generation is that the maximum amplitude of the fundamental frequency of the generated line-to-line voltage is only about 86% of the inverter DC rail voltage.

Section 3.2 describes the theory behind SVM. SVM is a method of sinusoidal voltage generation which generates voltages whose amplitude of the fundamental frequency of the line-to-line voltage is equal to the full DC rail voltage. The total harmonic distortion of SVM is also less.

Section 3.3 describes over-modulation. Over-modulation is a way of increasing the amplitude of the fundamental frequency even higher (to about 1.12 times the rail voltage). Unfortunately over-modulation introduces more low order harmonics and increases the total harmonic distortion.

3.1 Sinusoidally Weighted PWM (SWPWM)

One simple way to create three phase sinusoidal voltages is to create a signal which has a very high constant frequency (compared to the frequency of the desired sinusoid) and a sinusoidally weighted duty cycle. This method of sinusoidal PWM will be referred to as SWPWM. SWPWM can be implemented very simply by placing sinusoidally weighted values into the three compare registers of the CAPCOM6 module. The CAPCOM6 module can then be used to control the 6 transistors that make up the inverter.

SWPWM has the advantage of requiring very little calculation (assuming the appropriate look-up tables are used). Each of the three phases can be made to generate a sinusoid which is 120° out of phase. The sinusoidal phase voltages generate sinusoidal line-to-line voltages and sinusoidal line-to-neutral voltages when connected to a balanced star connected load as shown in Figure 5. Scaling the voltages can be done easily with a multiply, or through some trigonometric tricks.

It should be noted that phase voltage is the voltage at one motor terminal measured with respect to the inverter negative rail voltage. Line-to-line voltage is the voltage at one motor terminal measured with respect to another terminal. Line-to-neutral voltage is the voltage at one motor terminal measured with respect to the neutral (center of the star connected load).

Methods for Producing Sinusoidal Voltages

The major disadvantage to this method of sinusoid generation is that the magnitude of the fundamental frequency of the line-to-line voltage is only ~86.6% of the inverter rail voltage.

Figure 6 shows a frequency spectrum plot of the generated line-to-line voltages when creating this type of sinusoid. Notice that in addition to the fundamental frequency, the switching frequency (~20 kHz) harmonics also have a significant magnitude.

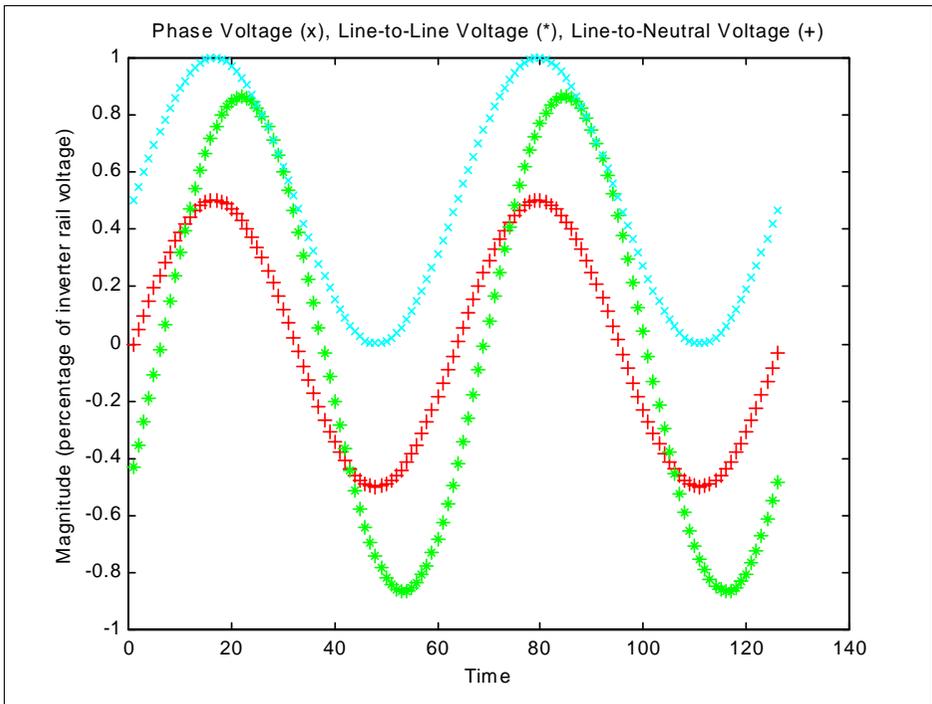


Figure 5 Sinusoidal PWM values produce sinusoidal

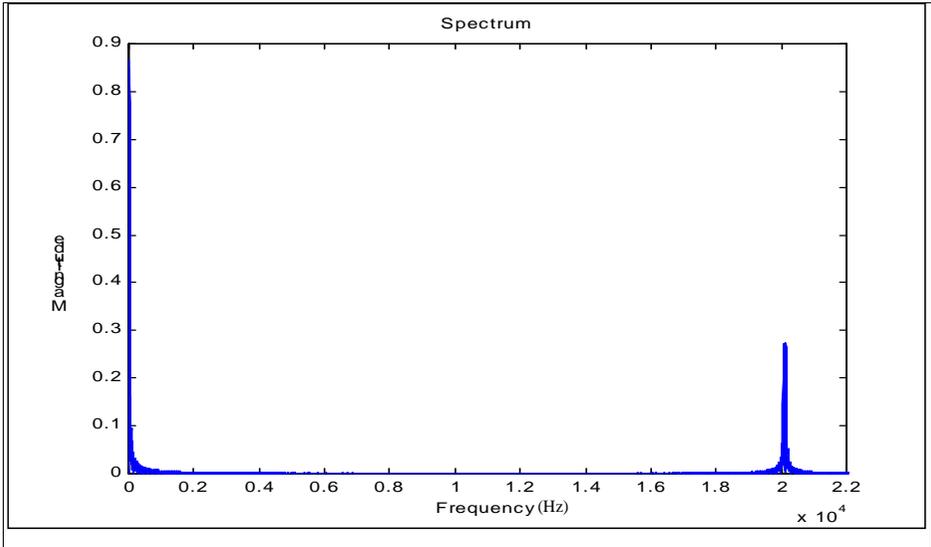


Figure 6 **Frequency Spectrum of SWPWM**

3.2 **Space Vector Modulation (SVM)**

SVM is a more sophisticated PWM method which provides a higher voltage to the motor (with lower total harmonic distortion). Consider the three phase inverter of Figure 7. Note that whenever transistor A+ is on, transistor A- must be off, and visa versa, to prevent damaging shoot-through current. This makes it easy to adopt a simple notation for describing the state of the inverter. For example, the state when transistors A+, B-, and C- are “on” (and of course A-, B+, and C+ are “off”) can be represented with the notation (+, -, -). The state where transistors A-, B+, and C- are on is denoted by (-, +, -).

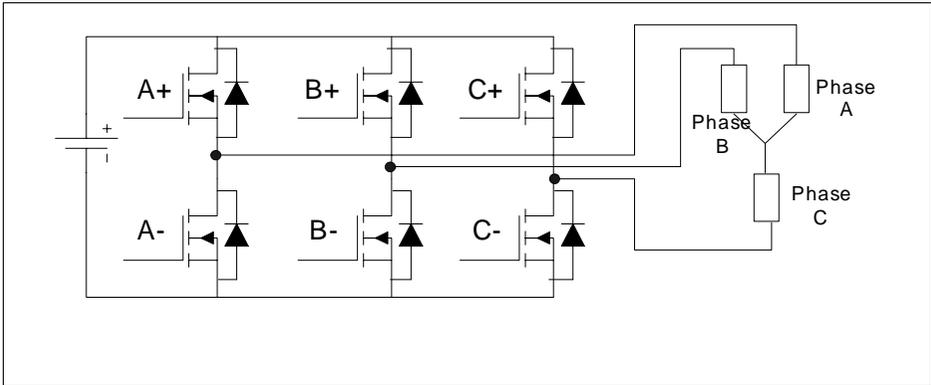


Figure 7 3 Phase Inverter with Balanced Star Connected Load

Using this notation, consider the following sequence of states:

(+, -, -), (+, +, -), (-, +, -), (-, +, +), (-, -, +), (+, -, +)

Running the inverter through this switching sequence will produce the line-to-neutral voltages shown in Figure 8. This mode of operation is called “six-step mode”. Operating in six-step mode allows you to use the full capabilities of the inverter. If you were to perform an FFT on the line-to-line voltages produced in six-step mode, you would find that the amplitude of the fundamental frequency is actually greater than the inverter rail voltage. Unfortunately six-step mode also creates high magnitude low order harmonics which cannot be filtered by the motor’s inductance.

Space vector modulation is based on six-step mode, but smoothes out the steps through some sophisticated averaging techniques. For example, if a voltage is required that is between two step voltages, the corresponding inverter states can be activated in such a way that the average of the step voltages produces the desired output. To develop the equations needed to generate this averaging effect, the problem is transformed into an equivalent geometrical problem. The first step in this re-definition is to transform the inverter voltages of six-step mode into space vectors.

Space vectors are similar to phasors in that they are denoted by a magnitude and an angle. It is important to note that space vectors are not phasors. A Phasor is used to represent something that varies sinusoidally in time. A space vector is used to represent something that varies sinusoidally in space with respect to an angle. For this reason space vectors are sometimes referred to as space phasors.

Methods for Producing Sinusoidal Voltages

In general, any three time varying quantities, which always sum to zero and are spatially separated by 120° can be expressed as a space vector.

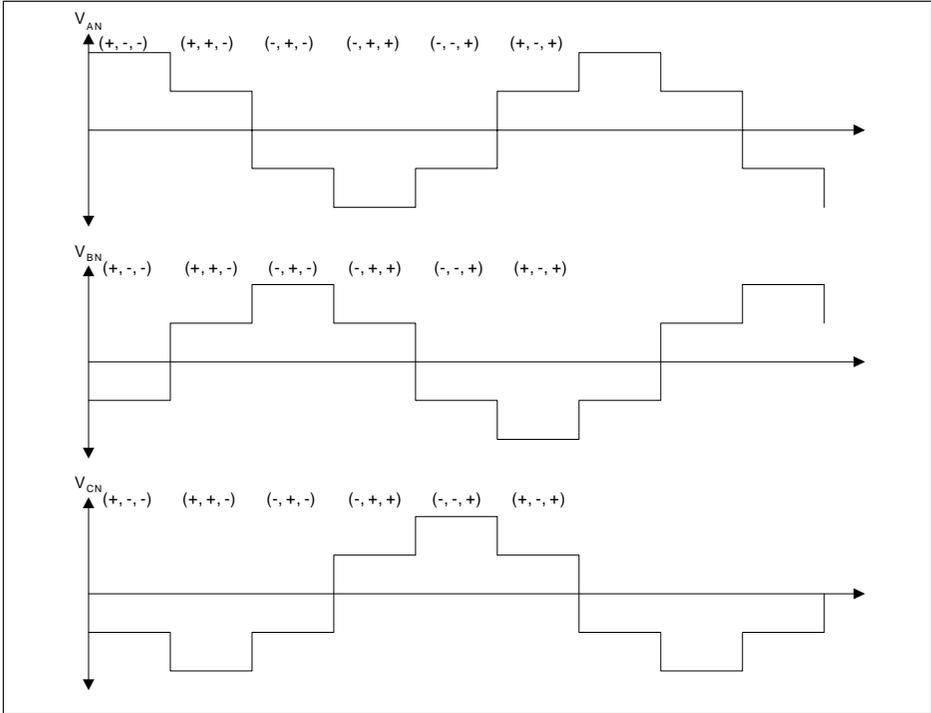


Figure 8 Line-to-Neutral Voltages in Six-Step Mode

Since the three line-to-neutral voltages sum to zero, they can easily be converted into a space vector (\underline{u}_s) using the following transformation:

$$\underline{u}_s = V_{an}(t) e^{j0} + V_{bn}(t) e^{j2\pi/3} + V_{cn}(t) e^{-j2\pi/3}$$

Since the components of space vectors are projected along constant angles (0, $2\pi/3$, and $-2\pi/3$), it is easy to graphically represent a space vector as shown in Figure 9.

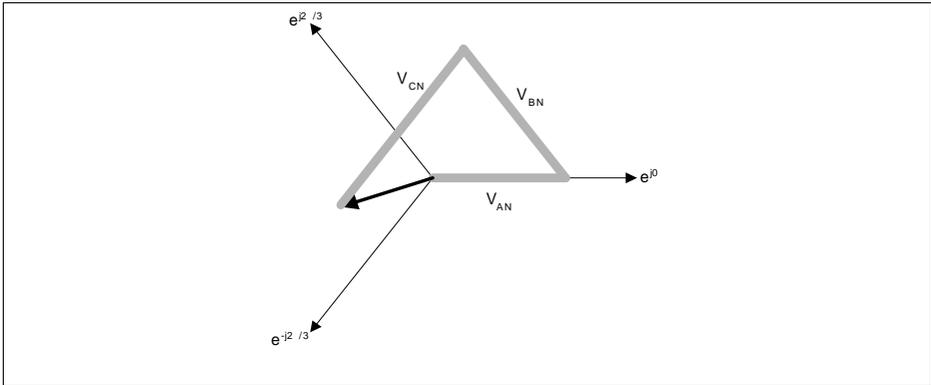


Figure 9 Transforming 3 quantities into a Space Vector

Usually, when creating space vectors, the three time-varying quantities are sinusoids of the same amplitude and frequency that have 120° phase shifts. When this is the case, the space vector at any given time maintains its magnitude. As time increases, the angle of the space vector increases, causing the vector to rotate with frequency equal to the frequency of the sinusoids.

If the voltages of Figure 8 are converted into a space vector and plotted on the complex plane, it can be seen that the space vector takes on one of 6 distinct angles as time increases (instead of rotating smoothly as it would if the voltages were pure sinusoids). Figure 10 shows the values that the space vector assumes as time increase.

The goal of space vector modulation is to generate the appropriate PWM signals so that any vector (\underline{u}_s) can be produced. Consider a space vector voltage \underline{u}_s located in the sector defined by \underline{u}_1 and \underline{u}_2 . We can approximate \underline{u}_s by applying \underline{u}_1 for a percentage of time (t_a) and \underline{u}_2 for a percentage of time (t_b) such that:

$$t_a \cdot \underline{u}_1 + t_b \cdot \underline{u}_2 = \underline{u}_s$$

This leads to the following formulas for t_a and t_b :

$$\begin{aligned}
 t_b &= 2U(3^{-1/2})\sin(\alpha) & \text{where } U &= |\underline{u}_s| \text{ (Modulation Index)} \\
 t_a &= U[\cos(\alpha) - (3^{-1/2})\sin(\alpha)] & \alpha &= \angle \underline{u}_s
 \end{aligned}$$

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So given a space vector of angle α (in sector 0) and modulation index U , the approximation can be constructed by applying vectors \underline{u}_1 and \underline{u}_2 for percentage of times t_a and t_b , respectively. Graphically this is represented in Figure 11. If the vector is in another sector, it can be rotated by a multiple of $\pi/3$ radians until it is in sector 0. The times can be calculated and then applied to the appropriate inverter states.

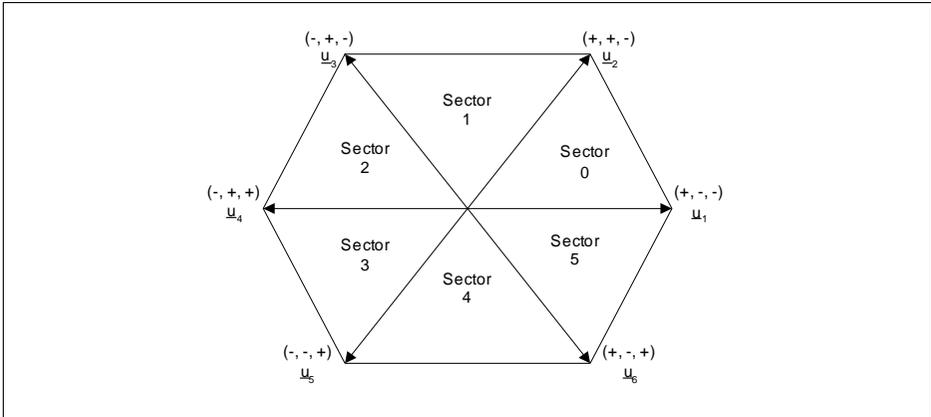


Figure 10 Space Vectors of Line-to-Neutral Voltages in Six-Step Mode

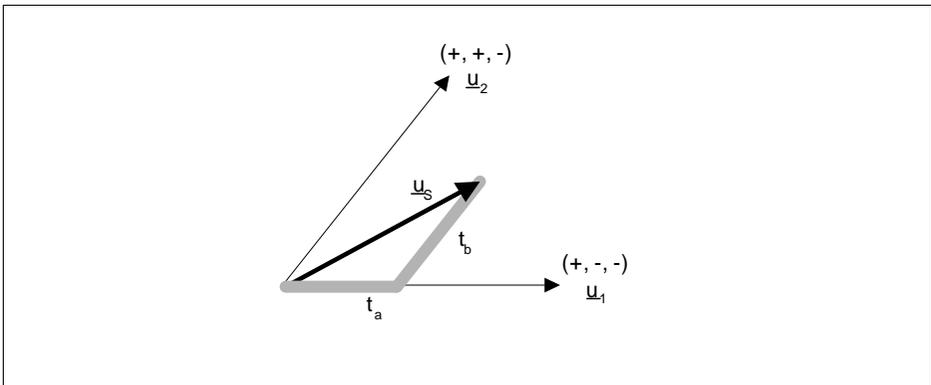


Figure 11 Approximation of the Space Vector \underline{u}_s by t_a and t_b

Like many other types of PWM, space vector modulation uses pulses of constant frequency (carrier frequency) with variable duty cycle. The carrier frequency is often chosen so that it is high enough to be out of the audible range and produces little

Methods for Producing Sinusoidal Voltages

current ripple, but not so high as to create excessive switching losses. The period of the carrier will be called T_0 .

To approximate the \underline{u}_s in Figure 11, the inverter state that corresponds to \underline{u}_1 should be active for $t_a \cdot T_0$ seconds, and the inverter state that corresponds to \underline{u}_2 should be active for $t_b \cdot T_0$ seconds. When the modulation index is sufficiently small (less than $\frac{1}{2}(3^{1/2})$), the sum of t_a and t_b will be less than one. This means that $t_a \cdot T_0 + t_b \cdot T_0$ is less than T_0 . So for the left over time no voltage should be applied to the motor. The "left over" time will be referred to as t_0 . To be more formal:

$$t_0 = T_0 (1 - t_a - t_b)$$

There are two ways to apply no voltage to the motor. The first way is to simply connect all three phases to the negative rail of the inverter. This will be called inverter state 0 and the corresponding switching pattern is (-, -, -). The second way to apply no voltage to the motor is to connect all three phases to the positive rail of the inverter. This will be called inverter state 7 and the corresponding switching pattern is (+, +, +).

So, to approximate the voltage \underline{u}_s during the PWM carrier period, the pulses and timing shown in Figure 12 could be used. To obtain a better total harmonic distortion, a slightly different method of applying the switching states can be used. If the t_0 time is split in half and applied at the beginning and the end of T_0 , then a more symmetric distribution of pulses can be generated. This method is known as symmetric or center-aligned space vector modulation. Figure 13 shows how symmetric space vector modulation is implemented over two consecutive carrier periods.

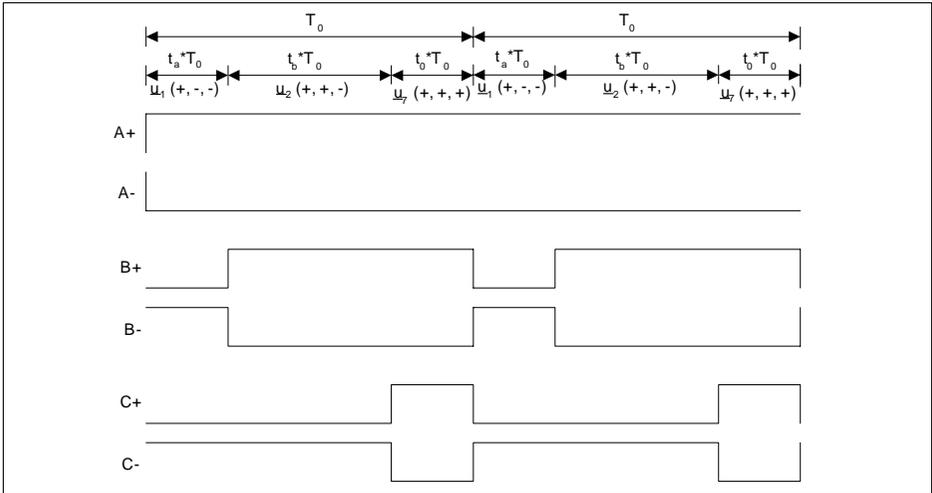


Figure 12 Asymmetric PWM for SVM

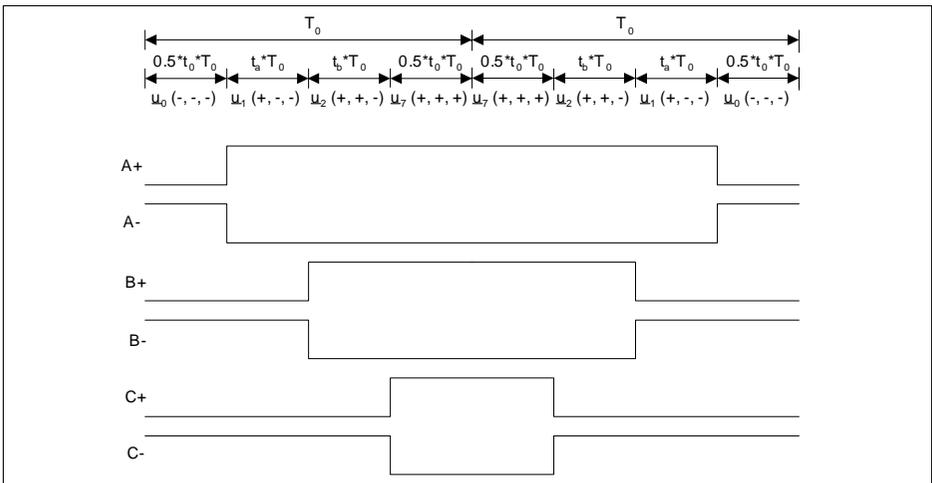


Figure 13 SVM using Symmetric PWM

Methods for Producing Sinusoidal Voltages

The pulses shown in Figure 13 are very similar to those shown in Figure 3, and can be easily generated using the CAPCOM6 module. As shown in Figure 13, the switching frequency is $1/(2 \cdot T_0)$.

When the modulation index exceeds $\frac{1}{2}(3^{1/2})$, the value of t_0 can become negative (depending on the angle). Since it is not physically possible to apply one of the zero vectors for negative time, the maximum modulation index for space vector modulation is approximately 0.866. Graphically, this means that for space vector modulation to work properly, the magnitude of the reference space vector, \underline{u}_s , must be small enough to ensure that the vector is totally contained inside the hexagon shown in Figure 10.

When symmetric space vector modulation is implemented with a modulation index of 0.866, the ideal phase voltage (after filtering by the motor) as shown in Figure 14 is generated. The phase voltage of Figure 14 has the same shape as the compare values that should be used. These unusual voltages create sinusoidal line-to-neutral voltages (as expected) and sinusoidal line-to-line voltages are also generated.

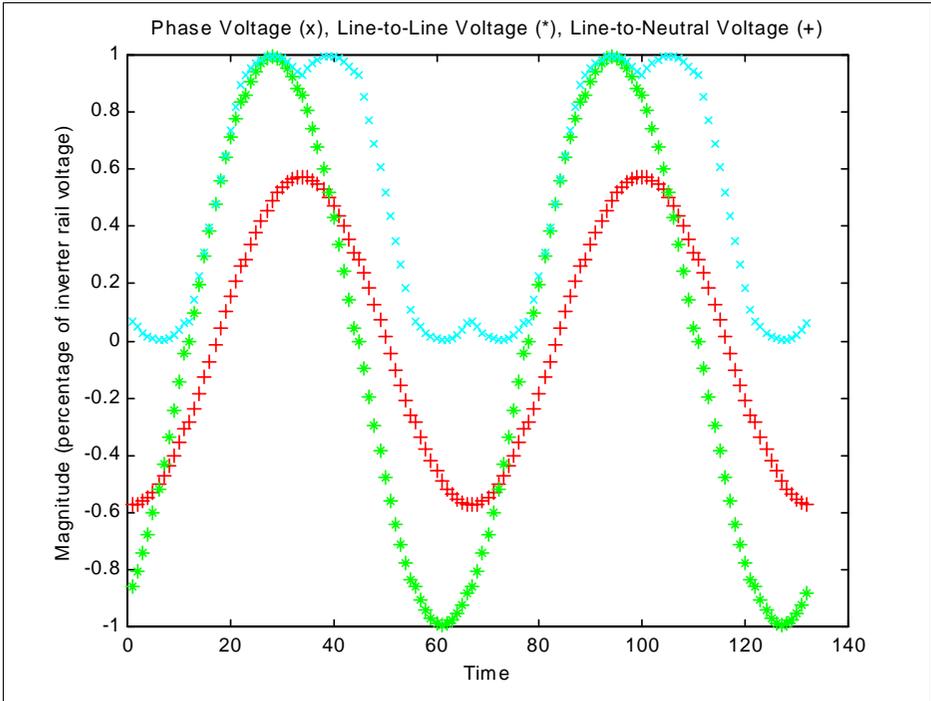


Figure 14 Voltages Generated by SVM

As shown in Figure 14, SVM can create sinusoidal line-to-line voltages which have amplitudes equal to the inverter rail voltage, even though the modulation index is only 0.866. SVM has also been proven to produce lower current harmonics and torque ripple than SWPWM. Figure 15 shows the frequency spectrum of the line-to-line voltage of a SVM simulation with modulation index of approximately 0.866. As Figure 15 shows, the magnitude of the fundamental frequency is higher and the magnitude of the switching frequency is lower than Figure 6.

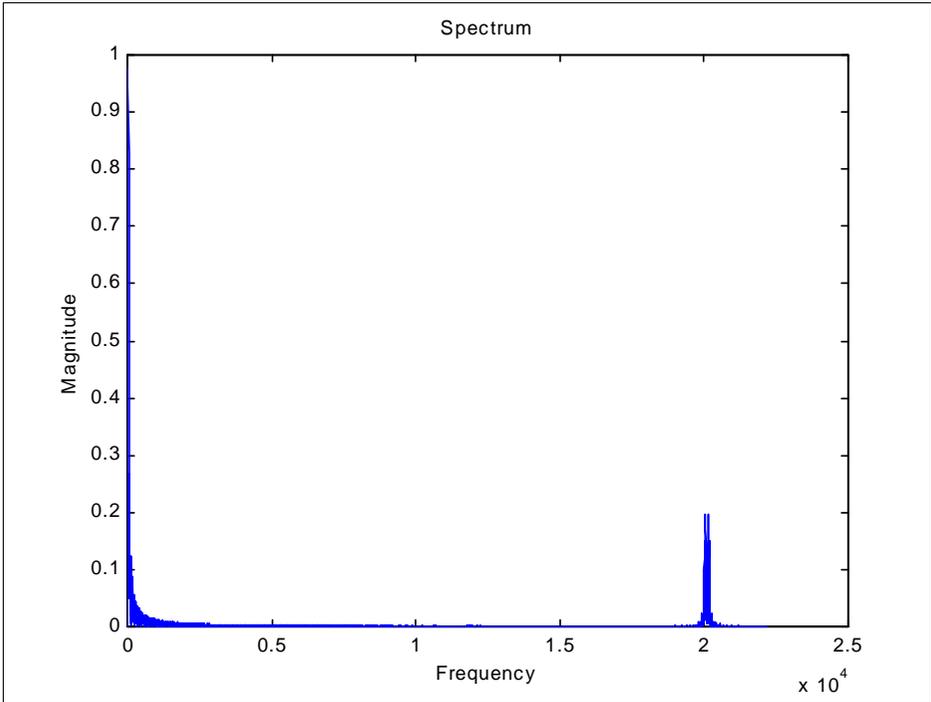


Figure 15 Frequency Spectrum of SVM Line-to-Line Voltage with $U=0.866$

3.3 Over-modulation

It has been proven that SVM can produce higher amplitude voltages than SWPWM, even if the modulation index is limited to 0.866. There are several techniques that can be used to extend this modulation index range. These techniques are referred to as over-modulation.

Figure 16 shows a graphical representation of the problem. In Figure 16, sector 0 from the hexagon of Figure 10 is shown. Over-modulation is needed when the modulation index (the length of the reference space vector, \underline{u}_s) causes the head of the vector to be located outside of the hexagon.

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In Figure 16, t_0 will only become negative if $\alpha_1 < \alpha < \alpha_2$. A simple method of overmodulation is based on the angle, α , of the reference vector \underline{u}_s , as shown in Table 1.

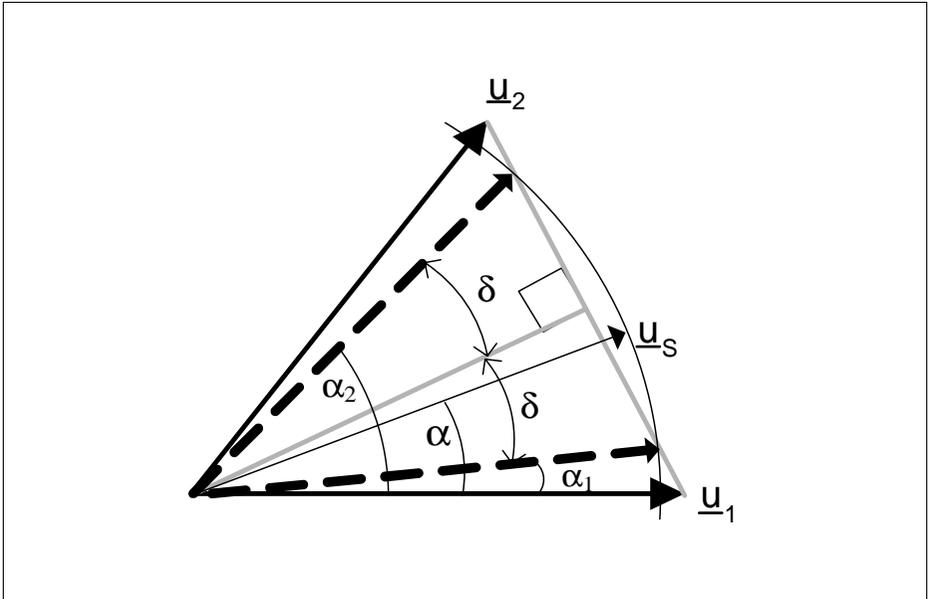


Figure 16 Graphic Depiction of a Space Vector with $U > 0.866$

Table 1 Angle and Magnitude to use for Over-modulation

Angle of \underline{u}_s α	Length of \underline{u}_s Modulation Index	Angle to use for SVM
$\alpha_2 < \alpha < \alpha_1$	U	α
$\alpha_1 < \alpha < \pi/6$	U	α_1
$\pi/6 < \alpha < \alpha_2$	U	α_2

Methods for Producing Sinusoidal Voltages

When α is less than α_1 , space vector modulation can be performed as usual using U and α . Since the head of \underline{u}_s is inside the hexagon, t_0 will be greater than zero and everything will work properly. When α is between α_1 and $\pi/6$, t_0 will be less than zero. To avoid this, SVM can be performed using α_1 and U . This will yield a t_0 of zero. When α is between $\pi/6$ and α_2 , again, t_0 will be less than zero. To avoid this, SVM can be performed with U and α_2 . Once α is greater than α_2 , SVM can be performed normally again with α and U .

This method of over-modulation will obviously not produce line-to-line and line-to-neutral voltages which are as 'clean' as normal space vector modulation, but it will allow the modulation index to exceed 0.866. If the frequency spectrum of the PWM is analyzed then it can be seen that the fundamental frequency does increase beyond what is capable using just SVM. Of course, the total harmonic distortion will increase.

When the modulation index reaches 1.000, over-modulation will produce signals equivalent to six-step mode. In six-step mode the magnitude of the fundamental frequency of the line-to-line voltage is ~112% of the inverter rail voltage.

The values of α_1 and α_2 can be determined by examining Figure 16:

$$\alpha_1 = \pi/6 - \delta \qquad \text{where} \quad \delta = \arccos(1/2(3^{1/2})/U)$$

$$\alpha_2 = \pi/6 + \delta$$

Figure 17 shows the magnitude of the fundamental frequencies produced using SVM, over-modulation and SWPWM.

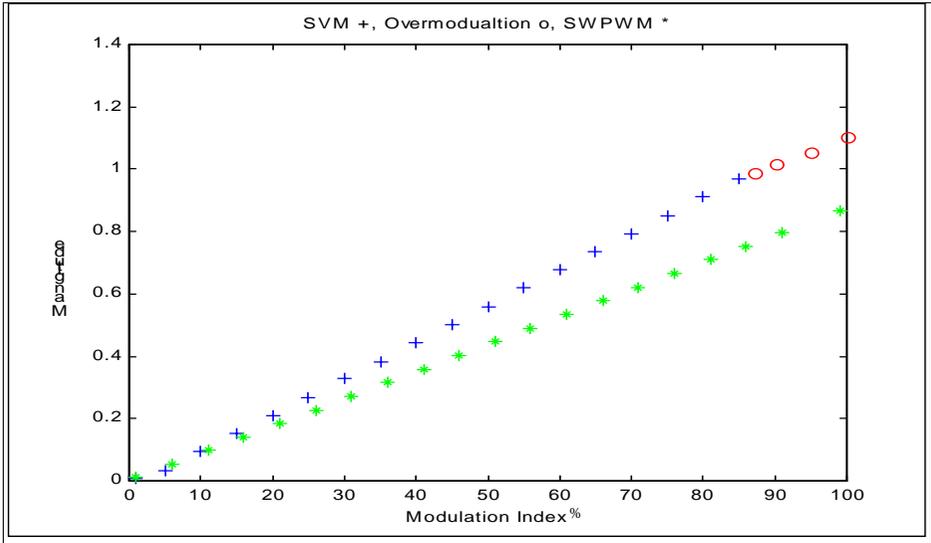


Figure 17 Fundamental Frequency of Line-to-Line Voltages

4 Microcontroller Implementation of SVM

Microcontroller implementation of SVM and over-modulation can be very difficult. The SVM equations can be complicated, and over-modulation adds to the complexity. Proper scaling variables can make the computations much easier. Section 4.1 describes the variable scaling and resolution used for a SVM and over-modulation implementation using the Infineon XC866 8051 based 8-bit microcontroller. An optimized flow chart for SVM and over-modulation is also given.

There are several implementation options which effect SVM performance and CPU load. Section 4.2 also discusses these options and possible trade-offs a designer should consider.

Section 4.3 shows the results of the SVM and over-modulation implementation with the XC866. Conclusions are also given.

4.1 Variable Scaling and Resolution and Software Optimization

To implement SVM, the microcontroller must receive (or perhaps even generate) a reference space vector. It is usually convenient if the space vector is given in terms of a magnitude (U) and an angle (α). Given U and α the switching times can be calculated by the formulas:

$$\begin{aligned}t_b &= 2U(3^{-1/2})\sin(\alpha) \\t_a &= U[\cos(\alpha) - (3^{-1/2})\sin(\alpha)] \\t_0 &= T_0 - t_a - t_b\end{aligned}$$

The first step should be to decide on a switching frequency. In many cases, PWM frequencies above 20 kHz are considered to be ideal. Since the CAPCOM6 unit will operate as an up/down counter, this means that the timer period value should be above 40 kHz.

To keep the calculations simple for an 8-bit microcontroller, T_0 should be represented as an 8-bit value. This means that the period value for the CAPCOM6 Timer (Timer 12) should be set to 0x00FF. The XC866 operating from the internal oscillator and at the maximum PLL factor runs at 26.67MHz. So setting up the CAPCOM6 Timer 12 in symmetric PWM mode with a period value of 0x00FF and a divide by 2 pre-scaler will enable 26 kHz PWM.

It is also convenient if U is scaled to be an 8-bit value. U is a "per unit" value which means that it is always between zero and one, so the resolution of U will be 1/255 or 0.00392.

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Since the equations for t_a , t_b , and t_0 are only valid for α between 0 and $\pi/3$, it would be easier if α is represented by an 11-bit value. If the most significant 3 bits can be used to indicate the sector, the least significant 8-bits can contain the angle within the sector with a resolution of $\pi/765$ radians or 0.235 degrees. This allows the formulas for t_a , t_b , and t_0 to be valid for any α as long as only the low byte is used.

A look-up table can be used for sine and cosine so that t_a and t_b can be calculated, but it would require less computation if the values of t_a and t_b for $U = 1.0$ (0xFF in fixed point) are stored in look-up tables. The values can then be looked-up and scaled for the appropriate value of U . If one creates a table of t_a and t_b for the 255 different values of α for the case when $U = 1$, it can be easily seen that the table for t_a is exactly the same as the table for t_b except in reverse. This means that only one table is needed. Table 2 shows the digital representation of the variables needed for SVM and over-modulation.

Table 2 Representation of Variables needed for SVM and Over-modulation

Variable	Digital Representation	Engineering Unit Resolution	Comments
U ($ \underline{u}_s $)	8-bit value (0x00 – 0xFF)	1/255 (~0.00392)	Input Variable
α ($\angle \underline{u}_s$)	11-bit value (0x0000 – 0x05FF)	$\pi/765$ radians (~0.235 degrees)	Bits 0-7 contain α , Bits 8 – 10 contain sector (input variable)
T_0	8-bit value (0x00 – 0xFF)	CCU timer resolution (100 ns)	~19.6 kHz Carrier Frequency (fixed)
t_b	8-bit value (0x00 – 0xFF)	CCU timer resolution (100 ns)	Stored in a table Table contains t_b for $U = 1.0$ (0xFF)
t_a	8-bit value (0x00 – 0xFF)	CCU timer resolution (100 ns)	Stored in a table t_b table is used in reverse
t_0	8-bit value (0x00 – 0xFF)	CCU timer resolution (100 ns)	Calculated $t_0 = \sim(U*t_a + U*t_b)/256$
α_1 and α_2	8-bit values (0x00 – 0xFF)	$\pi/765$ radians (~0.235 degrees)	Calculated as needed from δ

The CAPCOM6 unit relieves the CPU of much of the computational work required for symmetric PWM generation. From Figure 13, the relationship between the compare values and t_a , t_b , and t_0 can be determined. Table 3 shows how the compare values

Microcontroller Implementation of SVM

for phases A, B, and C can be chosen based on the sector in which the reference vector is located.

Table 3 Compare Values for Symmetric SVM

Sector	Phase A Compare Value	Phase B Compare Value	Phase C Compare Value
0	$\frac{1}{2} t_0$	$\frac{1}{2} t_0 + t_a$	$T_0 - \frac{1}{2} t_0$
1	$\frac{1}{2} t_0 + t_b$	$\frac{1}{2} t_0$	$T_0 - \frac{1}{2} t_0$
2	$T_0 - \frac{1}{2} t_0$	$\frac{1}{2} t_0$	$\frac{1}{2} t_0 + t_a$
3	$T_0 - \frac{1}{2} t_0$	$\frac{1}{2} t_0 + t_b$	$\frac{1}{2} t_0$
4	$\frac{1}{2} t_0 + t_a$	$T_0 - \frac{1}{2} t_0$	$\frac{1}{2} t_0$
5	$\frac{1}{2} t_0$	$T_0 - \frac{1}{2} t_0$	$\frac{1}{2} t_0 + t_a$

Fortunately, T_0 is 0xFF, so $T_0 - \frac{1}{2} t_0$ is simply $\sim \frac{1}{2} t_0$, and t_0 is simply $\sim (t_a + t_b)$. Figure 18 shows the flow chart (optimized for execution time) for a microcontroller implementation of SVM and overmodulation.

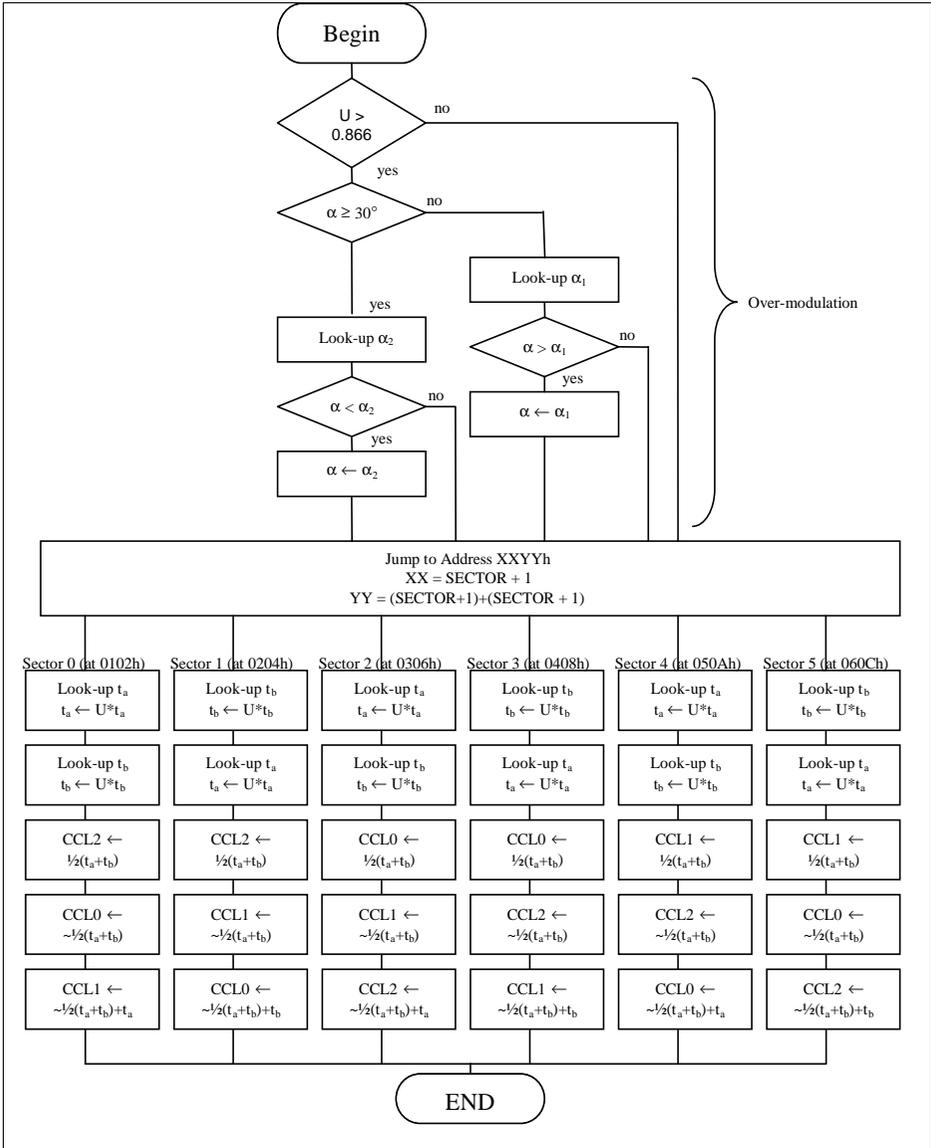


Figure 18 Microcontroller Implementation of SVM and Over-modulation

4.2 SVM Implementation Options

The compare registers of the CAPCOM6 peripheral have shadow registers that allow all of the compare values to be updated at once. When the compare registers are written to by the microcontroller, the values are actually stored in the shadow registers. If the Shadow Transfer Enable bit (STE12) is set, then the contents of the shadow registers are copied to the actual compare registers as soon as the timer (T12) reaches the period value (when counting up) or 0x0001 when counting down. This shadow latch mechanism ensures that the three compare values are updated simultaneously and it also guarantees that there are no disturbed pulses.

Generally SVM is performed twice every switching period as shown in Figure 13. To properly implement this, the shadow latch transfers must occur when the compare timer reaches 0x0001 and when the compare timer reaches its period value. However many times SVM is implemented so that the compare values are only updated when the timer is 0x0001 to reduce CPU load and to keep the PWM symmetric. The user can decide which option best suits his needs.

With most carrier based PWM methods, the microcontroller compare value calculation is synchronized with the carrier signal (the compare timer). This ensures a more consistent latency between the time that the new input values (u_s) are received until the pulses are actually present on the output pins. This synchronization is usually accomplished by performing the SVM calculations after a compare timer interrupt. The CAPCOM6 module can generate interrupts when the compare timer reaches zero and when the timer reaches its period value. This is equivalent to having an interrupt at the beginning of every T_0 . Using these interrupts to trigger the SVM calculations will ensure a more consistent input to output latency.

SVM and over-modulation have been implemented on the XC866. The actual SVM and over-modulation code was written in assembly language to optimize the execution speed. The assembly code is part of a larger project that includes C files for initialization and testing. A conditional assembly switch is also used to enable or disable over-modulation.

When implementing SVM in a motor control application, there are many factors which will influence the CPU load. Table 4 shows some of the major factors and their impact on CPU load when using the algorithms of Figure 18. It should be noted that the switching frequencies shown in Table 4 can be obtained without changing the SVM algorithm. The only modification needed is a change of the CAPCOM6 Timer 12 pre-scaler. Table 4 shows only the CPU load for the SVM algorithm (the compare timer

Microcontroller Implementation of SVM

ISR) without a control loop. It also assumes that the XC866 is operating at 26.67 MHz from internal flash with one wait-state (6.67 MIPS).

In addition to SVM and over-modulation, the demo code that accompanies this application note implements a simple control loop that allows the user to adjust the length and velocity of the input vector. Two A/D channels are used to control the amplitude and frequency of the generated voltages.

Table 4 CPU Load for SVM assuming 150 ns per Instruction Cycle

		Switching Frequency		
		6.5 kHz	13 kHz	26.0 kHz
SVM Executed Once Per Switching Period	SVM only	7.6%	15%	30%
	SVM w/Overmodulation	9.5%	19%	38%
SVM Executed Twice Per Switching Period	SVM only	15%	30%	61%
	SVM w/Overmodulation	19%	38%	76%

4.3 Results and Conclusions

The source code that accompanies this application note was executed using the XC866 microcontroller evaluation board. To view the output, either the CCx or COUTx pins of the microcontroller can be connected to an external circuit as shown in Figure 19. Capacitors are used to filter the PWM outputs so the voltages will appear smooth when viewed by an oscilloscope. The source code for this application note uses two analog inputs to control the magnitude and frequency of the generated voltage. This portion of the code will be omitted or modified in most applications.

Accompanying this application note are the source code files and an Excel spreadsheet which can be used to calculate the look-up table values if different dead-times are needed.

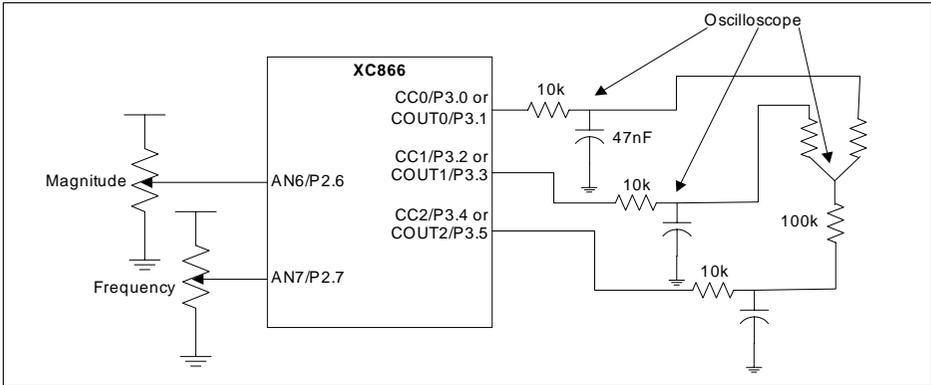


Figure 19 Circuit for Viewing SVM Output with an Oscilloscope

Figure 20 shows the phase, neutral, and line-to-neutral voltages when U is less than 0.866 (over-modulation is not active). Figure 21 shows two phase voltages and the line-to-line voltages for the same case. Figure 22 shows the phase, neutral and line-to-neutral voltages when U is greater than 0.866 and less than 1 (over-modulation is active). Figure 23 shows the phase, neutral and line-to-neutral voltages when $U = 1$ (six-step mode). As these figures show, both symmetric SVM and over-modulation with >20 kHz switching frequency are possible with Infineon microcontrollers and the CAPCOM6 unit.

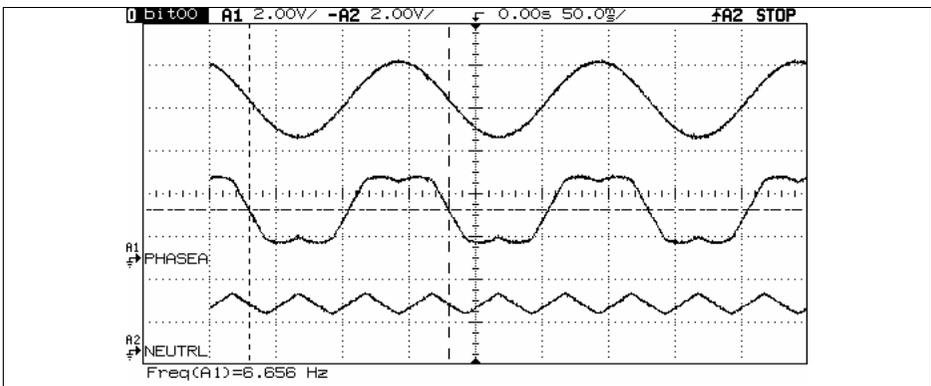


Figure 20 SVM Neutral, Phase and Line-to-Neutral Voltages for $U < 0.866$

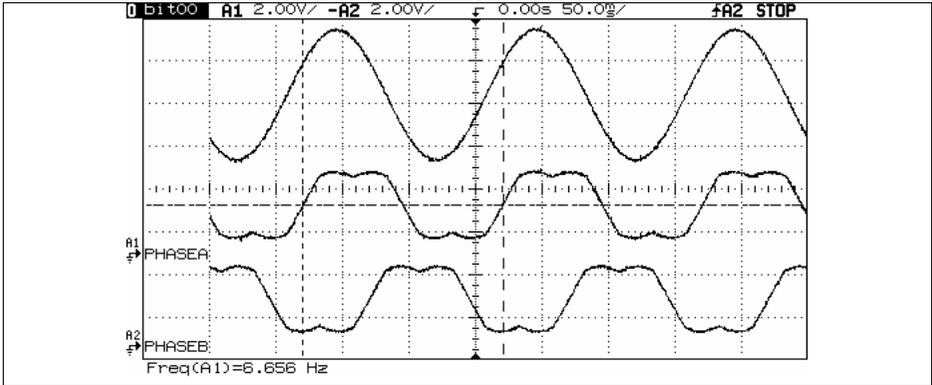


Figure 21 SVM Phase and Line-to-Line Voltages for $U < 0.866$

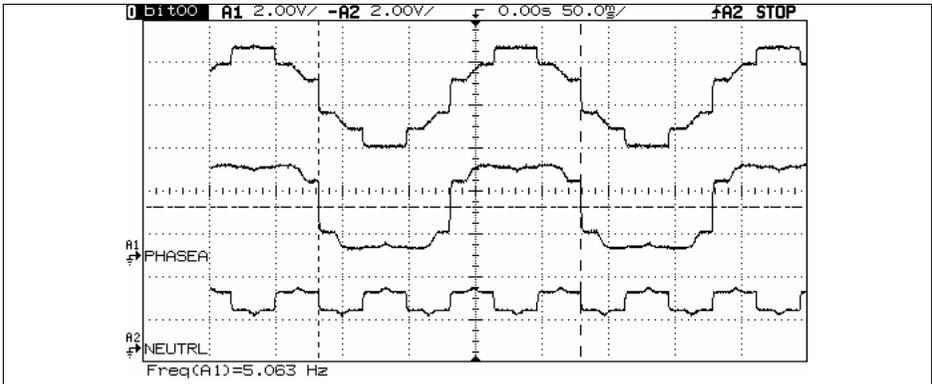


Figure 22 Over-mod Phase, Neutral and Line-to-Neutral Volts for $U > 0.866$

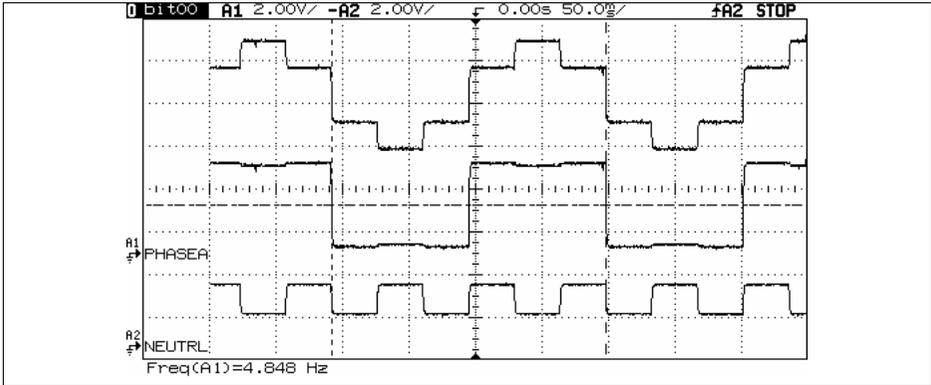


Figure 23 Over-mod Phase, Neutral and Line-to-Neutral Volts for $U=1$

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