IR1161 µSmartRectifier™ Control IC Design Notes

Authors: Helen Ding
Peter Green

Application Note

About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to using the IR1161 single channel synchronous rectification control IC in the output of a switch mode power supply (SMPS). The scope applies to all technical aspects that should be considered in the design process, including calculation of external component values, MOSFET selection, PCB layout optimization as well as additional circuitry that may be added if needed in certain cases.

Intended audience

Power supply design engineers, applications engineers, students.

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1 Introduction and Device Overview

The IR1161 smart secondary side controller drives an N-Channel power MOSFET used as a synchronous rectifier in isolated Flyback converters operating in discontinuous (DCM) or quasi resonant (QR) mode, also known as critical (CrCM) conduction, transition or boundary-mode. A pair of IR1161s and MOSFETs may be also be used as a dual synchronous rectifier in resonant half-bridge converters.

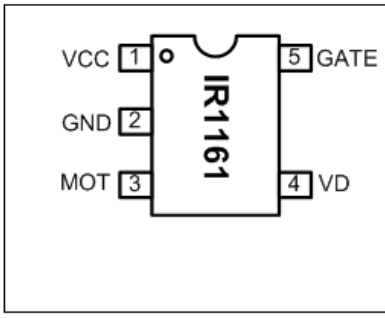
The IR1161 precisely controls switching on and off of the synchronous MOSFET thereby bypassing its body diode during the secondary conduction phase and emulating the rectifying action of a diode rectifier while eliminating the majority of conduction losses. The MOSFET drain to source voltage is sensed at millivolt levels to determine the polarity of the drain current switching the gate on and off gate in close proximity to the zero current transition. The high voltage input structure allows the IR1161 to withstand up to 200 V from direct connection to the drain.

Internal blanking, reverse current protection circuit and double-pulse suppression provide safe and reliable operation. The IR1161 based smart synchronous rectifier (SR) offers significant efficiency improvement in DCM Flyback converters over the full load range so that replacing a Schottky diode output rectifier with the IR1161 and a correctly selected high performance MOSFET provides significantly lower power dissipation. PCB space savings due to the IR1161's small SOT23-5 package are further aided by reduced MOSFET heat dissipation.

The IR1161 is able to operate from a wide V_{CC} supply voltage ranging from 4.75 V to 20 V making it possible to supply it from the output in a 5V system and eliminating the need for an auxiliary winding. A logic level MOSFET is required for low output voltage applications.

A built-in arming and triggering mechanism is included to allow correct switching on and off of the SR MOSFET under all system conditions, making it superior to a basic self-driven SR scheme or earlier generations of SR controller.

IR1161 is available in a 5-pin SOT-23 package. The pin out is shown below:



PIN#	Symbol	Description
1	VCC	Supply Voltage
2	GND	Ground
3	MOT	Minimum On Time Program Input
4	VD	FET Drain Sensing
5	GATE	Gate Drive Output

Figure 1 IR1161 pin assignment

2 SmartRectifier™ Concept

The SmartRectifier™ control technique is based on sensing the voltage across the MOSFET drain to source and comparing it with two internal negative thresholds determine the correct points of gate turn on and off. The first negative threshold V_{TH2} detects current through the body diode determining when to turn on. A second negative threshold V_{TH1}, which is in the range of milli-Volts, determines the level at which the gate is turned off.

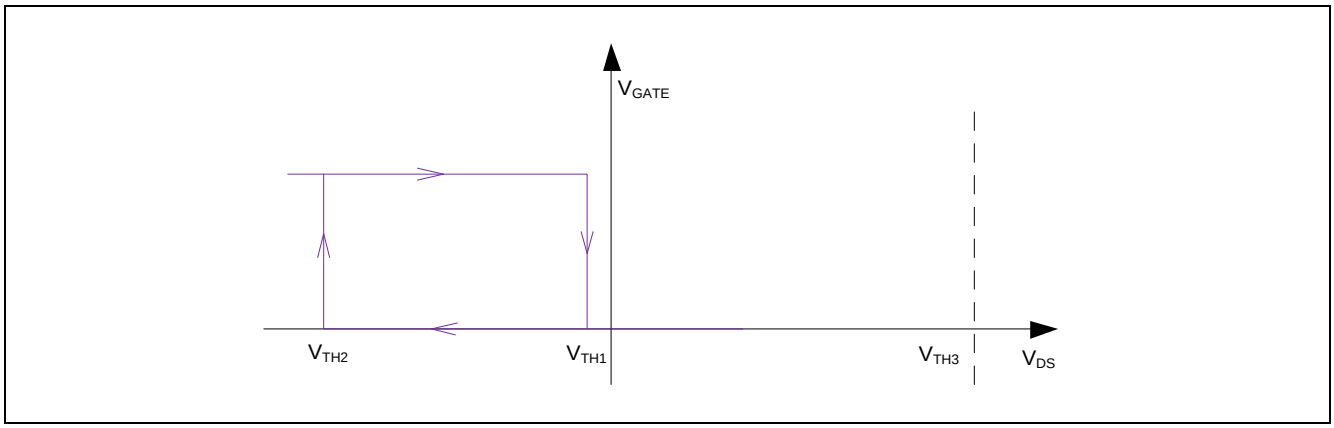


Figure 2 IR1161 SmartRectifier™ control IC voltage sensing thresholds

The secondary side of a Flyback converter is shown in Figure 3 with the IR1161 driving the SR MOSFET connected at the low-side return. The operating waveforms of the IR1161 in this application are shown in Figure 4.

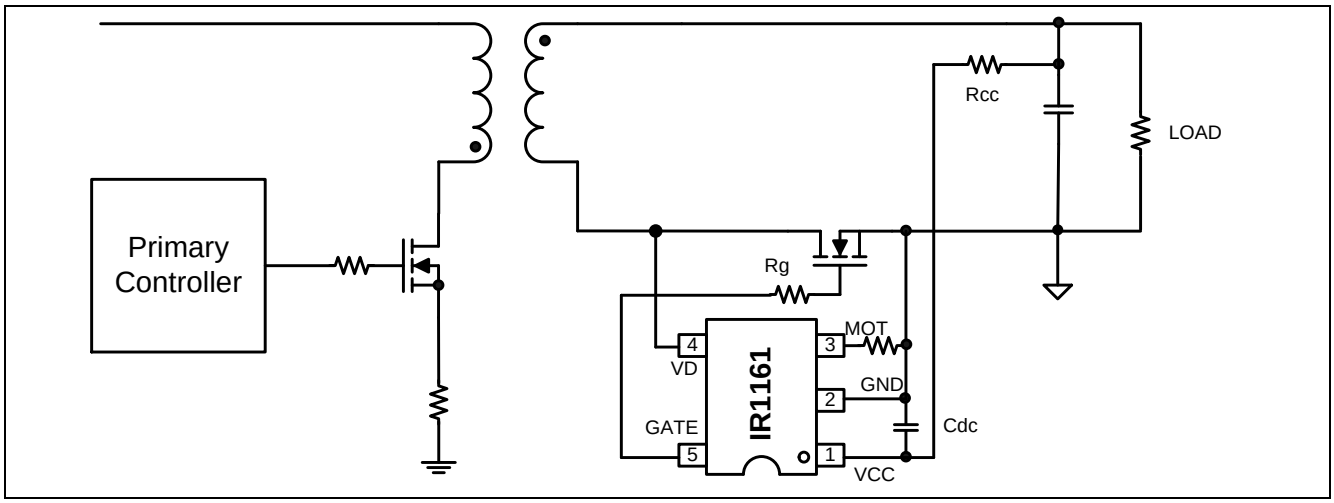


Figure 3 Flyback converter with synchronous output rectification

T1 is the conduction phase of the primary switch during which energy is being stored in the Flyback transformer. The T2 phase begins when the primary switch is turned off and the energy stored in the magnetic field starts to be delivered to load through the output rectifier circuit. At this point the conduction phase of the SR MOSFET is initiated and current starts flowing through the body diode, generating a negative V_{DS} voltage. The body diode has a much higher voltage drop than the turn-on threshold V_{TH2} causing the IR1161 to drive the gate of the SR MOSFET on to bypass it.

When the MOSFET is turned on the instantaneous sensed voltage reduces to $R_{DSon} \cdot I_D$. This voltage level being much lower than body diode forward voltage drop is sensitive to parasitic ringing generated by the transformer leakage inductance and MOSFET output capacitance. To avoid mis-triggering and resulting

premature gate turn-off, a blanking period (MOT) is used that disables V_{TH1} triggering for a minimum period of time set by an external resistor.

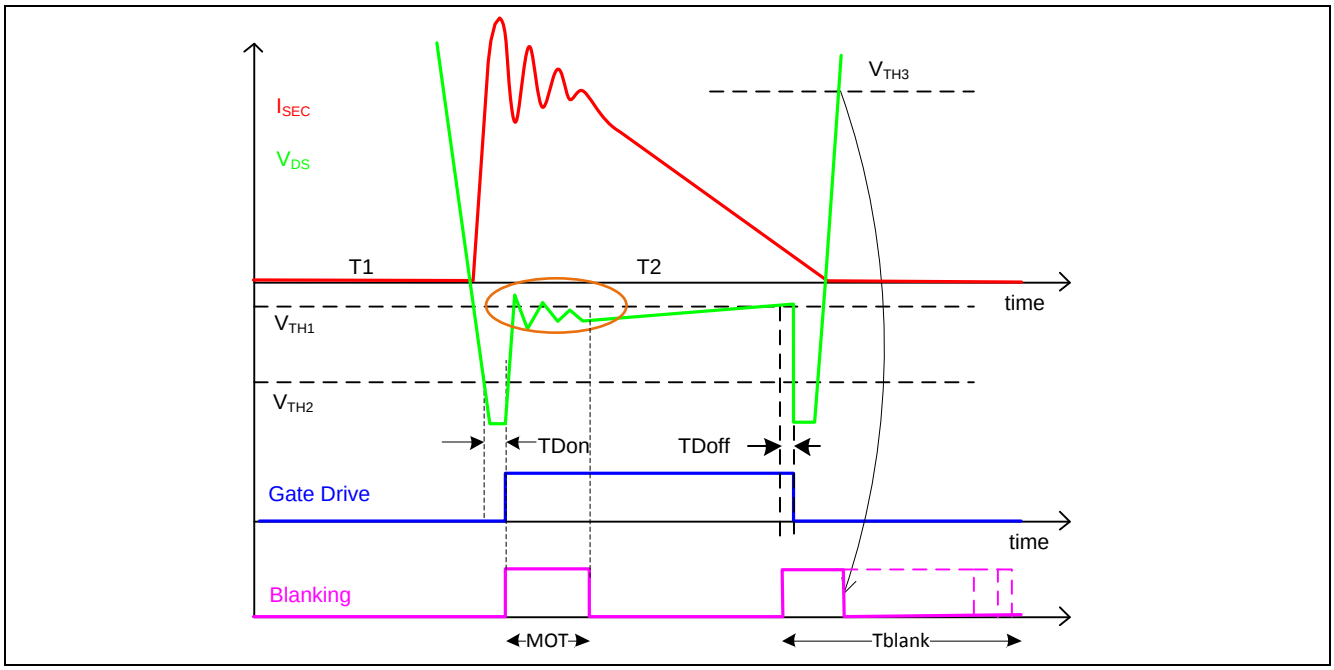


Figure 4 Secondary synchronous rectification waveforms of DCM/CrCM Flyback

At the end of each switching cycle the secondary current reduces to zero and the V_{DS} voltage crosses the turn-off threshold V_{TH1}. The IR1161 then turns the gate off and current will again start flowing through the body diode causing the V_{DS} voltage to make a sharp negative transition. Depending on the amount of residual current, V_{DS} may once again exceed the turn on threshold V_{TH2}. For this reason re-triggering is disabled after the gate drive has been switched off until the controller has re-armed.

The re-arming sequence requires V_{DS} to cross the V_{TH3} threshold and remain above it for a period denoted as t_{BRST}. If this does not occur, the gate drive will remain low for a period of t_{BLANK}, after which time re-arming will occur automatically.

To achieve high system efficiency and low standby loss at the same time, the IR1161 incorporates a programmable minimum on time. This feature offers flexibility in various applications at different switching frequencies. The MOT function determines the shut-down point at light load. During normal operation, the designer sets the minimum on time to be shorter than the secondary conduction period. At progressively lighter loads, the conduction period reduces until it eventually becomes shorter than the MOT. If the IR1161 detects no voltage drop signifying no SR drain current the MOT protection function causes the gate drive to remain off for the next cycle. MOT protection operates whether or not the SR gate drive is active or whether conduction is through the body diode. In this way the IR1161 does not drive the gate at light loads and therefore consumes minimal power improving system efficiency.

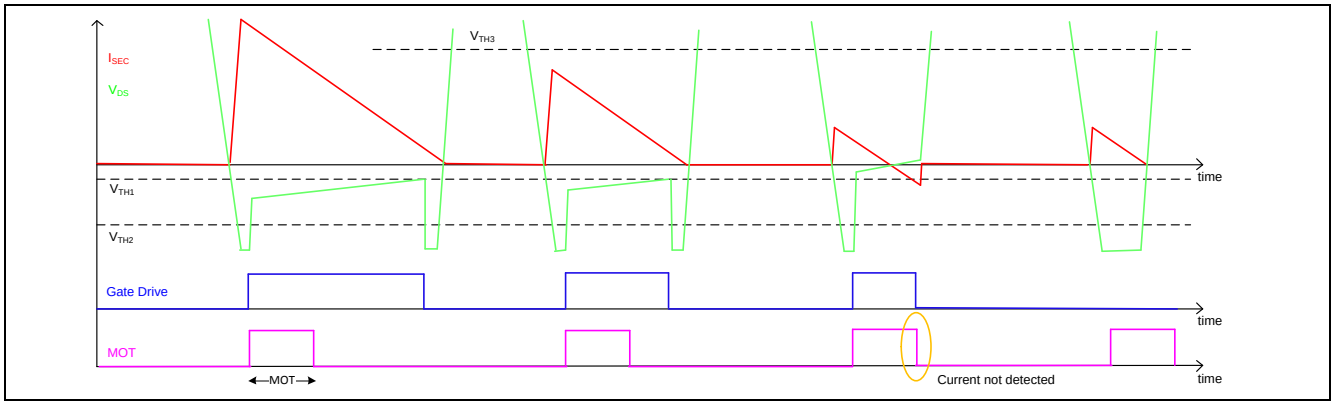


Figure 5 MOT protection as load decreases

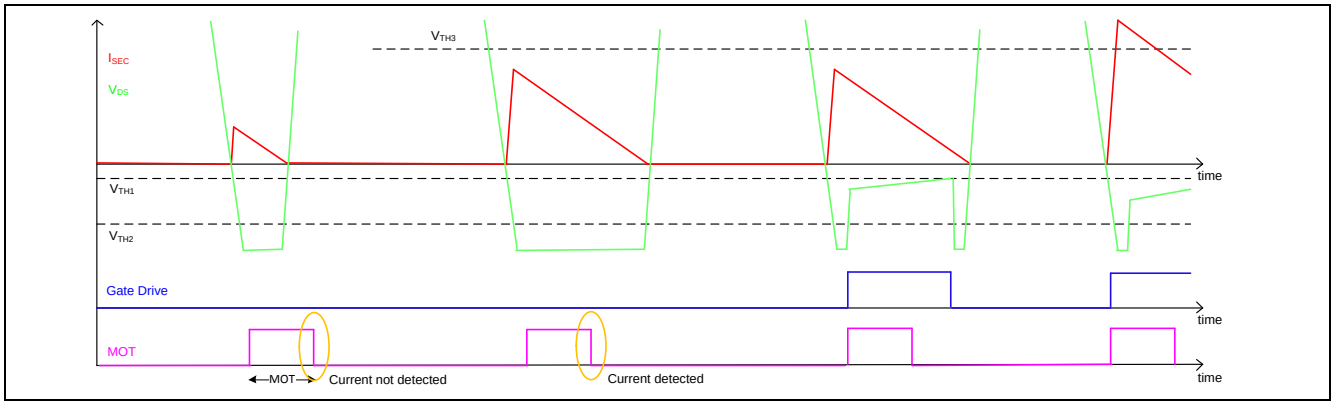


Figure 6 Gate drive resuming as load increases

3 Design and selection of passive components

3.1 IR1161 VCC supply and current consumption

The IR1161 may be biased from the output voltage if V_{OUT} falls within the range of 4.75 V to 20 V. A small RC filter is recommended between V_{OUT} and V_{CC} for noise filtering. A decoupling capacitor of at least 1 uF is necessary to prevent noise from interfering with the correct operation of the IR1161. Although the IR1161 accepts up to 20 V supply voltage, it is suggested in higher output voltage systems to limit the supply voltage to 12 V ~ 15 V where a standard SR MOSFET is used. This reduces gate drive switching losses since the gate drive output is not internally clamped. The following simple voltage level shift circuit supplies Vcc from V_{OUT}. V_{CC} is determined by V_{OUT} minus the value of $V_Z + V_{BE}$ with typically 0.5 V drop on R1. On startup as V_{OUT} rises it must exceed $V_Z + V_{BE} + 0.5 + V_{CC\_ON}$ before the IR1161 gate drive is enabled. This prevents possible shoot through from occurring due to the gate potentially being switched on due to ringing oscillations during start up.

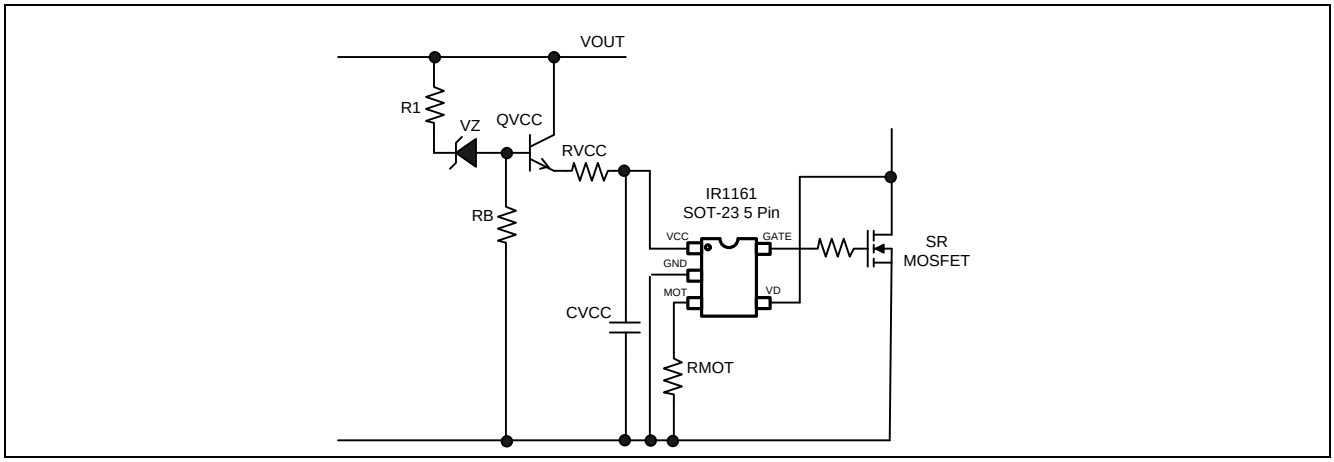


Figure 7 Simple VCC level shift supply circuit

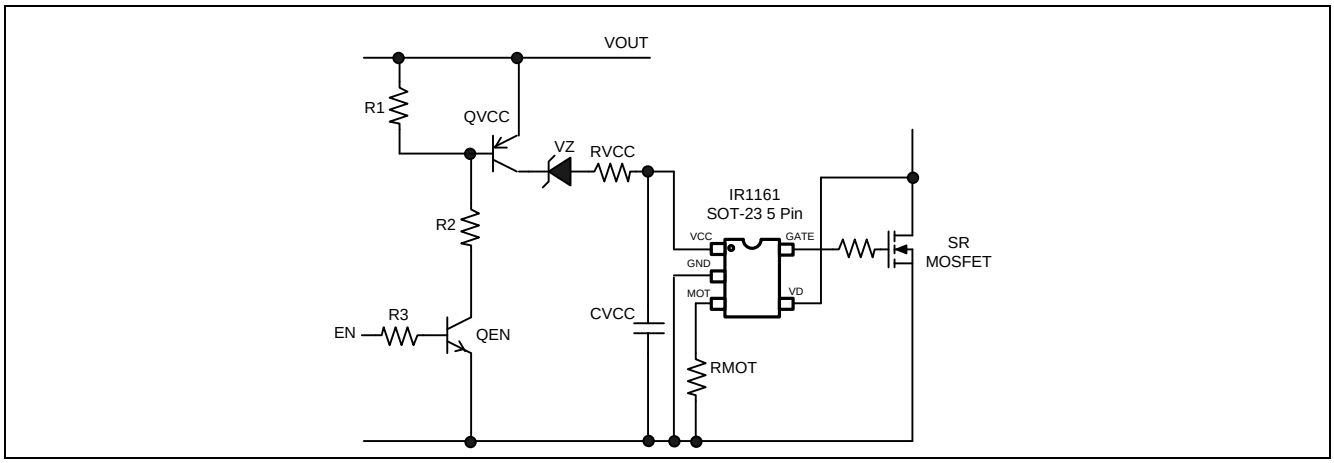


Figure 8 VCC level shift supply circuit with external logic level enable

The IR1161 can be disabled and placed in low power standby by removing Vcc as shown above in figure 8. The circuit above combines V_{IN} to V_{CC} voltage step down with an enable function from the logic level EN input. Power dissipation for 25 V input and 12 V V_{CC} is ~70 mW, mainly in the zener diode during operation and zero during shutdown. This is based on a typical I_{CC} of 5 mA as quoted in the datasheet.

Design and selection of passive components

In some applications, it is preferred to place the synchronous rectifier circuit at the high-side to obtain a better grounding connection. In this case an auxiliary winding must be available on the Flyback transformer to provide a floating bias supply V_{CC} to the IR1161. One implementation is shown below:

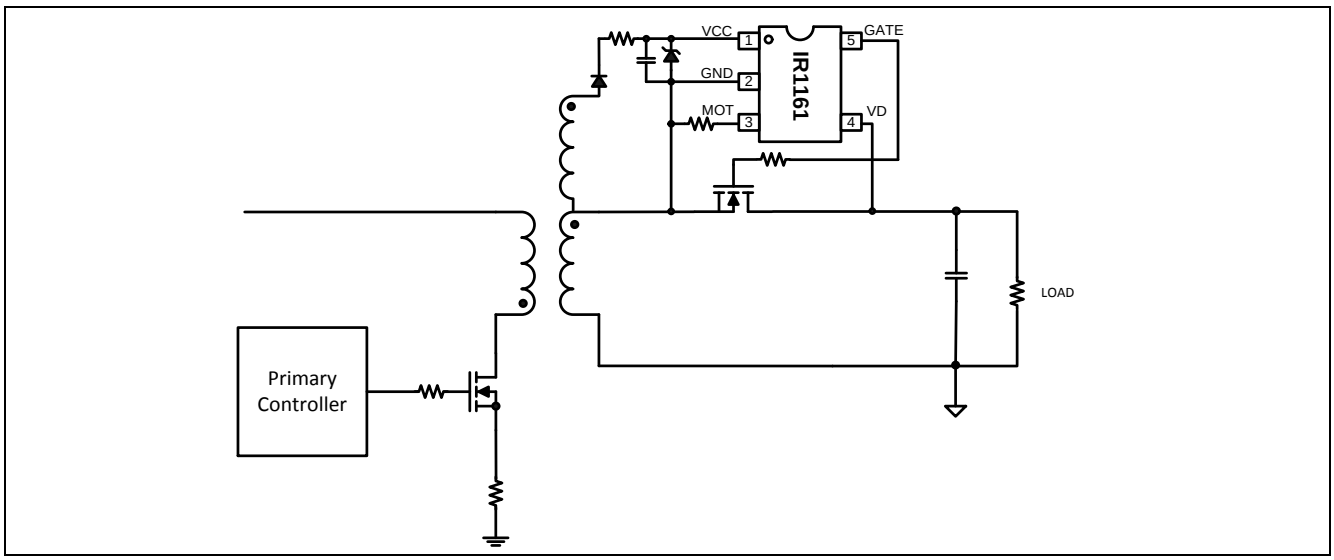


Figure 9 High-side connection with auxiliary winding to bias the IR1161

To calculate IR1161 current consumption the gate charge of the SR MOSFET needs to be determined. The secondary current initially flows through the body diode resulting in a low source to drain voltage drop, therefore turn on will occur in ZVS mode. This applies in DCM or QR/CrCM mode. In zero-voltage switching operation the MOSFET behaves like a constant capacitance load (C_{sync}) connected to the IC gate drive output.

The following diagram shows how the normal gate characteristics (Magenta) change when the switch is turned on at zero voltage (Blue). The gate plateau is effectively eliminated:

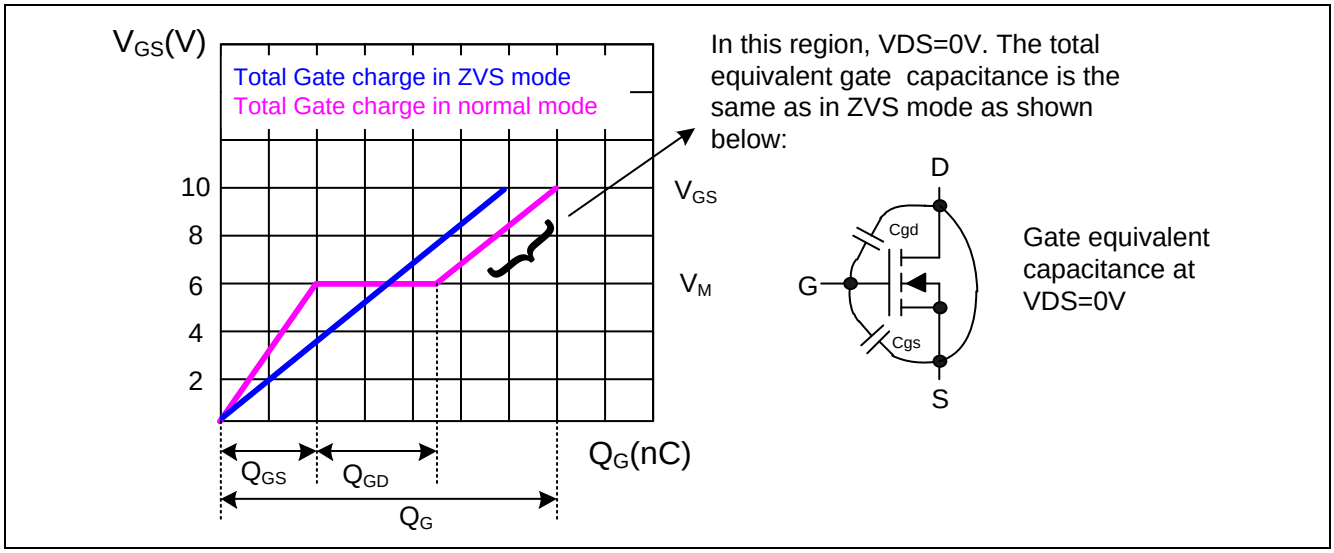


Figure 10 MOSFET gate equivalent capacitance in ZVS mode

$$C_{sync} = \frac{(Qg - Qgd - Qgs)}{Vgs - Vm}$$

V_{GS} is the gate voltage where Q_G, Q_{GD} and Q_{GS} are tested. In most datasheets it is specified as 10 V. V_m is the Miller plateau voltage. If two or more MOSFETs are connected in parallel, the above capacitance is multiplied by the number of devices.

Design and selection of passive components

The IC operating current can be calculated from the following equation:

$$I_{CC} = I_{QCC} + f_{SW} C_{sync} V_{cc} + 1 \cdot 10^{-9} f_{SW}$$

where, I_{QCC} is the IR1161 quiescent current in active mode, f_{sw} is the converter switching frequency. The second term is entirely due to the synchronous MOSFET gate drive while the third term accounts for the current consumption in the IC internal control circuitry during normal operation (the factor $1 \cdot 10^{-9}$ accounts for the frequency dependent current requirements for the internal logic).

3.2 Gate resistor and IC power loss calculation

Since IR1161 based synchronous rectification turns the SR MOSFET on and off at V_{DS} levels close to zero, the gate resistor does not have an impact on the transitions and can be designed in order for the gate loop to be optimized. Oscillations should be minimized as much as possible in regular operations, therefore assuming the total gate trace loop inductance (L_G) is known, (a first order estimation can be 1 nH/mm of physical trace length), the minimum recommended gate resistor value is:

$$R_{g_{loop}} > 2\sqrt{\frac{L_g}{C_{iss}}}$$

where, C_{iss} is the switch input capacitance (from MOSFET datasheet). It is evident how a correctly optimized layout can dramatically reduce this requirement.

$R_{g,loop}$ is the total resistance in the gate charge loop:

$$R_{g_{loop}} = R_{down} + R_{gFET} + R_g$$

R_{down} is the internal pull down resistance of the IR1161 gate driver; R_{g_FET} is the internal gate resistance of the SR MOSFET and R_g is the external gate resistor.

Rearranging the equation gives:

$$R_g = R_{g,loop} - R_{gFET} - R_{down}$$

The following figure shows how increasing the gate resistor reduces oscillation when loop inductance is large due to long traces and/or MOSFET leads. The gate waveform with a 1 Ω external resistor is shown in dark green and the waveform with a 5 Ω resistor is shown in yellow. It can be seen that the 5 Ω resistor has faster overall rise time due to less oscillation.

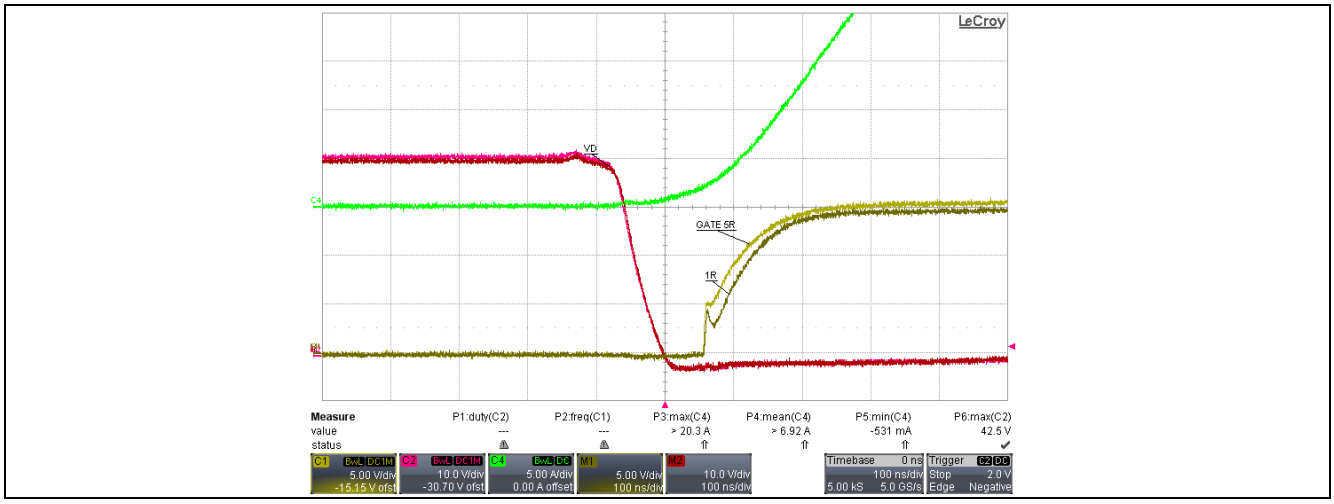


Figure 11 Gate turn-on waveform with 1 Ω and 5 Ω resistor

The energy dissipated by the gate resistor is exactly equal to the energy stored in the capacitor. The IR1161 internal gate driver resistance is in series with the external gate resistor so the power dissipation is proportionally shared.

Design and selection of passive components

The total power dissipated by the driver and the total gate resistance is given by:

$$P_{dr} = C_{sync} \cdot V_{cc}{}^{2} \cdot f_{sw,\max}$$

The driver buffer and the gate resistance will linearly share this power dissipation as described in the following relationship:

$$P_{R_g ext} = \left(\frac{R_g + R_{gFET}}{R_g + R_{gFET} + R_{Source}} + \frac{R_g + R_{gFET}}{R_g + R_{gFET} + R_{Sink}} \right) \cdot \frac{P_{dr}}{2}$$

Solving this equation with respect to $R_{g,ext}$ (which includes the external gate resistor R_g and the MOSFET internal gate resistance $R_{g,FET}$), it is possible to determine the percentage of the total driving power dissipated into the gate resistor as a function of its value. Pull up (r_{up}) and pull down (r_{down}) resistances are defined in the IR1161 datasheet. For the above calculations:

$$R_{Sink} = 2r_{down} \text{ and } R_{Source} = 2r_{up}$$

are used in order to allow for temperature shift and process variation.

The power loss in IR1161 now can be calculated as:

$$P_{IC} = Vcc \cdot Icc - P_{R_g ext}$$

It is clear that reducing supply voltage V_{CC}or increasing external gate resistor value could effectively reduce SR controller IC power dissipation.

3.3 MOT resistor calculation

The MOT is linear in relation to the resistor value R_{MOT}, therefore the following formula can be used to determine the required value:

$$R_{MOT} = 5 \cdot 10^{10} t_{MOT}$$

The value of R_{MOT} should not be lower than the minimum recommended on the datasheet.

3.4 Thermal Verification

Thermal verification is based on calculated power dissipation in the IR1161. SOT23-5L is a small package and the thermal performance strongly depends on PCB layout. For the SOT23-5L package in free air, the thermal resistance between junction and ambient can be as high as 427°C/W. It will drop to 212°C/W when the IC is soldered on 14 mm by 11.5 mm two-layer PCB using a standard footprint. Thus sufficient PCB area is required for IR1161 heat dissipation.

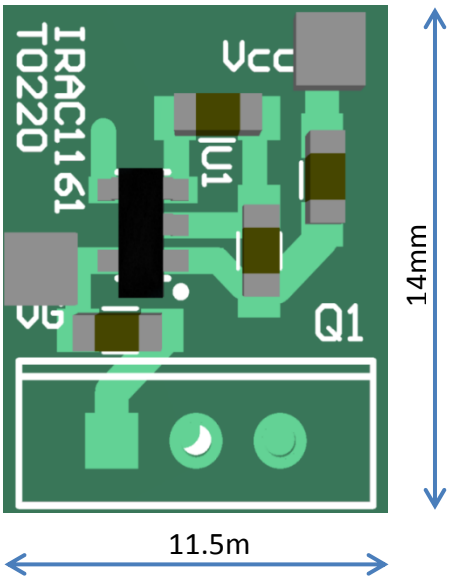


Figure 12 IR1161 TO-220 daughter card layout

Using the junction to ambient thermal resistance, the maximum ambient temperature (where ambient refers to the environment in which the IC will work, i.e. box, PCB etc.) and the IC maximum power dissipation, it is possible to calculate the maximum junction temperature of the IR1161 package. The thermal resistance quoted in the datasheet is based on 11.5 mm x 14 mm 2-layer PCB with standard SOT23-5L footprint.

$$T_{J\max} = P_{IC_{\max}} R_{\Theta JA} + T_{IC\_amb}$$

If the maximum junction temperature exceeds the system design target it will be necessary to either; reduce the total power dissipation by reducing V_{CC} voltage or increasing the gate drive resistor R_g, or reduce thermal resistance by increasing the PCB area or increasing the Copper area of the GND trace.

4 SR MOSFET Power Loss Calculation and Device Selection

The power loss in the SR MOSFET is the sum of conduction loss, switching loss, and gate driver loss. This application note focuses on the power loss calculation in a Flyback converter operating in DCM or quasi-resonant (QR) also known as critical conduction (CrCM) mode, where the secondary synchronous rectifier is switched on and off at zero voltage (ZVS condition) resulting in zero switching loss.

Conduction loss can be broken down into channel conduction losses and body diode conduction losses. The conduction period is illustrated in Figure 15, refers to schematic of Figure 14. T_{b1} and T_{b2} are the body diode conduction phase and T_C is the channel conduction phase.

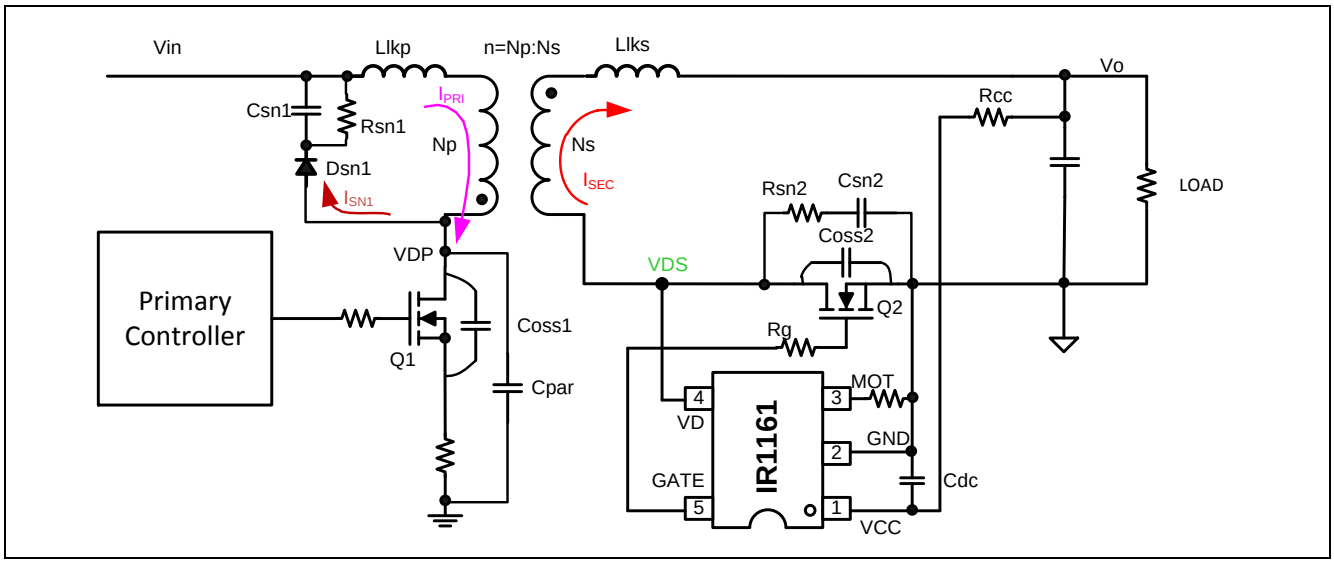


Figure 13 Typical Flyback converter with parasitic capacitance (Parasitic capacitor Cpar includes transformer cancellation inter-winding capacitance and snubber capacitance between the Drain of Q1 and Ground if included in the circuit)

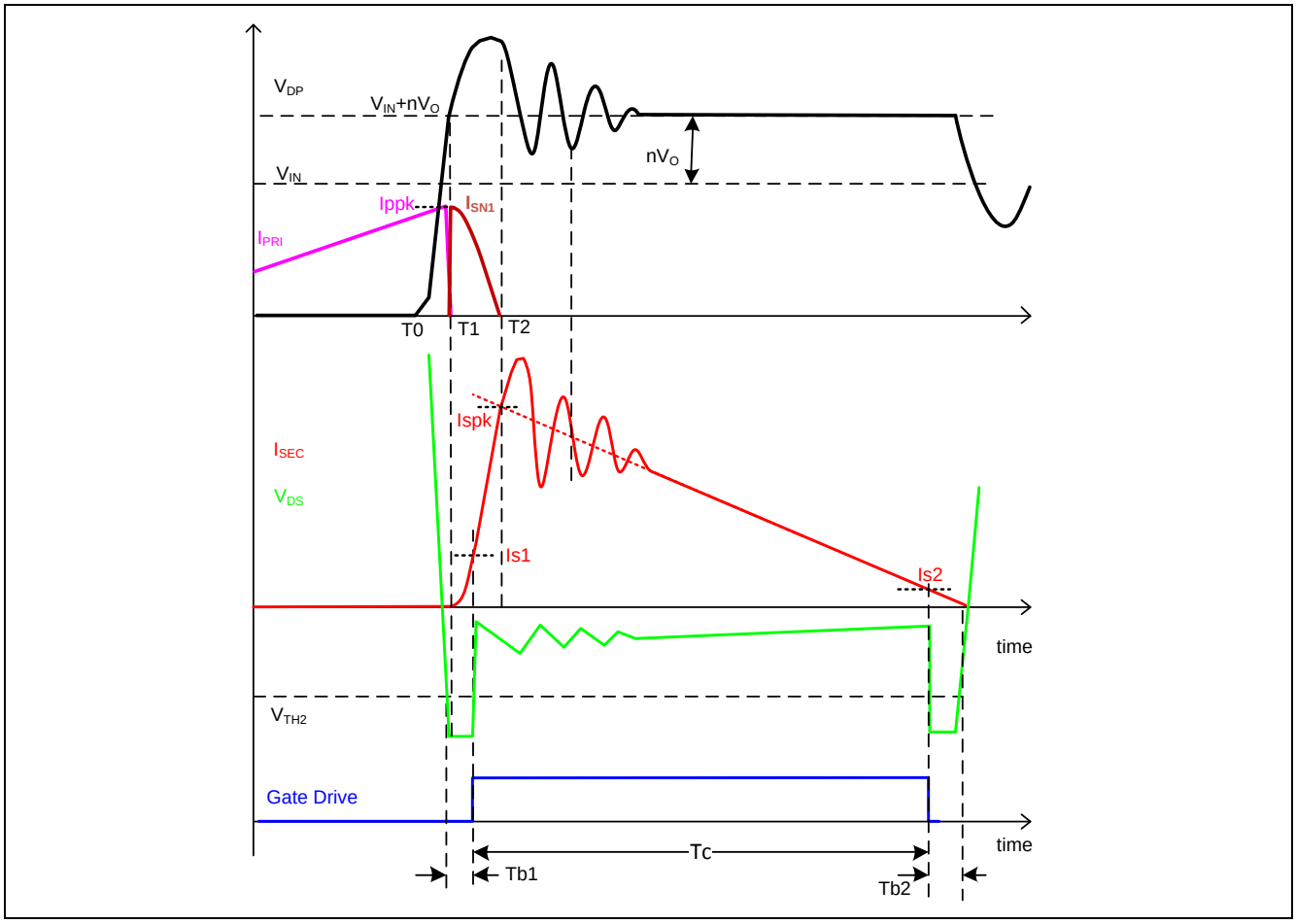


Figure 14 SR MOSFET conduction waveform

4.1 Body diode conduction loss at turn-on

The power loss in the first body diode conduction phase can be calculated by:

$$P_{body1} = \frac{1}{2} \cdot T_{b1} \cdot f_{SW} \cdot V_F \cdot I_{S1}$$

T_{b1} is approximate the turn-on propagation delay of the IR1161 (TDon in the datasheet). If additional turn-on delay is applied in circuit or a large gate resistor is used, the additional turn-on delay and gate rising time should be considered in calculating T_{b1}.

V_F is the body diode forward voltage drop and Is1 is the secondary current value at the time IR1161 gate turns on.

At the time when the primary switch turns off, the voltage at the primary MOSFET drain increases as shown by the black trace in Figure 14. From T_0 to T_1, C_{oss1} of the primary MOSFET Q1 and the parasitic capacitor C_{par} are charged by the primary peak current I_{ppk}. The secondary parasitic capacitance C_{oss2} of Q2 and the snubber capacitor C_{sn2} are then discharged. Usually the voltage on the snubber capacitor C_{sn1} is higher than the transformer reflected voltage nV_o, therefore D_{sn1} is reverse blocked and C_{sn1} does not contribute to the rise time during T_0 to T_1. At time T_1, the primary drain voltage V_{DP} reaches $V_{in} + nV_o$. C_{oss2} and C_{sn2} are discharged to zero voltage and the body diode of the SR MOSFET Q2 starts conducting current.

From T_1 to T_2, primary drain voltage is rises to a voltage higher than the voltage on snubber capacitor C_{sn1}, the primary snubber diode is conducting and C_{sn1} started to be charged. Transformer leakage inductance resonates with C_{sn1}, C_{oss1} and C_{par}. The resonant period can be calculated by:

$$T\_res1 = 2 \cdot \pi \sqrt{L_{lkp} \cdot \left(C_{sn1} + C_{oss1} + C_{par}\right)}$$

At T_2 the primary drain voltage reaches its peak, which is determined by transformer leakage inductance and the snubber elements C_{sn1}, R_{sn1}. The secondary current reaches the ideal peak current I_{Spk}.

Assuming the snubber capacitor C_{sn1} is being charged when the primary drain voltage reaches $V_{in} + nV_o$, the T_2-T_1 time interval is obtained as follows:

$$dT = T2 - T1 = \frac{T\_res1}{4} = \frac{1}{2} \cdot \pi \sqrt{L_{lkp} \cdot \left(C_{oss1} + C_{par} + C_{sn1}\right)}$$

The first body diode conduction phase of the IR1161 (T_{b1}) usually falls into the T_1~T_2 resonant period. I_{s1} current is obtained by:

$$I_{S1} = I_{Spk} \cdot [1 - \cos\left(\frac{Tb1 \cdot 2\pi}{T\_res1}\right)]$$

For DCM or QR Flyback, the primary and secondary peak currents are calculated by the following:

$$I_{Ppk} = \sqrt{\frac{2 \cdot P_{in}}{L_p \cdot f_{SW}}}$$

$$I_{Spk} = n\sqrt{\frac{2 \cdot P_{in}}{L_p \cdot f_{SW}}} = \frac{N_p}{N_s}\sqrt{\frac{2 \cdot P_{in}}{L_p \cdot f_{SW}}}$$

Here L_p is the transformer primary magnetizing inductance and P_{in} is the converter input power. The transformer primary to secondary turns ratio (N_p:N_s) is denoted by n, where N_p is the transformer primary turns and N_s is the transformer secondary turns.

he MOSFET C_{oss} is not a fixed capacitance but is actually V_{DS} dependent exhibiting a non-linear relationship with the V_{DS} voltage. The charging of C_{oss} is usually simplified with an equivalent capacitance. Most MOSFET datasheets specify the effective value of C_{oss} at 80% of rated voltage. For the timing calculation, the time related effective value according to the datasheet should be used. As the actual V_{DS} voltage in a real application is not usually exactly 80% of V_{BRDSS}, a more accurate calculation of $T_{\_res1}$ should be based on the time equivalent of C_{oss} at the actual V_{DS}.

Note that the peak current Ispk here refers to secondary peak current in an ideal case (see the dotted red line in figure 14) and that the actual peak current is higher than I_{spk} due to resonant action. In the worst case the actual peak current could be as much as twice Ispk. This depends on the snubber and damping circuit so the actual secondary peak current will reach somewhere between I_{spk} and 2 x I_{spk}.

4.2 Channel conduction loss:

The IR1161 has a very low turn-off threshold V_{th1} to achieve nearly zero current turn-off. To simplify the calculation without introducing significant error it is acceptable to consider the channel to be turned on during the entire secondary current conduction time:

$$P_{ch} = Isrms^2 \cdot R_{DS(on)}$$

$R_{DS(on)}$ is the MOSFET on state resistance $R_{DS(on)}$, which is normally shown in the datasheet at 25ºC. This would be approximately 1.5 times higher at Tj=100 ºC, which should be assumed for channel conduction loss calculations.

I_{srms} is output RMS current and can be calculated by:

$$I_{srms} = \frac{2 \cdot Io_{av}}{\sqrt{3.D_{SEC}}}$$

In this formula, Ioav is the converter output average current and DSEC is the secondary conduction duty-cycle, given by:

$$D_{SEC} = \frac{2 \cdot Io_{av}}{I_{Ppk} \cdot n}$$

4.3 Body diode conduction loss at turn-off

T_{b2} is the second body diode conduction time. This is included in the channel conduction time in the above P_{ch} calculation because the T_{b2} body diode conduction loss is not negligible in some conditions. For example, if a through-hole packaged MOSFET with low $R_{DS(on)}$ is used, the turn-off body diode conduction loss should be taken into account. As illustrated here, the parasitic inductance in series with MOSFET creates a voltage drop due to changing current (di/dt), which can degrade the accuracy and effectiveness of the voltage-sensing control technique of the SR controller. Though the designer should always optimize the PCB layout to obtain a Kelvin connection to the MOSFET, there are some limitations based on the device package. Generally through-hole packages like TO-220 and TO-247 have larger stray inductances than surface mount packages such as QFN, SO-8 and DirectFET. Even a small inductance can cause a voltage drop in the range of the IC's threshold levels with the di/dt values present in this application, which could in turn trigger the IR1161 to turn-off the gate before the drain current drops to $V_{th1}/R_{DS(on)}$ as in the ideal case.

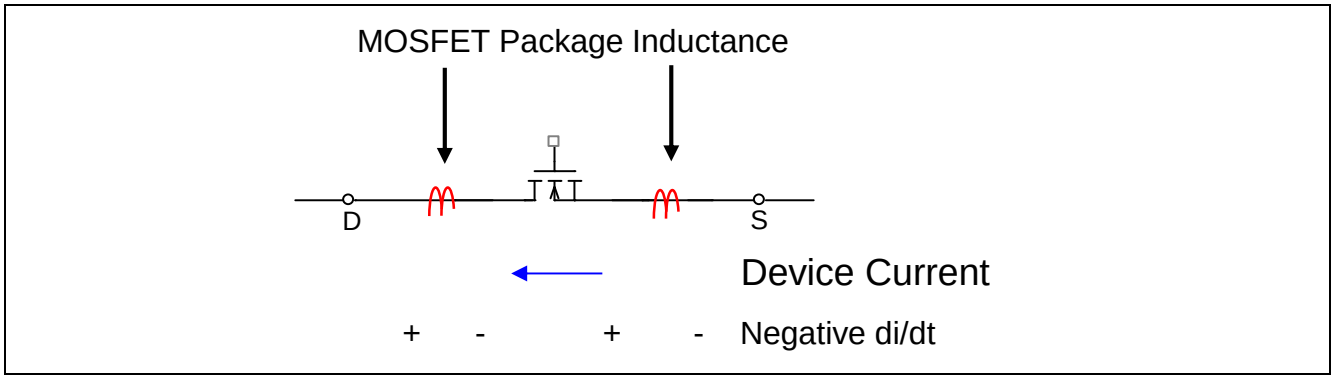


Figure 15 MOSFET package inductance

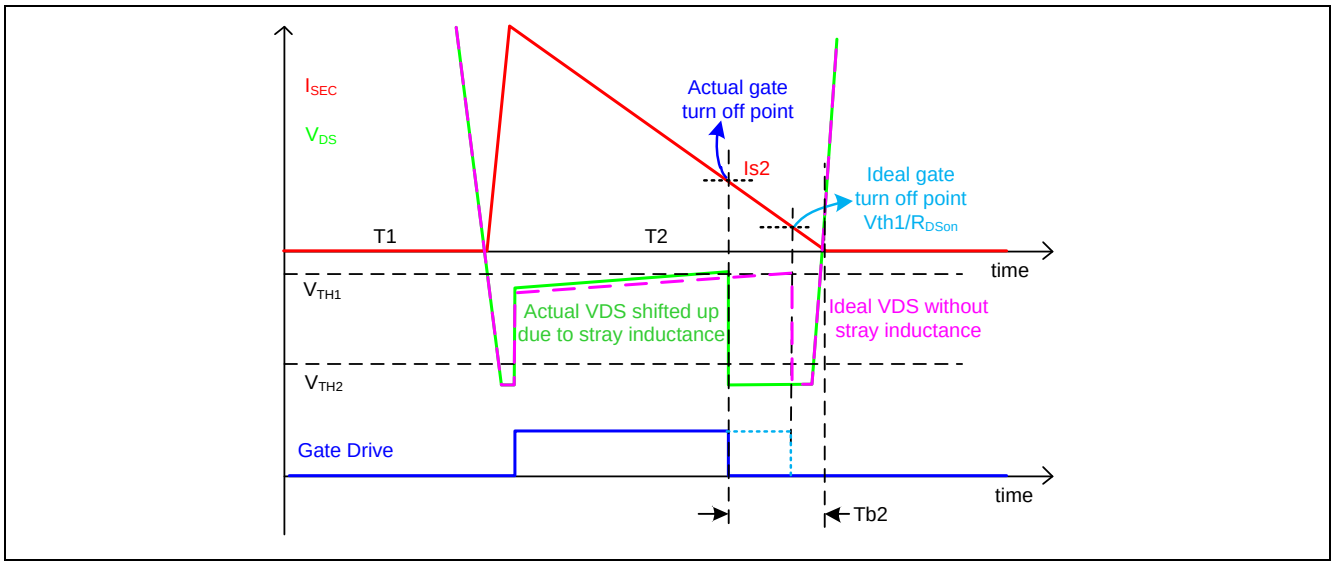


Figure 16 IR1161 waveform with parasitic inductance

The offset voltage generated by parasitic/stray inductance can be calculated by the secondary current di/dt slope and the stray inductance (LSTRAY).

SR MOSFET Power Loss Calculation and Device Selection

$$V_{OFFSET} = \frac{di}{dt} L_{STRAY}$$

The actual gate turn-off current I_{S2},

$$I_{S2} = \frac{V_{th1} + V_{OFFSET}}{R_{DSon}} - T_{Doff} \cdot \frac{di}{dt}$$

$$\frac{di}{dt} = \frac{I_{Spk} \cdot f_{SW}}{D_{SEC}}$$

V_{th1} is the turn-off threshold of the IR1161. In the above equations the negative sign should not be included. T_{Doff} is the turn-off propagation delay of the IR1161.

Now the body diode conduction loss in the turn-off phase is calculated:

$$P_{body2} = \frac{1}{2} \cdot I_{S2} \cdot V_F \cdot T_{b2} \cdot f_{SW}$$

$$T_{b2} = \frac{I_{S2}}{di/dt}$$

The total conduction loss:

$$P_{con} = P_{body1} + P_{ch} + P_{body2}$$

The plots shown in figure 18 below, illustrate how it is not necessary to use an SR MOSFET with extremely low $R_{DS(on)}$.

Low $R_{DS(on)}$ only provides benefit when the package inductance of the SR MOSFET is also very low such as with a directFET or a QFN MOSFET with copper clip. A TO-220 MOSFET could have up to 20 nH package inductance based on the number and size of internal bonding wires. It is therefore highly recommended to carefully check the turn-off timing and the body diode conduction loss when a through-hole MOSFET is being used. The designer could select a device with higher $R_{DS(on)}$ if the body diode loss is taking a significant percentage in total conduction loss. As previously pointed out, this is due to the SR gate drive switching off prematurely thereby increasing the second period of conduction through the body diode with the resulting increased power dissipation.

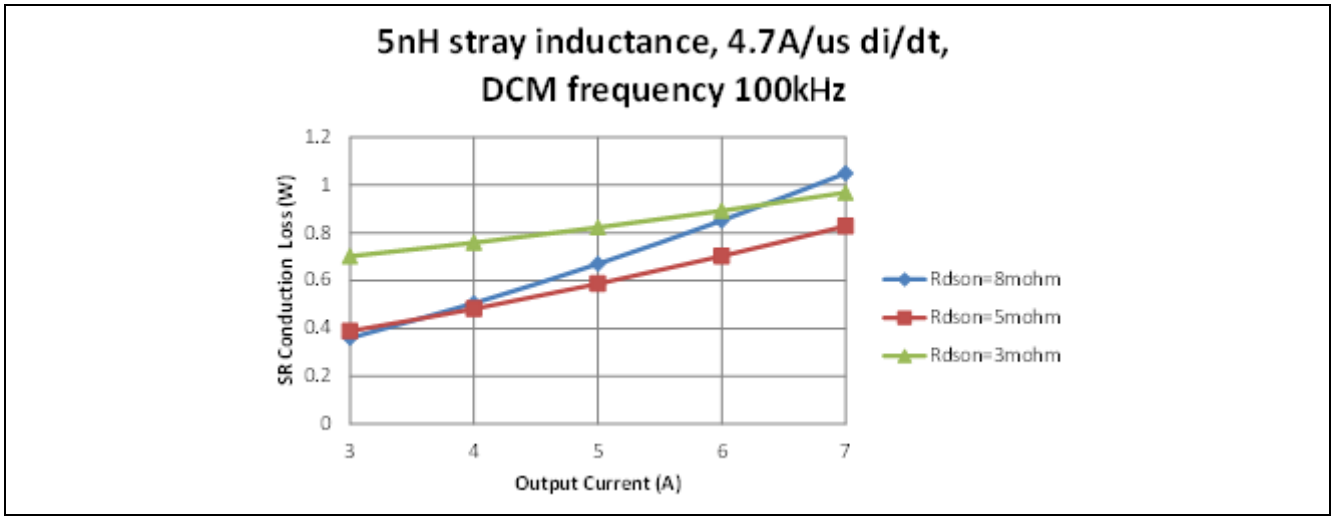


Figure 17 Total conduction loss in sync rect MOSFET vs. $R_{DS(on)}$

The total gate driver loss is discussed in section 3.2. P_{Rgext} may be used to calculate the gate drive loss that dissipated in MOSFET:

SR MOSFET Power Loss Calculation and Device Selection

$$P_{R_g FET} = \frac{R_{gFET}}{R_g} P_{R_g ext}$$

R_{gFET} is the internal gate resistance of the SR MOSFET and R_g is the external gate resistor.
Total power loss in the SR MOSFET is therefore:

$$P_{FET} = P_{con} + P_{RgFET} = P_{body1} + P_{ch} + P_{body2} + P_{RgFET}$$

5 Other Application Information

5.1 Driving a Logic Level MOSFET

An external gate drive pull down circuit is recommended when driving a logic level MOSFET.

This is because during power up and power down the drain may be switching while the IR1161 remains in UVLO.

SR MOSFET drain to gate capacitance causes voltage pulses to appear at the gate that could have sufficient amplitude to reach the turn on threshold because the IR1161 gate sink capability is limited when VCC < 2V.

The following circuit ensures that the gate voltage remains below 1 V under all conditions:

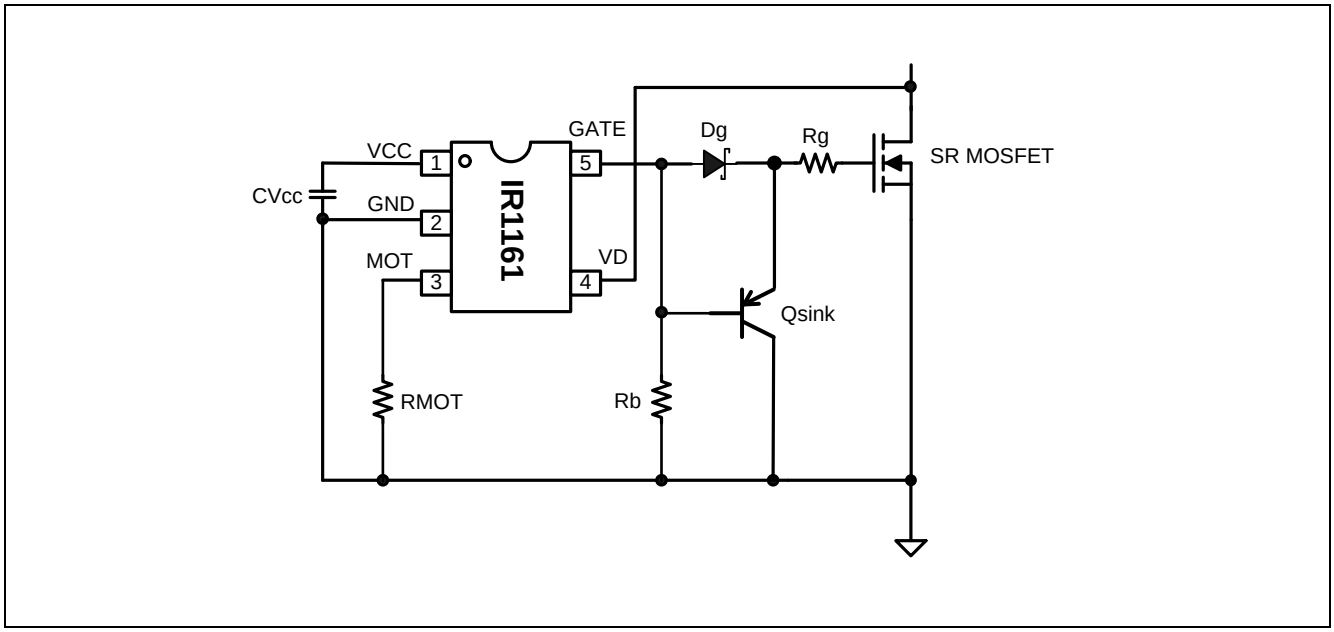


Figure 18 Gate clamping circuit for logic level SR MOSFET

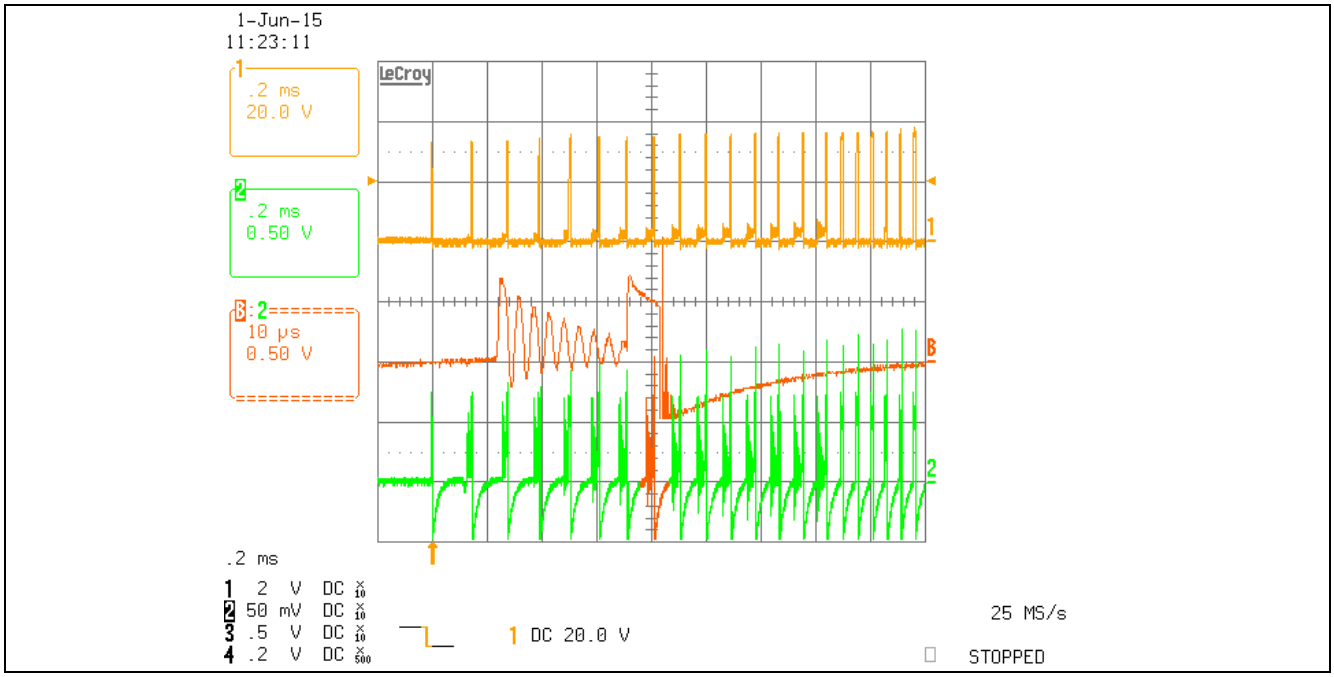


Figure 19 Gate waveform with clamping circuit during startup

The oscilloscope traces above show that the drain voltage is switching due to primary MOSFET switching, before the IR1161 V_{CC} supply has reached the startup threshold. Under this condition Q_{sink} holds the gate voltage below 1 V.

5.2 VD filter and delay

In DCM operation the secondary drain voltage rings due to the transformer leakage inductance after all of the stored energy the Flyback transformer has been delivered to the output. The resonant frequency of these ringing oscillations depends on the magnitudes of primary inductance (L_p) and parasitic capacitances (C_{oss1}, C_{oss2}, C_{sn2}, C_{sn3}). The initial amplitude of the secondary ringing is equal to the output voltage V_o plus SR MOSFET body diode forward voltage drop V_F. The ringing will be damped by the resistive elements in the circuit and does not therefore normally transition below zero volts at each of the valleys. However, in rare cases large body diode voltage drop and/or slow reverse recovery of the body diode can potentially drive the V_{DS} ringing negative peak below the turn-on threshold of the IR1161 (V_{th2}). In this case the IR1161 would turn on SR MOSFET if it had previously been armed by V_{DS} remaining above V_{TH3} for longer than t_{BRST}. This would cause negative shoot though current to flow through the MOSFET from drain to source causing the output capacitor to be discharged and reducing system efficiency.

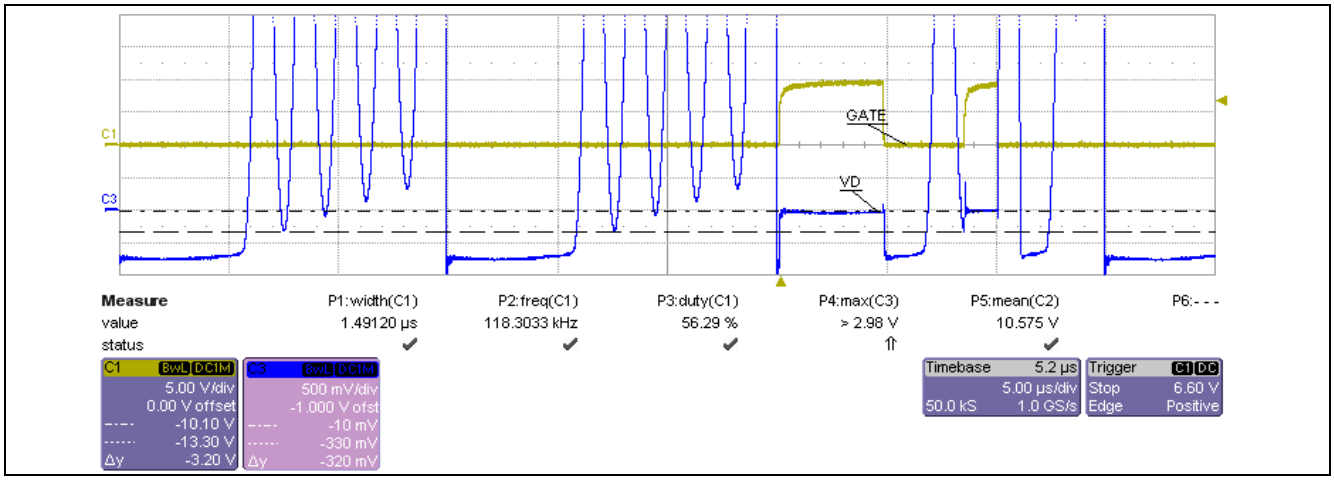


Figure 20 DCM false triggering waveform

The negative ringing effect described above does not occur in the majority of practical power supply circuits since series resistances provide sufficient damping to prevent it. Furthermore low voltage, low $R_{DS(on)}$ SR MOSFET body diode characteristics should be selected with best possible reverse recovery and lowest forward voltage.

A series RC snubber is also often connected across the SR MOSFET drain and source, which provides further damping for such high frequency oscillations.

An RC filter can also be added to the VD pin of the IR1161 as shown below. This filter introduces a small delay to reduce the amplitude of negative ringing appearing at the drain sensing input. Considering the turn-on body diode conduction loss, it is not recommended to delay the IR1161 gate turn-on by more than 200 ns. A small Schottky diode could also be added in parallel with the SR MOSFET.

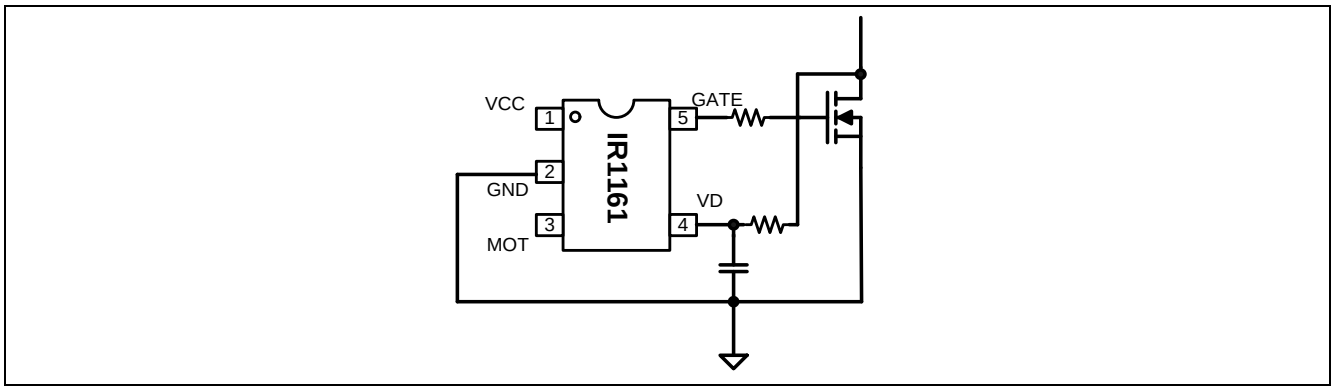


Figure 21 RC filter to VD pin

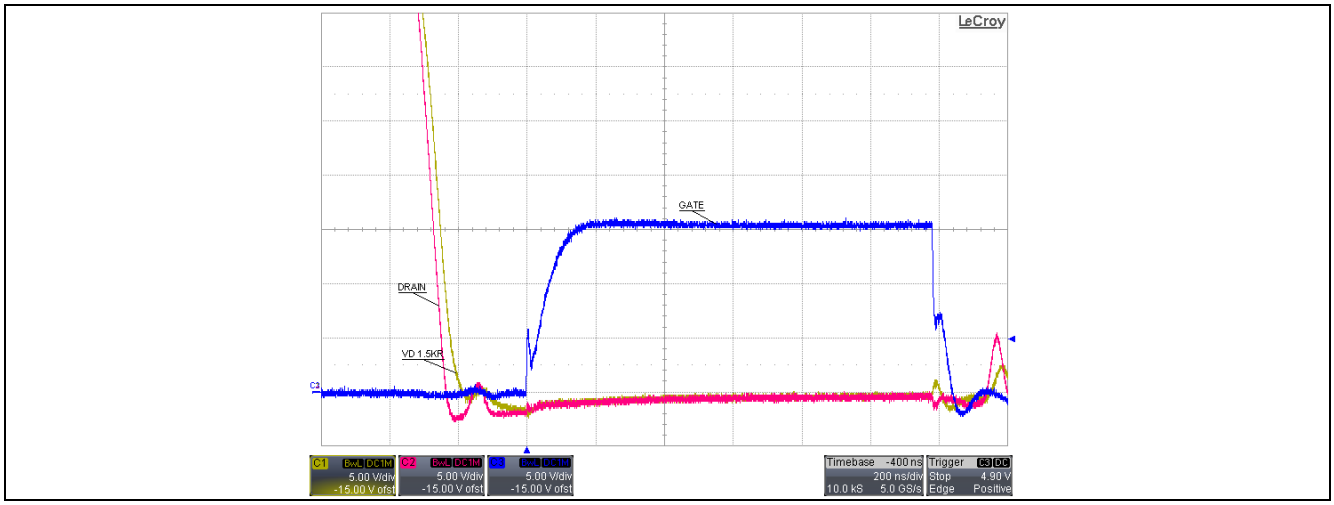


Figure 22 VD waveform with 1.5 kΩ VD resistor and IR1161 internal capacitance

6 PCB Layout Guidelines and Examples

IC placement

Due to the nature of SR control based on fast and accurate voltage sensing, it is essential that the circuit layout be optimized in order to keep the IR1161 as close as possible to the SR MOSFET. As a general guideline, the physical distance between the two devices should never exceed 10 mm (0.4 inches).

IC decoupling capacitor

The key element to properly decoupling the IC is the physical location of the V_{CC} capacitor and its connections to the power terminals. In order for this capacitor to provide effective filtering, it must be located as close as physically possible to the V_{CC} and COM pins and connected through the shortest available path.

Gate Drive Loop

Minimal gate drive loop will reduce requirements for damping and enhance system robustness. Gate loop inductance plays a major role in damping requirements. Once layout is finalized, then a “rule of thumb” estimation consists of measuring the physical loop trace length, assuming each millimeter (1mm = 39.37 mils) to add 1 nH of inductance. Other methods include measurement (low frequency RCL meters or current slope for a given voltage pulse) or FEM simulations.

Single layer board layout examples are shown in the following figures:

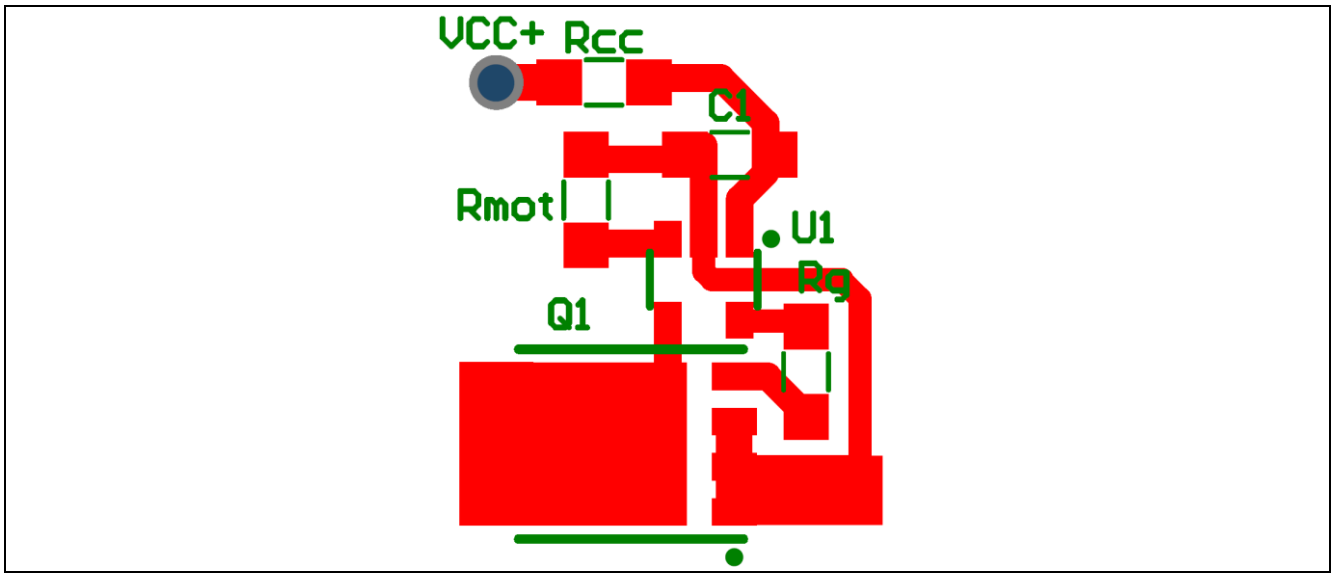


Figure 23 Single layer layout example with QFN MOSFET

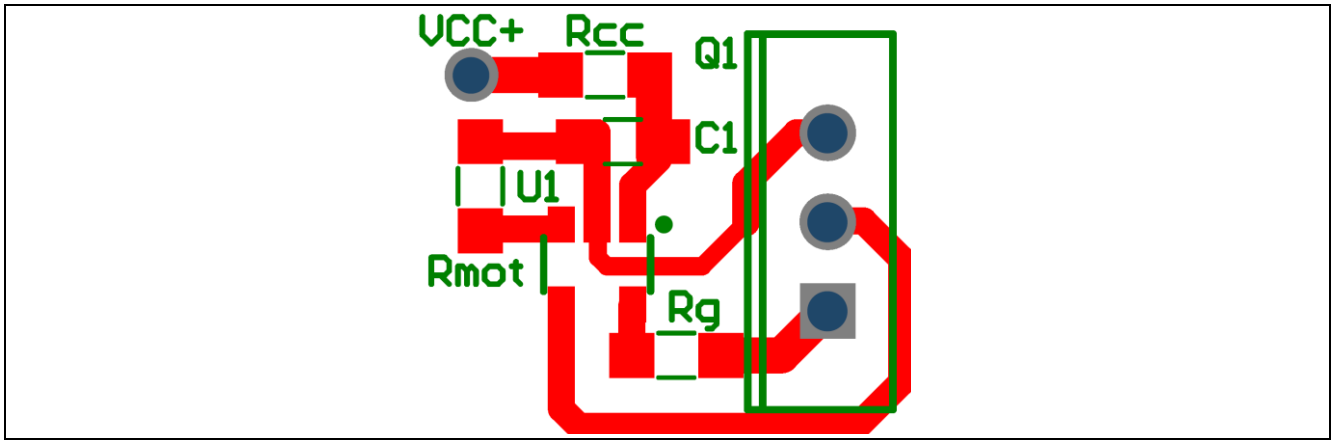


Figure 24 Single layer PCB example with TO-220 MOSFET

7 Appendix

Symbols list [1]

V_{TH1}: IR1161 turn-off threshold
V_{TH2}: IR1161 turn-on threshold
V_{TH3}: IR1161 periodic logic (reset) threshold
$R_{DS(on)}$: synchronous rectifier MOSFET channel ON resistance
I_D: synchronous rectifier MOSFET drain current
V_{DS}: synchronous rectifier MOSFET drain to source voltage
MOT: IR1161 minimum ON time parameter
t_{blank}: IR1161 turn off blanking time
C_{dc}: IR1161 decoupling capacitor on Vcc
R_g: SR MOSFET gate drive loop resistance external to IR1161 IC
R_{CC}: supply voltage series resistor value (Vsupply to VCC)
$f_{sw,max}$: converter maximum operating switching frequency
Q_g: SR MOSFET total gate charge
Q_{gd}: SR MOSFET gate to drain (Miller) charge
Q_{gs}: SR MOSFET gate to source charge
I_{QCC}: IR1161 quiescent current
L_g: total gate loop parasitic inductance
C_{iss}: SR MOSFET input capacitance
P_{dr}: Total power dissipated by the gate drive function for each SR MOSFET
R_{Source}: gate driver source resistance
R_{Sink}: gate driver sink resistance
P_{Rg}: Power dissipated in each gate resistor
P_{IC}: IR1161 IC maximum power dissipation
T_{IC_amb}: IC environment temperature (most cases is PCB temperature where IC is soldered)
$R_{\Theta JA}$: IR1161 IC junction to ambient thermal resistance
V_{CC}: Supply voltage on IR1161 Vcc pin
I_{CC}: IR1161 IC supply current
T_{Don}: IR1161 turn on propagation delay
C_{oss}: MOSFET output capacitance, time related effective

[1] IR1161 SmartRectifier™ control IC datasheet, International Rectifier.

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First Release

Appendix

Page or Reference	Description of change

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