Application Note AN-1207

Reference Design for AUIRCS3040N

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Introduction & Device Overview

This Application Note describes the AUIRDC3040, reference design board for the AUIRCS3040N AU-Convert*IR*™ Power Stage.
It is intended to provide an exemplary design, including layout guidelines, and provides results for efficiency tests, as well as few typical measured waveforms.

The AUIRCS3040N is an automotive qualified integrated power stage, including one high and low side 200V driver and two 40V - 6 mOhm mosfets (control Fet and synch Fet) in a compact PQFN 5x6mm. It is intended to operate as a step down (buck) or step up (boost) converter to convert 12V to 12V (voltage stabilizers), 24V to 12V or viceversa, in automotive applications, with up to 30A output current (step down mode) and switching frequency up to 400kHz.
It can operate with Vcc between 10 and 20V, and, when in step down mode, with input voltages between 10 and 40V and output voltages between 0 and Vin (Note 1).

Typical simplified application diagram and package outline are shown in figures 1 and 2.

The package compactness assures very low parasitic in the power stage but, to get full advantage of that, external layout has to be carefully designed.

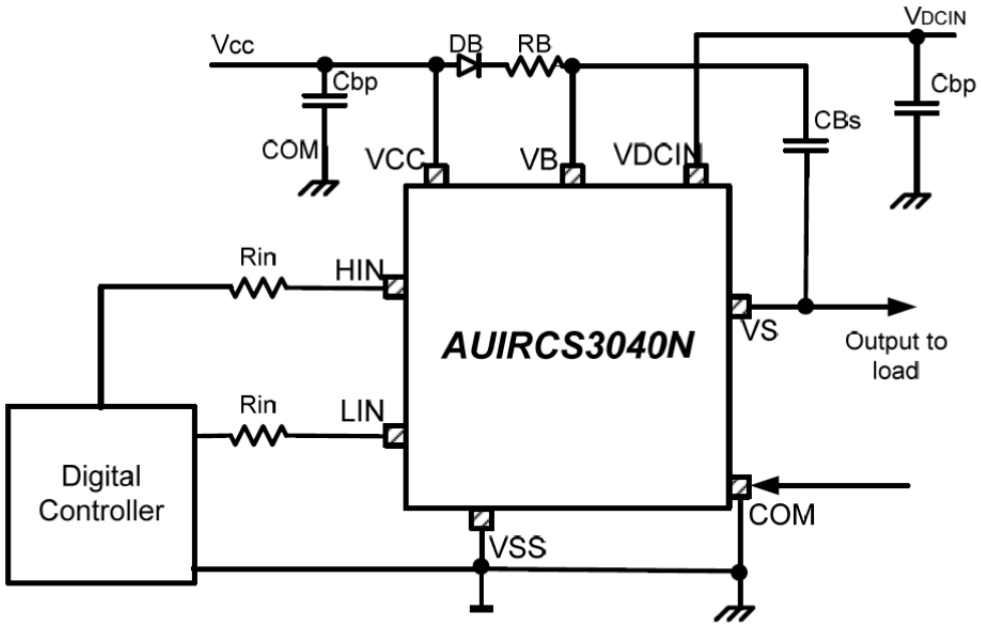


Figure 1: simplified application diagram (AU-Convert*IR*™ only)

Note 1: theoretical maximum duty cycle is 100% but it may be limited by the time needed to re-charge the bootstrap capacitor Cbs, via bootstrap network DB and RB.

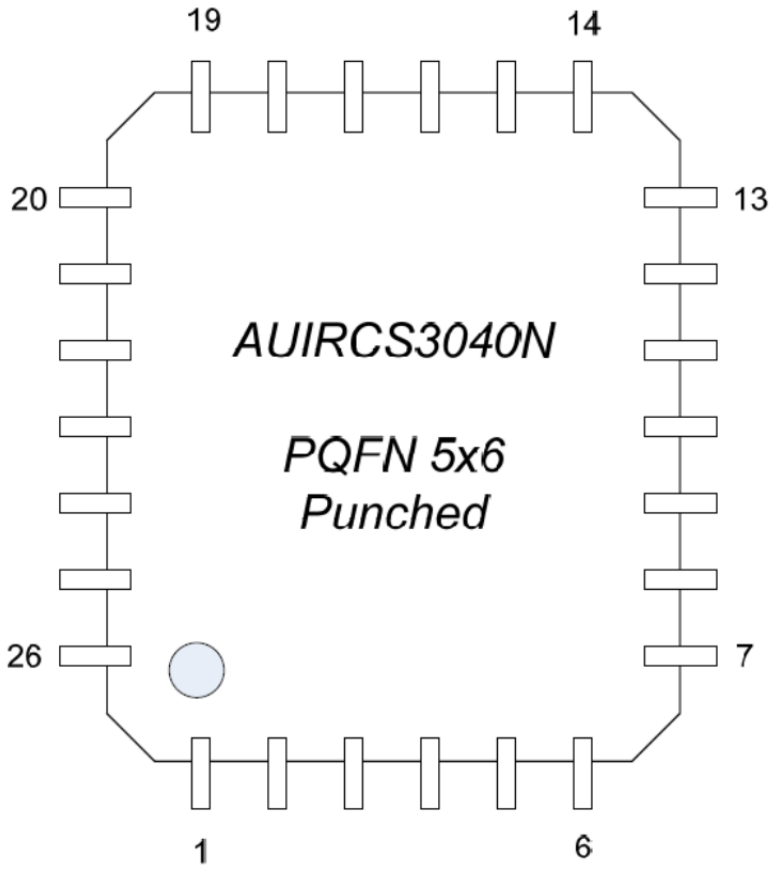


Figure 2: package outline

Reference Board description

A pictorial view of the board is shown in Figure 3.
It is very easy to use: it just needs an auxiliary power supply (10 to 20V, few mA) on Vcc, a V_{DC}-IN power supply, a load connected to the V_{OUT} and two PWM signals.
V_{DC}-IN and V_{OUT} can be exchanged between each other depending if step-down or step-up mode of operation is required.
The board is equipped with a 10uA - 25A inductor.

IMPORTANT NOTICE: the reference design board is not equipped with current limiting or shoot thru and thermal protection. Therefore, damage may occur if thermal limits are exceeded, or if PWM signals generate shoot trough between the control and the synch Fets.

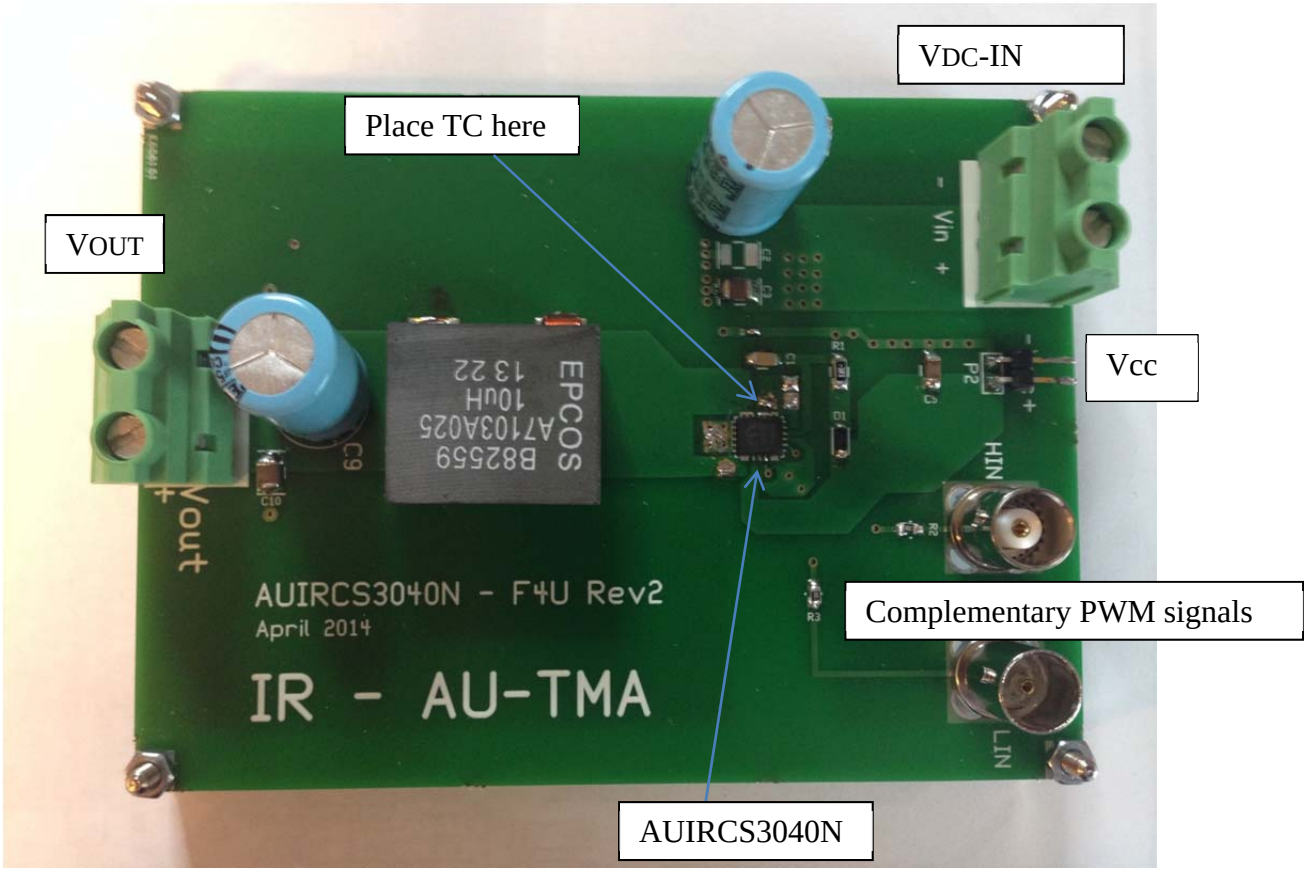


Figure 3: Reference design pictorial view.

PWM signals HIN and LIN MUST be complementary to each other (they must NOT overlap) with a MIN suggested deat time of 100nsec.
Their amplitude must NOT exceed 5Vpp (0 to 5V).
Input signals of the AUIRCS3040N are 3.3V CMOS logic compatible.

Because of the internal structure, the two hottest points during operation are close to pins 18, 20-23 (-VDCIN-) and pins 7-8 and 24-26 (VS).
Due to layout reasons, it is easier to place more pcb copper close to VS, which means the absolute hottest point is VDCIN. Thermal characterization of the board has been performed with a T-type thermocouple placed as indicated in figure 3.

Another important note is needed here. Differently from discrete components design, where the thermal limits are imposed by the junction temperature of the power devices, integrated SMT modules design thermal limits are imposed by the max pcb surface temperature, NOT by device's Tj.
Typical high Tc FR4 should not be used with a surface temperature above 130C, otherwise glass transition will occur and the pcb reliability will be impaired.
With a typical, optimised pcb design, thermal resistance pcb to ambient (Rthpcb-amb) may be as high as 20-25 C/W, while the device junction to pcb Rth is in the range of 3 C/W.

Therefore, with a Tamb of 60C, and assuming Rthpcb-amb=20C/W, the maximum power which may be locally dissipated by the pcb is:

$$P_{diss,max} = (130C - 60C) / 20[C/W] = 3.5W$$

With such power dissipation, the expected internal Tj of the control and synch fet does not go beyond

$$T_j = 130C + 3\ [C/W] * 3.5W = 140.5\ C$$

which is still well below the absolute Tj max rating (150C).

Note: the calculation of Tj needs to be better explained. When defining the Rthj-c (or Rthj-pcb) of an integrated power module, often one single device is powered, and its Tj increase is measured.
Therefore, when both devices are working and total dissipated power is 3.5W, one would expect the power dissipated by each device only being a fraction of 3.5W, and therefore its Tj being lower than the one calculated above.
This is only partially true, for two reasons:

a) in case of very low or very high Duty Cycles, most of the power is dissipated in one of the two Fets. Therefore the calculated Tj fully applies to this worst case situation

b) the two Fets are so close to each other than thermal interaction between them cannot be neglected. It is easier to think to them as a single device, dissipating the whole 3.5W power.

As said before, layout plays a very important role when using micro integrated power modules like the AUIRCS3040N.
First of all, from a thermal point of view, as discussed above: the heat dissipation occurs via the pcb so as much as possible copper should be placed close to $V_{DC}IN$ and VS terminals (some tricks to reduce Rth_pcb-amb will be described later).
Second, to get full advantage of the very low parasitics within the power stage, the rest of the converter must also have an optimised layout.

The exemplary layout of AUIRDC3040 is shown in figure 4.
Some classical rules have been followed to generate such layout:

a) signal GND plane and power GND plane isolated between each other and connected to a single GND star point,
b) superposition has been avoided between pcb tracks interested by fast changing signals (like VS) and GND power plane, to reduce parasitic capacitances,
c) ceramic capacitors between $V_{DC}IN$ and power GND are very close to the AUIRCS3040N inputs

A part from that, the biggest possible amount of copper has been placed on $V_{DC}IN$ terminals and on VS terminals.

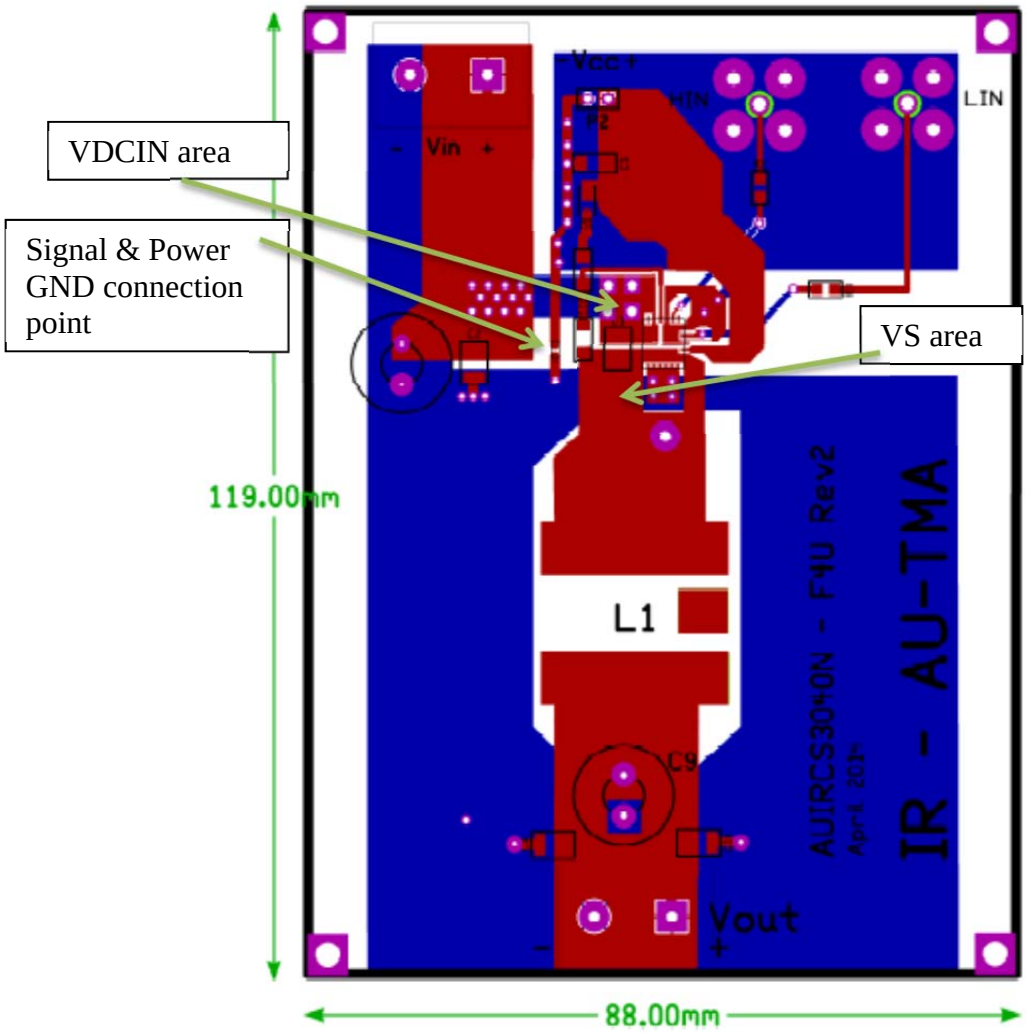


Figure 4: board layout

Copper thickness also plays a major role from a thermal viewpoint.
Suggested copper thickness is 2oz/inch2 (70um); this thickness is compatible with most manufacturing processes, by considering that the integrated power module pins width is 0.25mm (-nom-) and the clearance between pins is 0.75mm (nom).

Reference Board Design and Test Results

While the reference design board can, as said, be used as step down or step up converter, the design was approached by considering the following specifications:

Input voltage range: 16 to 32V
Ouptut voltage: 12 to 14V
Output current: 0 to 18A (recommended from 3A to 15A)
Fsw: 100kHz to 400kHz
Output voltage ripple: not critical (typical case of battery charging)
Input EMI: not considered for this reference design

The minimum average output current to get continuous conduction mode is:

$$Iavemin(Vin, Fsw) := 0.5 \cdot \left[\frac{Vo \cdot \left(1 - \frac{Vo}{Vin}\right)}{L \cdot Fsw} \right]$$

At Vin=Vin_nom=24V, Vo=Vo_nom=12V, Iout=3A and Fsw=100kHz, L turns-out to be around 10uH. A 10uH, 25A inductor has been chosen.
The reason to stay in CCM as much as possible is that this reference design does not have provisions to block the output inductor current when it becomes negative (average output current below the mask of figure 5, that is at low frequency, high inductor current ripple, low average output current). This introduces efficiency penalty at light load (DCM) conditions.
For switching frequencies between 100 and 400kHz, the minimum current to stay in CCM can be mapped as shown in figure 5.

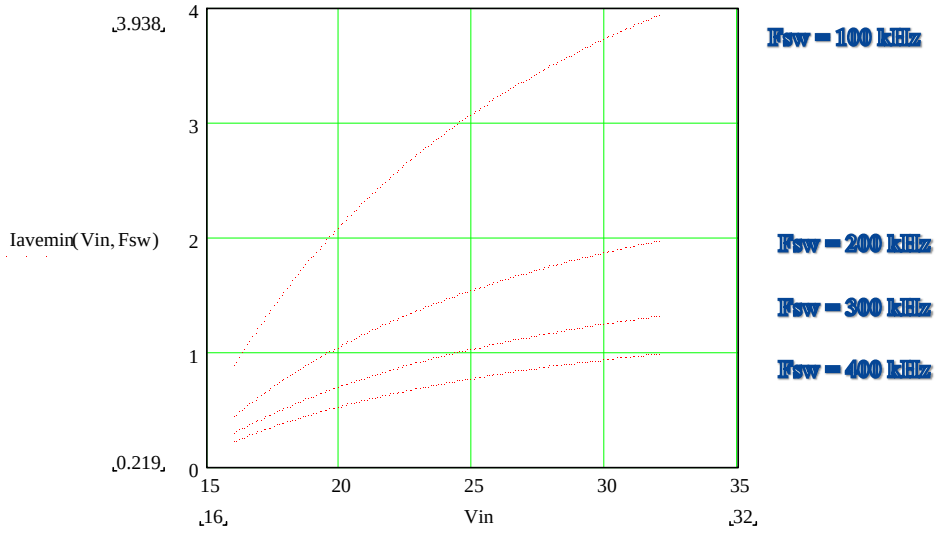


Figure 5: Min current mapping versus Vin and Fsw at Vo = 14V

Because output voltage ripple is not critical and EMI specifications not considered, input and output capacitor's design is mostly related to their self-heating due to input and output current ripples.

Worst case output current ripple (Vo = 12V) is at Fsw=100kHz and Vin=32V
It turns out to be:

$$I_{Lripplepp\_max}=7.5A$$

Actually, what is important is the RMS value of such current. For a triangular waveform, it is:

$$I_{Lrms\_max}=7.5A/\sqrt{3}=4.33A$$

Input current ripple is maximum at maximum output current and minimum input voltage. Its maximum rms value (at Vo=12V and neglecting the effect of the inductor current ripple) is then:

$$I_{INrms\_max}=13A$$

A very low ESR capacitor has then to be used, especially on the input side.
The capacitors used in this reference design are 470uF, 50V, 30mOhm ESR and 105C.
At Io=15A, Vo=12V and Vin=24V, the output capacitor will dissipate much less than 1W, but the input capacitor will dissipate around 3W.
Lower ESR and/or multiple input capacitors in parallel need to be considered for a reliable design.

Let's now see some measurement results.
First of all, efficiency of the whole board, with Vin = 24V, Vout = 12V (step-down mode), versus output current. This is shown in Figure 6, for different switching frequencies.
Please note that for Iout below about 3Adc at 100kHz, the converter will operate in DCM.

As said before, because the reference board has not provisions to block the inductor current when it becomes negative, the efficiency in DCM (light mode or light load) will be affected, and this is clearly visible in figure 6.
It is interesting to note the higher efficiency reached, at light loads and at high Fsw (200 and 400kHz): this is, of course, due to the reason that, at light loads, Rdson losses in the control and synch. switches are mostly dictated by the inductor current ripple, which is smaller and smaller as the frequency increases. At the same time, switching losses, including recovery losses of the body diodes, play a minor role at these current levels (recovery losses do not exist at all because of DCM operation).

Of course the converter efficiency depends not only on the AUIRCS3040N, but also on the power dissipated by the input capacitor and output inductor mainly, then direct measurement of the power dissipated by the AUIRCS3040N is much more interesting. This is shown in Figure 7, again versus current and for different switching frequencies.

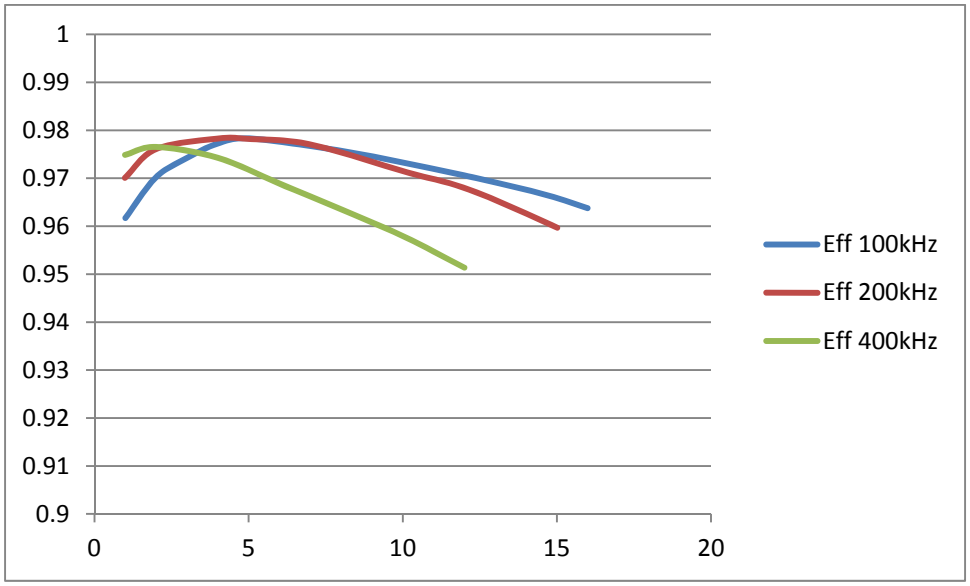


Figure 6: board efficiency vs Iout at different Fsw

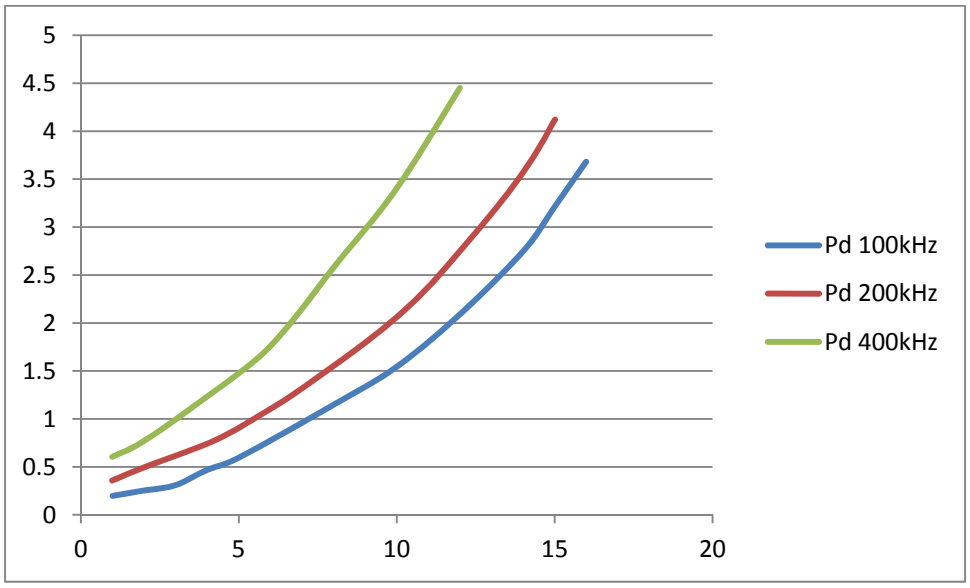


Figure 7: thermally estimated AUIRCS3040N Pdiss

Note: AUIRCS3040N dissipation includes auxiliary power (few tens mW) while board efficiency is simply Vout*Iout / Vin*Iin, not including auxiliary power. Auxiliary power only affects efficiency at very light loads.

Figure 8 show the pcb temperature (at the reference point shown in figure 3) versus current and Fsw.

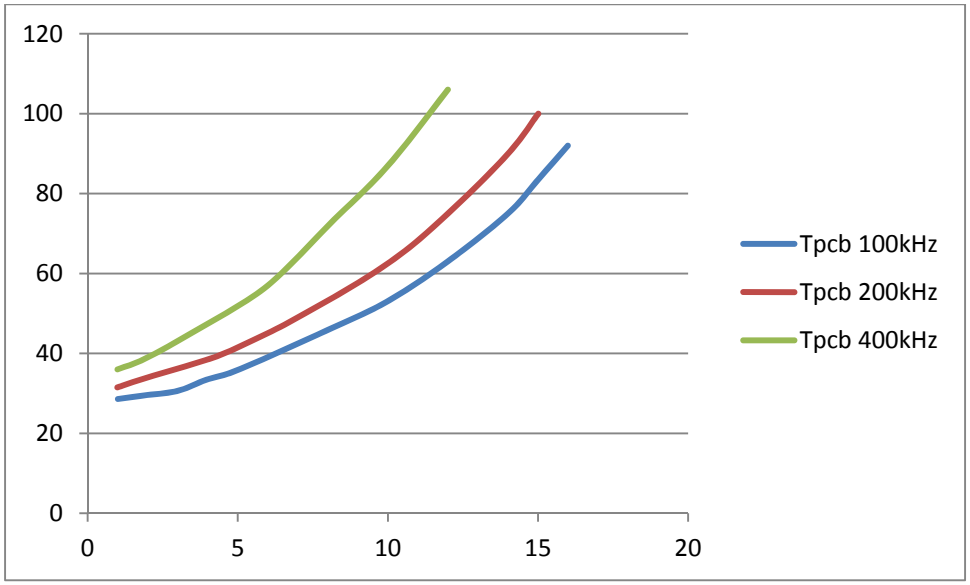


Figure 8 : Tpcb versus Iout and Fsw

Now, a small copper clip (8mm wide and 30mm long, 0.5mm thick) is soldered vertically on the VDCIN pcb vias, to increase the effective copper amount on these terminals. The vertical position also improves thermal exchange.
The pcb temperature is measured again, only at 400kHz; results are shown in figure 9.

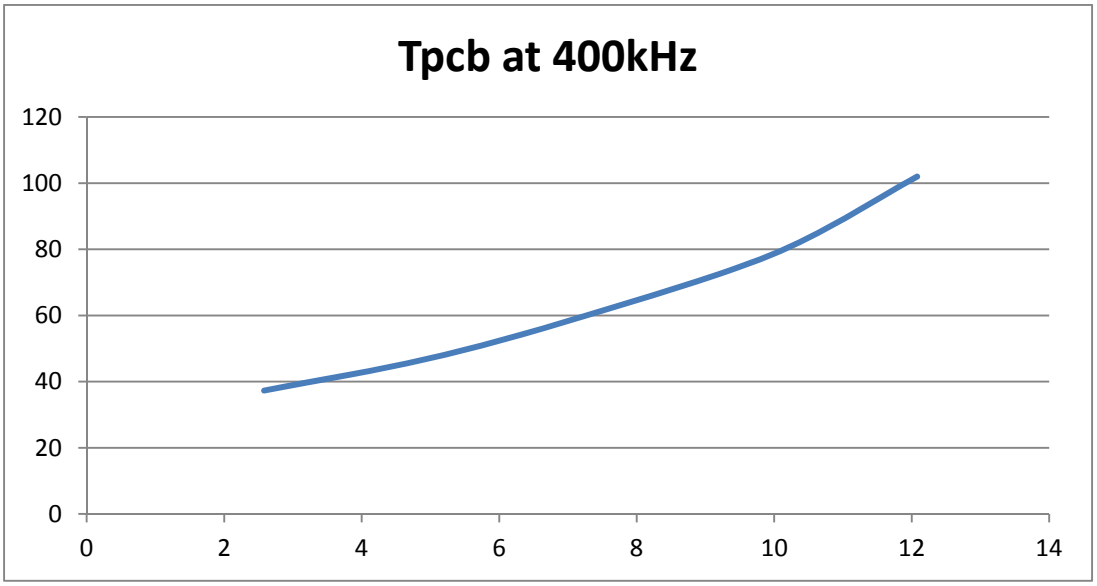


Figure 9 : Tpcb with a small vertical copper clip

At 12A, it is now possible to decrease Tpcb from 108C to about 100C.

This shows the importance of placing as much copper as possible on VDCIN terminals, and suggests that a small heatsink can improve a lot the thermal behavior of the AUIRCS3040N.

For reference, Vs and Vout ripple have been recorded at 100kHz, 10A and 400kHz, 8A. They are shown in figures 10 and 11.

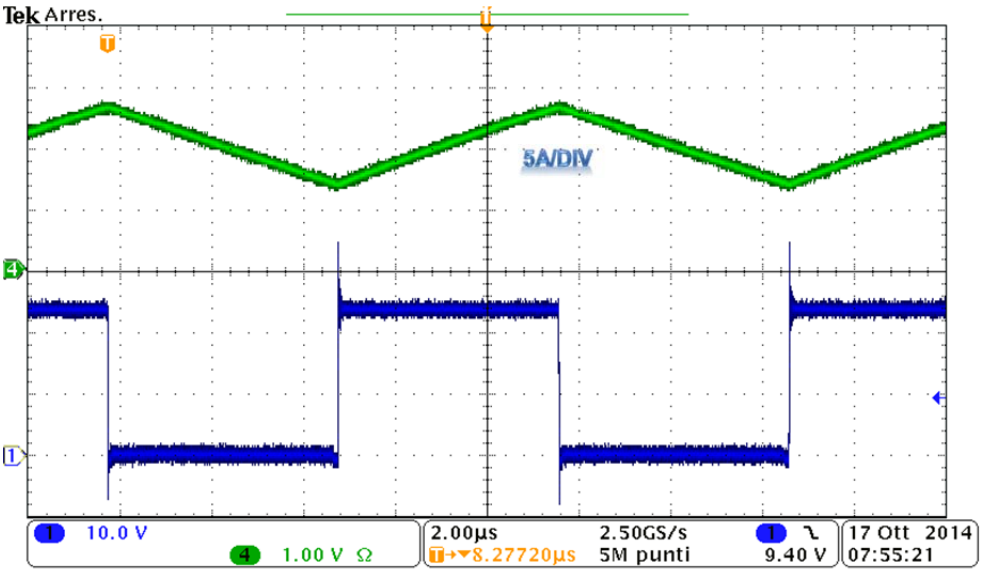


Figure 10 : Vs and Vout,ripple at 10A, 100kHz

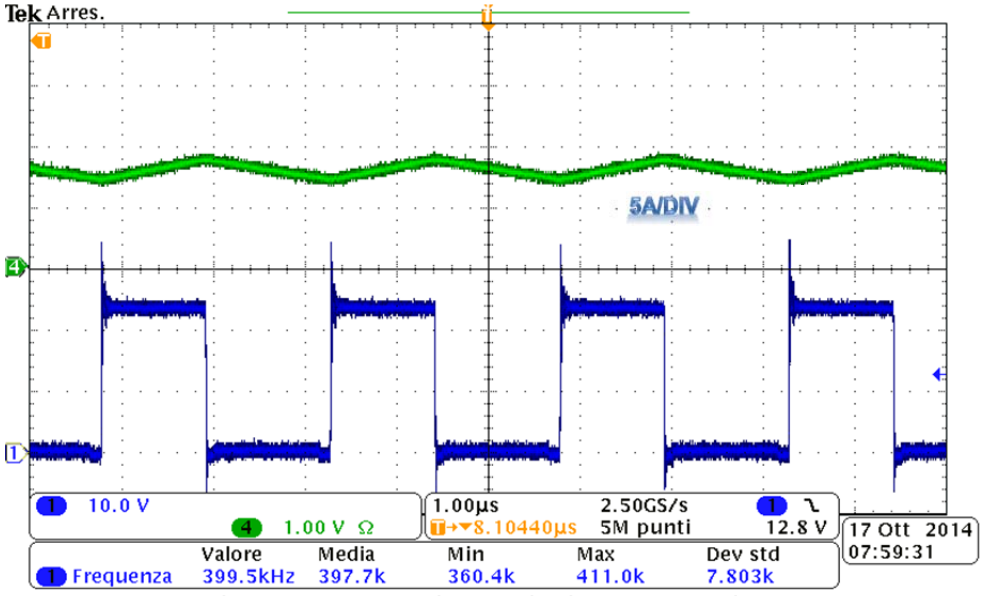


Figure 11 : Vs and Vout,ripple at 8A, 400kHz

Conclusions

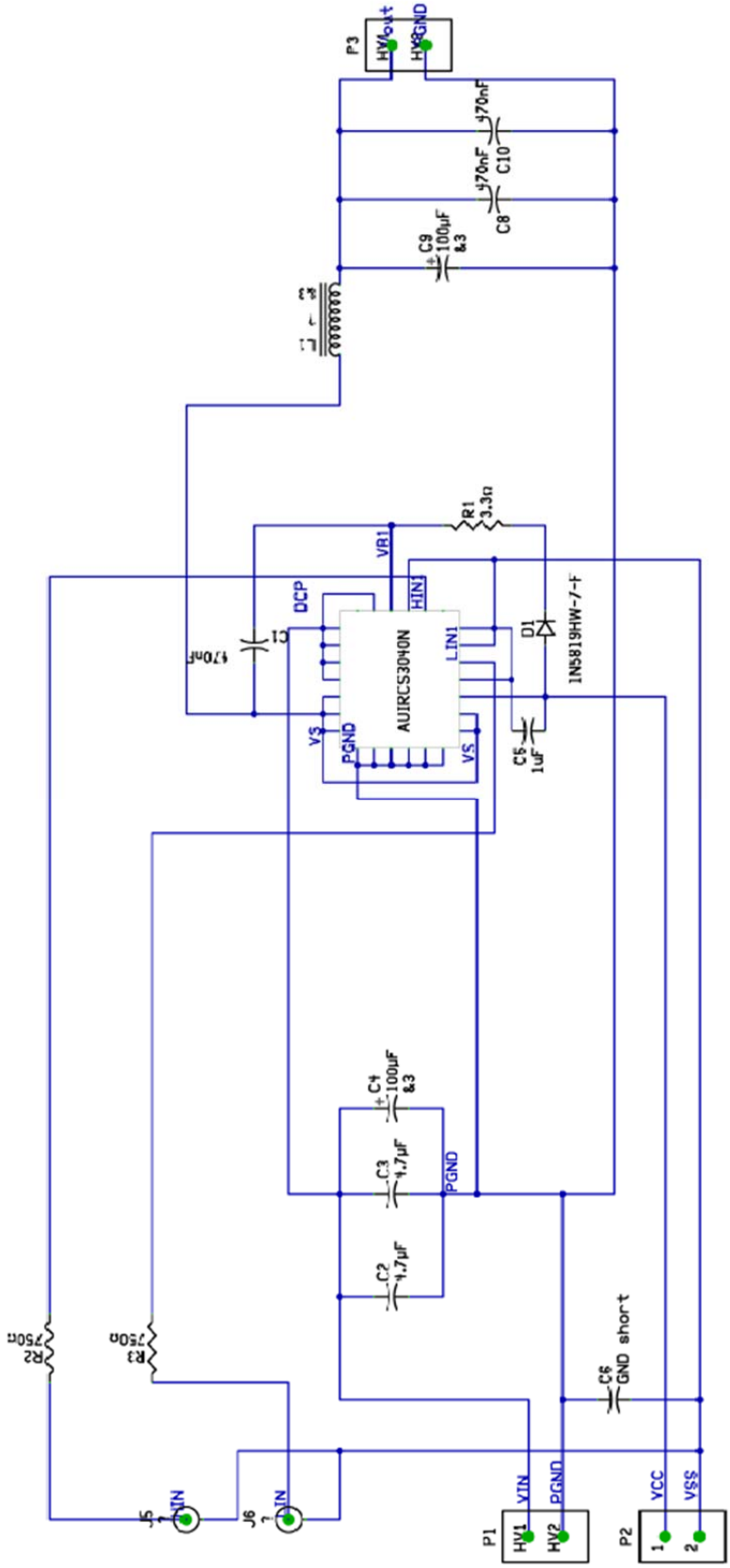
The AUIRDC3040 reference design board provides a simple, while quite optimised, example on how to implement the AUIRCS3040N AU-convert*IR*™ power stage into a practical step-down or step-up design, for automotive applications.

References

AUIRCS3040N data sheet; www.irf.com
Circad PCB, Omnigliph 6.0B, 2012
Mathcad 11.0a, is a registered trademark by PTC,

Appendix: Reference Board Schematic and BOM

IC1 : AUIRCS3040N
R1 : 3.3 to 4.7 Ohm, SM1206
R2,R3 : 330 Ohm, SM0805
C2,C3,C8,C10 : 4.7uF 50V, SM1210
C4,C9 : 470uF, 50V, low ESR
L1 : 10uH, 25A;
P1,P3 : PCB connectors, 2 poles, 10.16mm
P2 : PCB connector, 2 poles, 5.08mm
J5,J6 : Jack BNC, PCB mount, vertical


P3
HVout
HVGND
470nF
C10
470nF
C8
C9
100µF
&3
L1
R1
3.3Ω
VR1
DCP
HIN1
LIN1
AUIRCS30H0N
VS
PGND
VS
C1
470nF
D1
IN5819HW-7-F
C5
1uF
C4
100µF
&3
C3
4.7µF
C2
4.7µF
PGND
R2
750Ω
R3
750Ω
C6
GND short
J5
VIN
J6
VIN
P1
HV1
HV2
VIN
PGND
P2
1
2
VCC
VSS