International
IOR Rectifier

APPLICATION NOTE

Application Note AN-1205

Design of Secondary Side Rectification using The AUIRS1170S Smart-Rectifier Control IC

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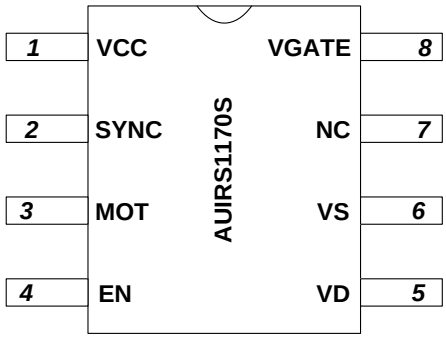
Paragraph annotation of the contents of this application note.

Introduction & Device Overview

The AUIRS1170S is an automotive qualified smart secondary side gate driver IC designed to drive N-channel power MOSFETs as synchronous rectifiers in both hard switching and soft switching / resonant converters. The IC can control one or more paralleled MOSFETs to emulate the behavior of very low Vf diodes.
The drain to source voltage of the MOSFET switch is sensed to determine the level of the current and the device is turned ON and OFF in close proximity of the zero current transition.
The pin-out for the 8 pin device is shown here below.



PIN #	Symbol	Description
1	VCC	Supply Voltage
2	SYNC	SYNC Input for direct turn off
3	MOT	Minimum On Time
4	EN	Enable
5	VD	FET Drain Sensing
6	VS	FET Source Sensing and GND connection
7	NC	Not connected
8	VGATE	Gate Driver Output

From a functional point of view, the device is an improved version with respect to previous smart rectifier ICs, like the IR1167S or the IR1169S in that:

a) output current capability has been increased to 3A source / 6A sink
b) a SYNC input has been added, which allows to anticipate the turn-off transition, or to delay the turn-on transition, complementing the Vds voltage sensing. This is especially useful in hard switching converters where shoot trough due to even shorter transition delays has to be avoided.

A typical application diagram is shown in figure 1: this is the typical output stage for hard switching converters (forward, half bridge, full bridge) or ZVT fixed frequency converters (i.e. phase shift ZVS, as an example).

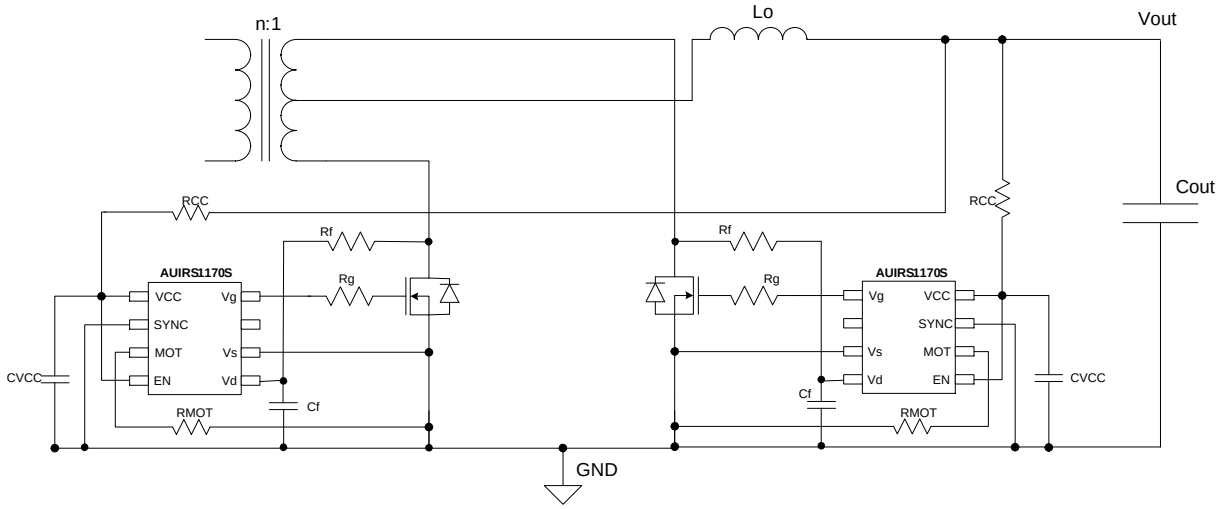


Figure 1: typical application diagram

The detailed functionality of each pin is described in the AUIRS1170S data sheet. The aim of this note is to give some hints to fully utilize the capabilities of this IC.

Operation in hard switching converters

As an example, let's consider the AUIRS1170S being used in a CCM flyback. Principle schematic and main waveforms are shown in figures 2 and 3.

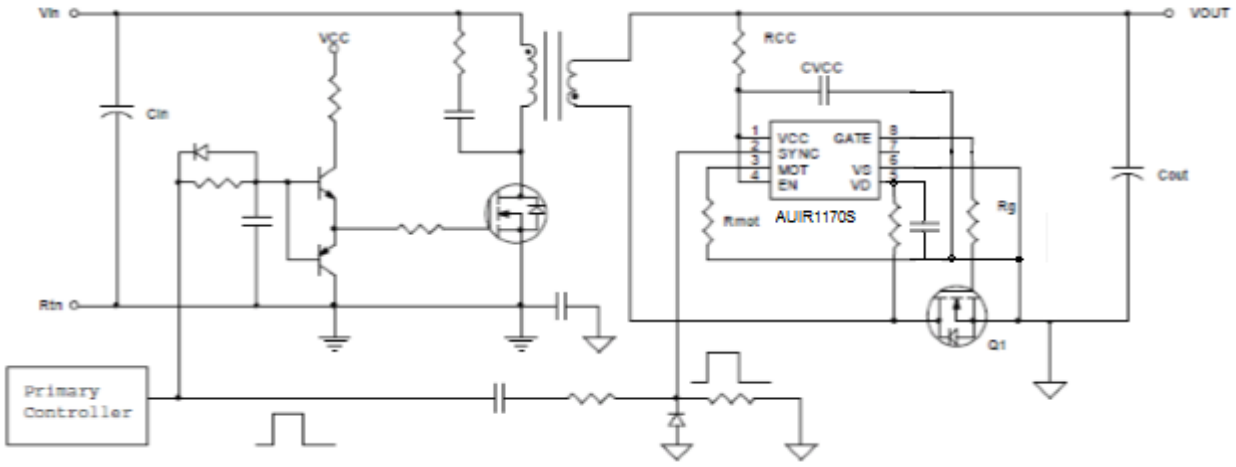


Figure 2 : Flyback converter with smart synch-rectification

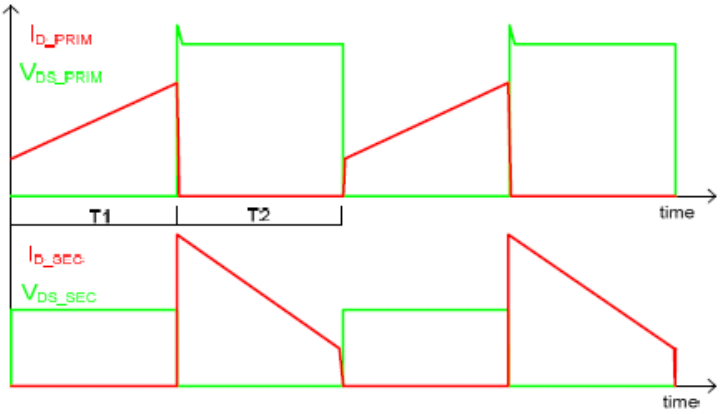


Figure 3 : main waveforms of the flyback converter operating in CCM

In the following figure 4, an expanded time scale measurement of the waveforms is shown. The red curve is the gate of the primary switch, which is turning-off, and the green waveform is the Vds voltage as seen by the AUIRS1170S. Despite the layout is quite compact, the ringing can easily cause premature turn-off of the synch. switch.
The effect is clearly shown in figure 6 and 7. Here, the test circuit used is a simple positive-tied buck converter, whose simplified schematic is shown in Figure 5.
In figure 6, the synch switch turns-on for less than MOT, simply because its current is very close to Vds turn-off threshold.
In Figure 7, the synch switch sometime turns-off after MOT, and the next pulse is skipped, because of the noise on the Vds pin.
The effect also depends on the Tj of the device and of the synch MOSFET.
If the synch MOSFET works at low Tj, its Rds-on is lower, hence its ON state Vds is lower, which decreases the level of the signals at the IC pins, thus increasing system noise sensitivity. On the other side, if the IC Tj is lower, its thresholds may decrease, which further increase noise sensitivity.

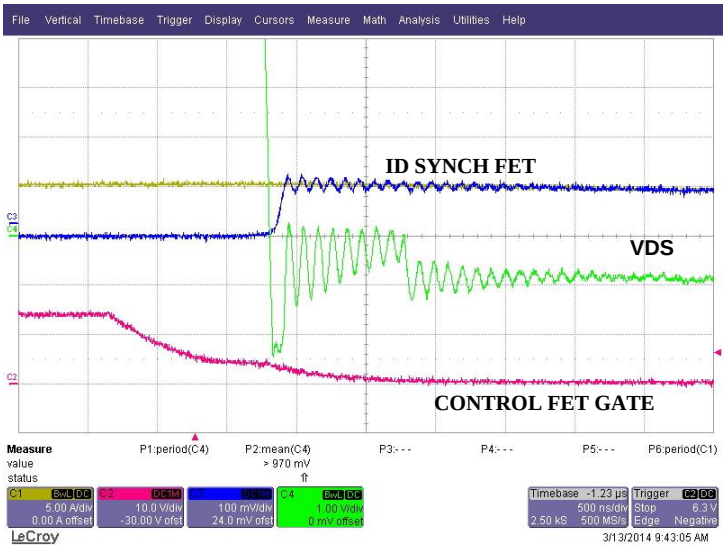


Figure 4: expanded time scale view of operating waveforms

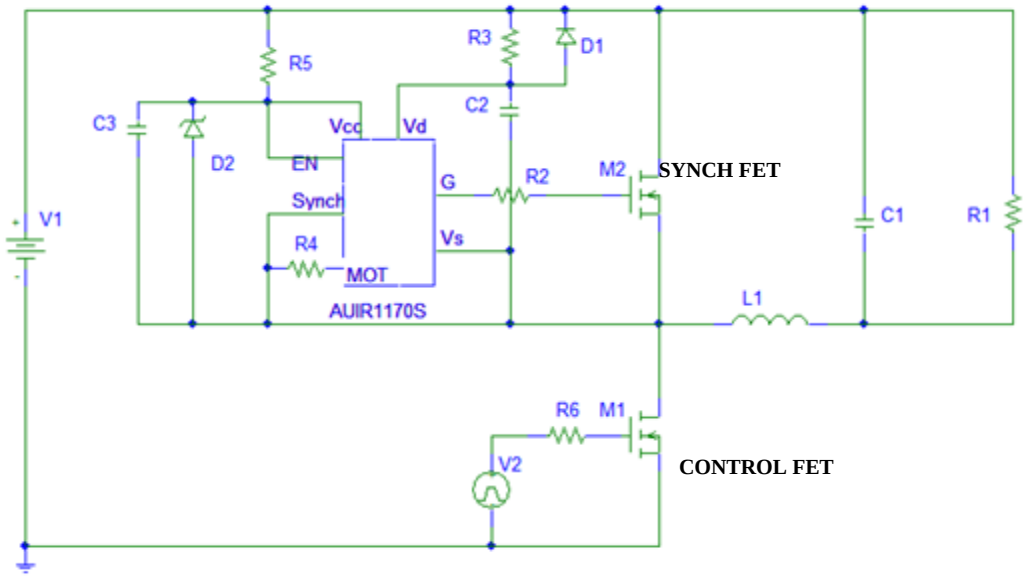


Figure 5: actual circuit used for hard swithing tests

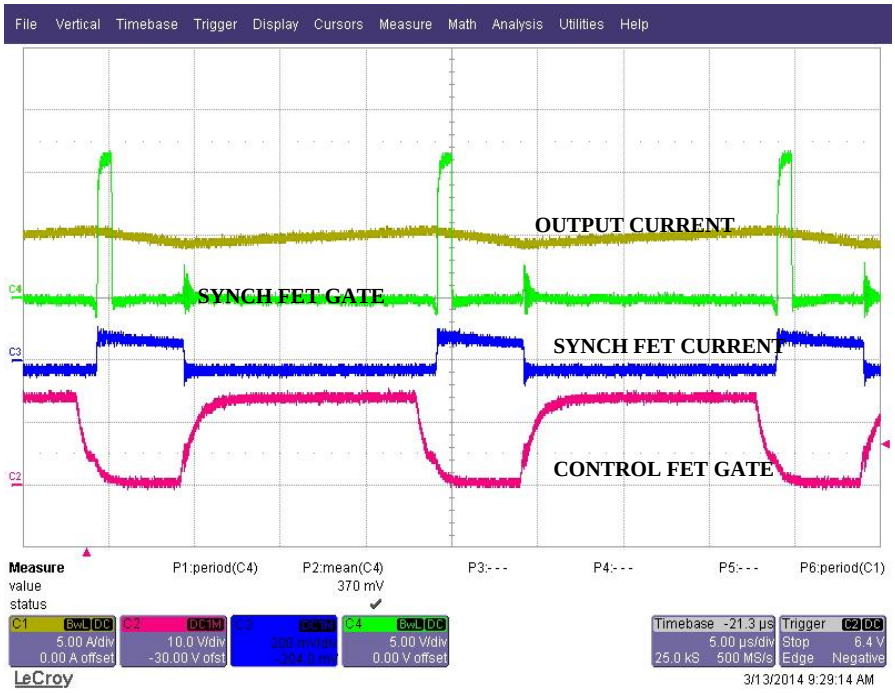


Figure 6: premature turn-off of synch switch due to low current level

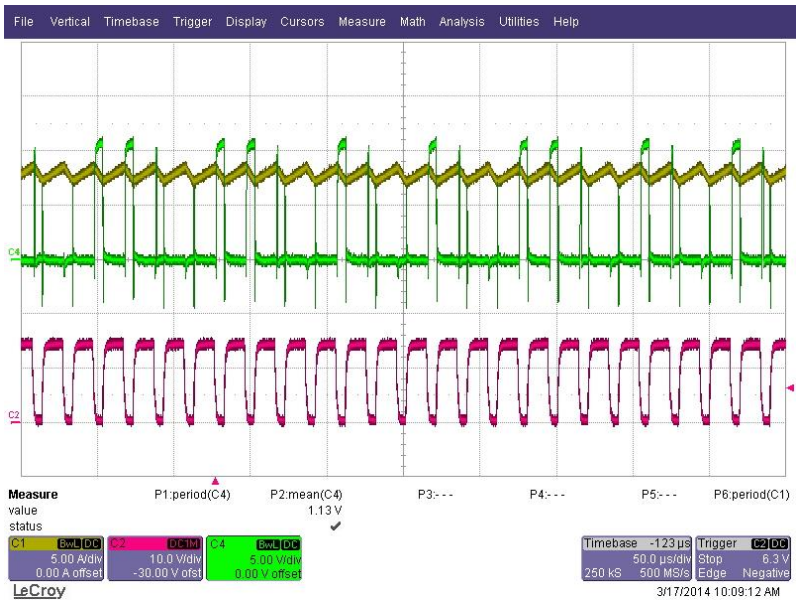


Figure 7: premature turn-off of synch switch due to noise on Vds

The nature of the phenomena can also be seen from another perspective.
Figure 8 show a simplified schematic of the smart rectifier which also includes parasitics.
Drain and source stray inductances play a major role in decreasing the Vds seen by the IC when di/dt is positive (turn-on phase) and increasing it when di/dt is negative.
Thus, Vds zero crossing may appear "anticipated", creating premature turn-off of the synch switch, and increasing power dissipation across the synch fets.

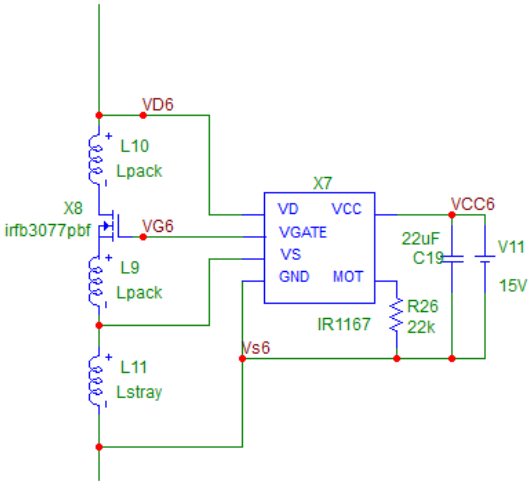


Figure 8: parasitics playing a role in the smart rectifier commutation

There may also be some stray inductance between Vs and GND pins. For that reason, Vs and GND have been connected together inside the IC in the AUIRS1170S. This helps improving quite a lot the noise sensitivity but it may be not enough.
Therefore to get a robust design for high power applications, it is strongly recommended to place a small filter on Vds, as shown in Figure 9.

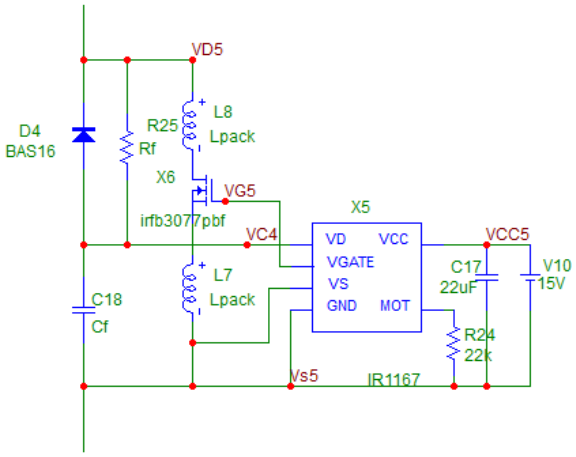


Figure 9 : Vds filtering for improved noise rejection

Fig. 10 shows the effect of filtering.
An AUIRF7737L2 directFet® driven by the AUIRS1170S emulates the diode.
The AUIRF7737L2 has a Tamb Rds-on of 1.9mOhm,max. The gate is turned off in a very clean way at less than 1A. On the other side, without filtering it was not possible to get turn-off at less than 4-5A, as shown in Fig.6.
The threshold of the AUIRS1170S is 3.5mV typ and 0mV max. Vds voltage drop at turn-off is less than 1.9mOhm * 1A = 1.9mV.
This very good results actually hides one side effect of the filter: the delay it introduces at both turn-on and turn-off. These delays will be analyzed later on, in the relevant chapter.
The actual Vds turn-off threshold of the tested IC was higher than 1.9mV; the small delay introduced by the filter, as well as other small propagation delays, make the gate being turned-off a bit later, when the current has already decreased to 1A.

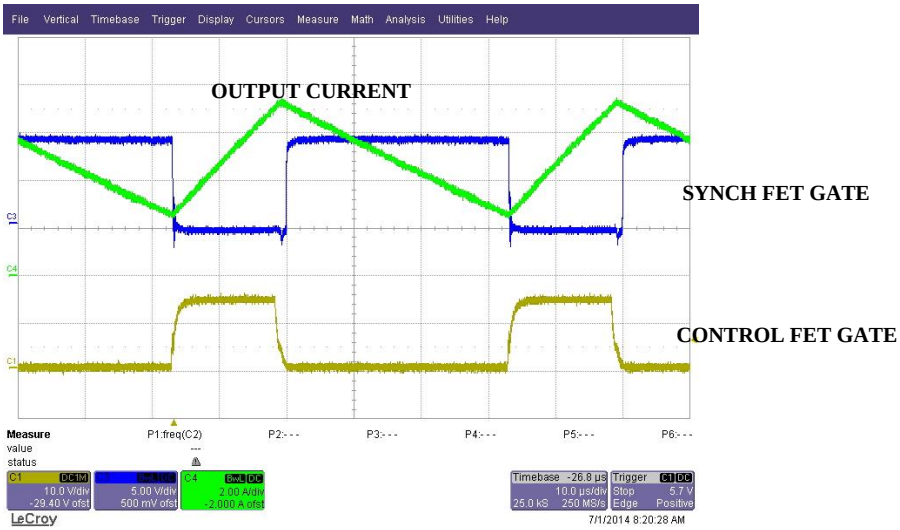


Figure 10 : the effect of correct filtering.

Operation in resonant power supplies

Operation in resonant power supplies is somewhat easier, somewhat more complicated.
Figure 11 gives an example of theoretical secondary waveforms for a LLC converter.
Now, current has a quasi-sinusoidal shape, so, for sure, di/dt effects may be reduced because di/dt may be lower (it depends, of course, on the actual switching frequency!)
On the other side, secondary switch Vds may be not so clean, because of secondary stray inductances (see an example in figure 12 where dark blue is the voltage across the secondary switch which is in OFF state, let's say S1; green is the total secondary current, flowing into the two alternate branches of the rectifier, S1 and S2; purple is the primary current and light blue the gate signal of the AUIRS1170S which drives S1).
Except when working at exactly the resonant frequency, there will always be a phase shift between the half (or full) bridge center tap voltage and the current. This is clearly visible in figure 12, where some extra Vds ringing appears in the middle of the Vds pulse, caused by the commutation of the primary switches.
This extra ringing on Vds, if not properly filtered, may induce false, or premature, commutations of the AUIRS1170S.
The nice thing is that a filter designed to get a hard switching application robust, is also usually enough for a resonant application.
The guidelines to design such filter are exposed in the next chapter.

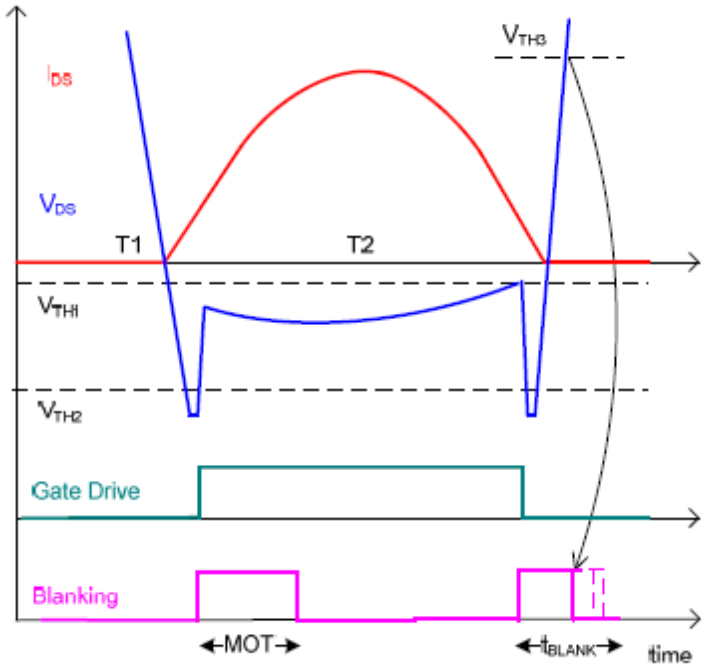


Figure 11: theoretical secondary waveforms for a resonant converter

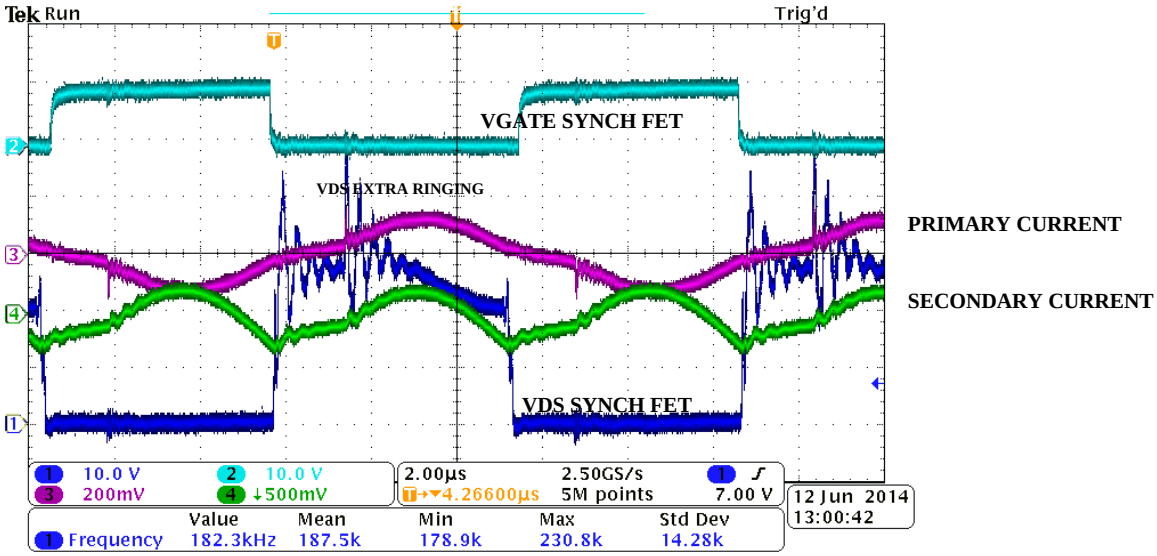


Figure 12: practical secondary waveforms in a LLC converter

Filter Design and PCB layout guidelines

Filtering Vds to achieve robust IC operation is a simple and powerful tool, but it has to be managed carefully.
When only considering the stray inductances across the synch switch, triggered by di/dt, as the main ringing source, the filter can be calculated by the following approximate formula:

$$Rf * Cf = Lstray/Rdson \quad [1]$$

This formula only holds for low di/dt (so mostly in resonant converters operating at few tens of kHz) or high Rds-on, and comes from the idea that the delay due to the time constant of the filter has to compensate for the premature turn-off due to the Lstray*di/dt effect described earlier. Example, with a 2 mOhm Rds-on synch Fet, and a 2nH stray inductance, a 1usec time constant filter would be needed.
Even considering that this time constant decreases with temperature, because Rds-on increases, the filter calculated time constant remains quite high. Example: assuming Rds-on increasing by a factor 2x at Tjmax, the filter time constant would be around 500nsec.
The formula, by itself, does not contain di/dt, and is thus valid for any kind of output current waveform. But, at very high di/dt or with very low Rds-on the reasoning is no more valid. In fact, without stray inductances the Vds zero crossing would appear after $I_{fwd}/(di/dt)$ while, with stray inductances, it would be practically instantaneous. So, the actual anticipation generated by the stray inductances cannot be longer than $I_{fwd}/(di/dt)$.
Example: with 50A and di/dt = 500A/usec, Vds zero crossing occurs after 100nsec.
So, a filter introducing a delay in this range would fully compensate Lstray effects.
A practical example is shown in figure 13 (yellow: actual Vds; purple: filtered Vds).

So, we need to find a more general rule to calculate filter cut-off frequency.

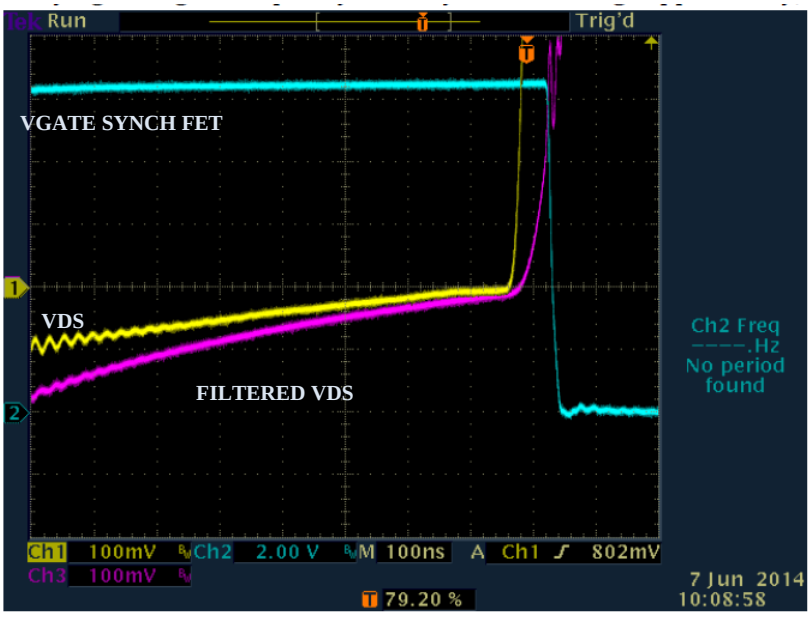


Figure 13: turn-off delay by 600kHz cutoff frequency filter.

There may be different sources of noise: referring back to Figure 4, the ringing on the Vds waveform is mostly due to a resonance between the synch fet body diode capacitance and the stray inductances in series with drain and source. But, other noise sources may be present (i.e. noise conducted or radiated by the primary side switch commutation in resonant converters).
The general rule is that filter cut-off frequency has to be set according to the fundamental frequency of the ringings (Fring): because it is a first order filter, its -3dB frequency shall be at least a decade below the ringing fundamental.
On the other side, the filter introduces delays at both turn-on and turn-off. We have already discussed about the turn-off delay so let's concentrate on the turn-on delay.
An example is shown in figure 14. A filter with a cut-off frequency of 1MHz (100pF - 1.5kOhm) introduces a turn-on delay of several hundred nsec (350nsec theoretical, a bit more actually).
Such delay can be, fortunately, easily compensated by introducing a diode in parallel to the filter resistance, which quickly discharges Cf during the high to low Vds transition.
The effect of such diode is shown in figure 15, where the turn-on delay is now only 134nsec.
Not considering for a moment the compensation by the diode, the delay cannot become a significant part of the switching half cycle. The delay introduced by the filter (0 to 90%) is 2.3 * R_f*C_f. Assuming as a starting point that the delay must stay below 20% of the half PWM period (Tsw/2), which is about half of the delay shown in Fig. 14, we have that:

$$\frac{1}{2.3*R_f*C_f} \geq \frac{10}{Tsw} = 10 * Fsw \qquad [1]$$

The delay compensation by the diode will then further reduce the real delay, to be more precise instead of "R_f" the diode equivalent resistance "Rd", which is usually much smaller than R_f, should be placed into Eq. 1.

Then the final approximated formula to determine the RC filter pole value is the following:

$$\frac{2.3 * 10}{2 * \pi} Fsw \leq \frac{1}{2 * \pi * R_f C_f} = Fp \leq \frac{Fring}{10}$$

A final verification of the best value has to be verified in the real application and a good compromise has to be found case by case.

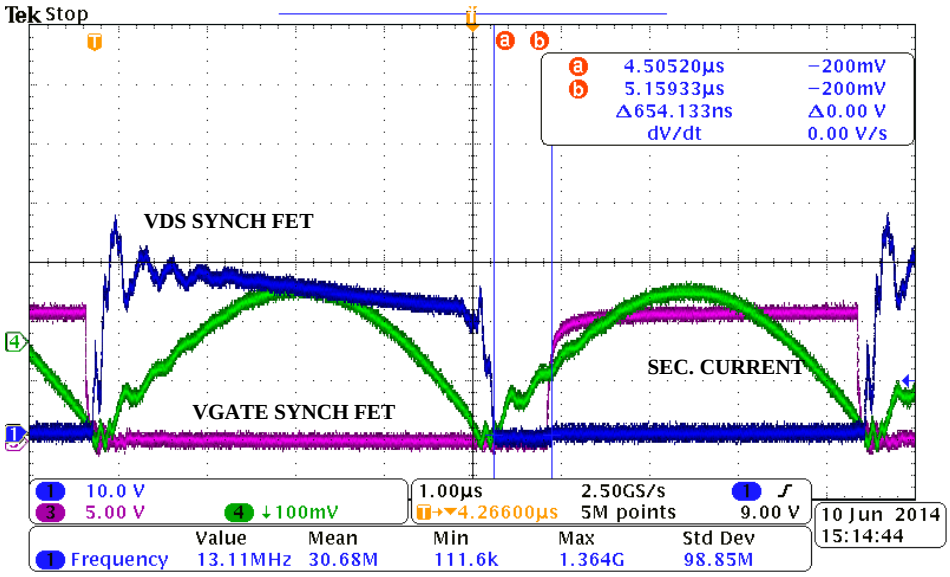


Figure 14: effect of Vds filter on turn-on delay.

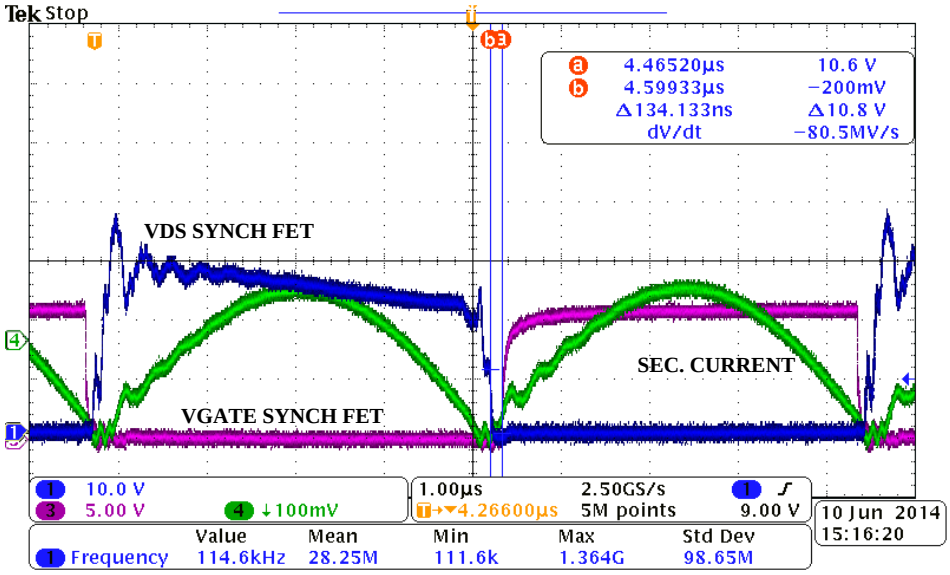


Figure 15: diode-discharge compensation of filter induced turn on delay

In all cases, the choice of R_f and C_f is not free. R_f is directly in series with pin Vd on the AUIRS1170S. Because the input Vd-Vs comparator is fed by an internal current source, adding too much external resistance may severely impact the turn-off threshold. Therefore a R_f value below 1.5k - 2k Ohm is recommended.

Both turn-on and turn-off delays are influenced by other two important parameters:

a) IC Ton and Toff propagation delays, which are in the range of 50-70nsec
b) Ton and Toff delays due to synch fet input capacitances. These delays may be much more important, especially in the case when several mosfets in parallel are driven by the IC. The AUIRS1170S has been designed to have strong driver stage (3A source and 6A sink) but delays when driving several big die size mosfets in parallel may be significant (several tens nsec to few 100nsec) especially if no particular care is taken with proper layout design, aimed to reduce gate stray inductances as much as possible.

This introduces to the layout guidelines.
An example of layout, with one AUIRS1170S driving 3 x DirectFet™, is shown in figure 16. Usual care must be taken in placing filter Vcc capacitor very close to the IC.
As well, MOT resistor placement and SYNC track layout must be very careful.
The use of DirectFet™ helps compacting the layout (the complete length of the board in figure 14 is just few cm) but a different layout could be also designed, such that each mosfet is placed at the same distance from the IC (see figure 17).
In such further example few basic ideas are highlighted, especially having gate tracks as large as possible and of equal length for the three mosfets.

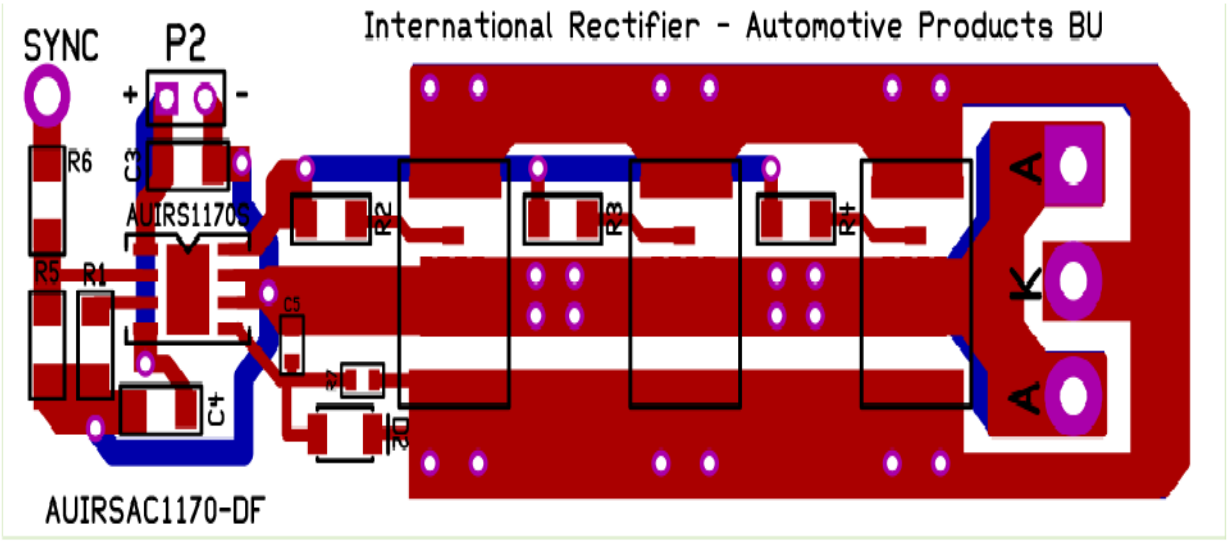


Figure 16: example of layout

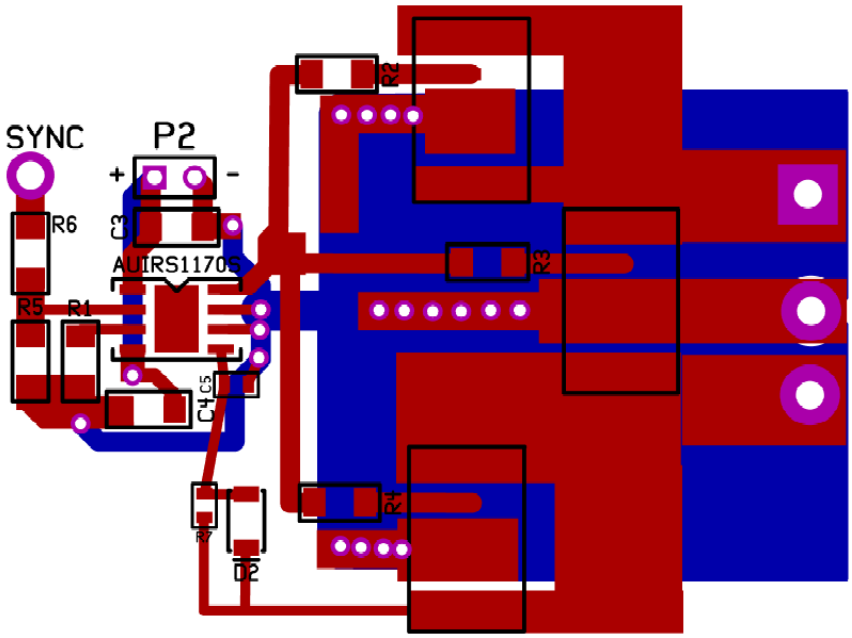


Figure 17: example of even more optimized layout

Conclusions

The AUIRS1170S is a powerful smart synchronous rectification IC; when used in applications where high current and high output power are involved, some care has to be taken in reducing noise propagation as much as possible, first of all by a proper layout, and then filtering out locally the remaining noise.
In this AN, some tips have been provided to help the designer to get the maximum performances from this IC and optimize the efficiency of the final design.

References

International Rectifier AN-1087
International Rectifier AN-1139
CIRCAD pcb design software, Version 6.0B, OmniGliph, 2012.