Sensing Current with IR25750L

IR25750L Technical description

IR25750L

About this product

The ***IR25750L Current Sensing IC*** is a simple and innovative solution for measuring the VDS(on) of a power MOSFET or the VCE(on) of an IGBT. This allows for conventional current sensing resistors or transformers to be eliminated, as well as their associated power losses and cost. The IR25750L is a parallel-connected solution so it does not generate additional power losses or parasitic inductance as with series-connected methods.

About this document

This application note provides detailed information to help speed up design time and avoid circuit problems that can occur due to incorrect usage of the IC or noise susceptibility. Helpful information is included for understanding how the IC works and how to use this IC to sense current through a power MOSFET or IGBT. PCB layout guidelines are also included to help avoid unwanted circuit noise or malfunction.

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1 IR25750L Functional Description

The IR25750L circuit is designed to perform two main functions:

1. Measure the VDS(on) or VCE(on) during the MOSFET or IGBT on-time.
2. Block and withstand high drain or collector voltage during the off-time.

The IC is connected directly to the existing pins of the power MOSFET or IGBT to be measured (***Figure 1***). The VIN pin connects to the drain (or collector), the COM pin connects to the source (or emitter), and the GATE pin connects to the gate of the MOSFET or IGBT. The VDS(on) or VCE(on) voltage level across the switch can then be measured at the CS output pin during the switch on-time. The IR25750L does not require an additional VCC pin so no other connections are necessary. The IC includes an internal 600 V NMOS (HVFET) that is connected from the VIN pin to the CS pin (***Figure 1***). The gate of HVFET is connected to the GATE pin so that the HVFET is turned on and off synchronously with the external MOSFET or IGBT. An internal resistor (R1) and capacitor (C1) form a turn-on delay (200 nsec) of the HVFET after the GATE pin turns on. This is necessary to ensure that the power MOSFET or IGBT is fully on before the internal HVFET is turned on. When the HVFET is on, the VDS(on) or VCE(on) voltage at the VIN pin is transmitted to the CS pin through a resistor divider network formed by a 1 K resistor, the RDSon of the HVFET (200 ohms), and a 50 K resistor. This voltage divider gives a VIN-to-CS ratio of approximately 0.98. An additional 5 K resistor and 10 pF capacitor is also included at the CS output pin for high frequency noise filtering.

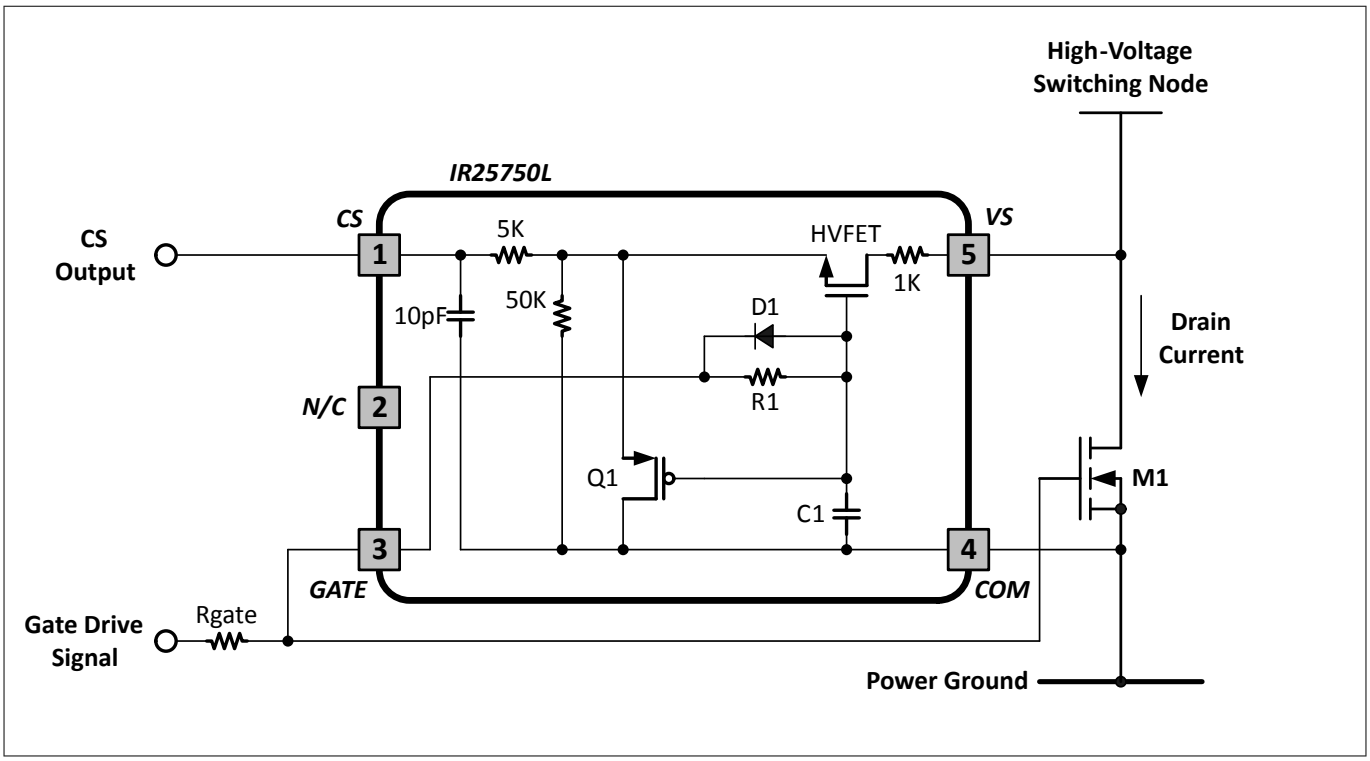

Figure 1 IC pin out and internal block diagram

When the gate drive signal goes high, the external MOSFET or IGBT turns on. The drain or collector voltage decreases quickly from a high voltage down to the VDS(on) or VCE(on) voltage level (***Figure 2***). The drain or collector current increases to a level depending on the type of load circuit connected to the switching node. If the switching node is connected to an inductor, for example, then the current will ramp up linearly and at a rate determined by the inductor value and the amount of voltage pushing on the inductor. After a small delay (200 nsec), the internal HVFET turns on and the VDS(on) or VCE(on) of the external MOSFET or IGBT is translated to the CS pin.

When the external MOSFET or IGBT is turned off, the GATE pin goes low and the internal diode (D1) pulls the gate of the HVFET down quickly and turns the HVFET off. This is necessary to ensure that the HVFET turns off quickly before the external drain or collector voltage of the power switch increases again at the beginning of the

off-time. During the off-time, the internal PMOS (Q1) turns on and holds the CS pin down to COM. Also important to note, the HVFET has a parasitic output capacitance that can cause a momentary spike at the CS pin at the turn-off edge of the external power switch (see ***Figure 4***). The amplitude and duration of this spike depends on the dv/dt slew rate of the drain or collector of the MOSFET or IGBT as it rises again after turn off.

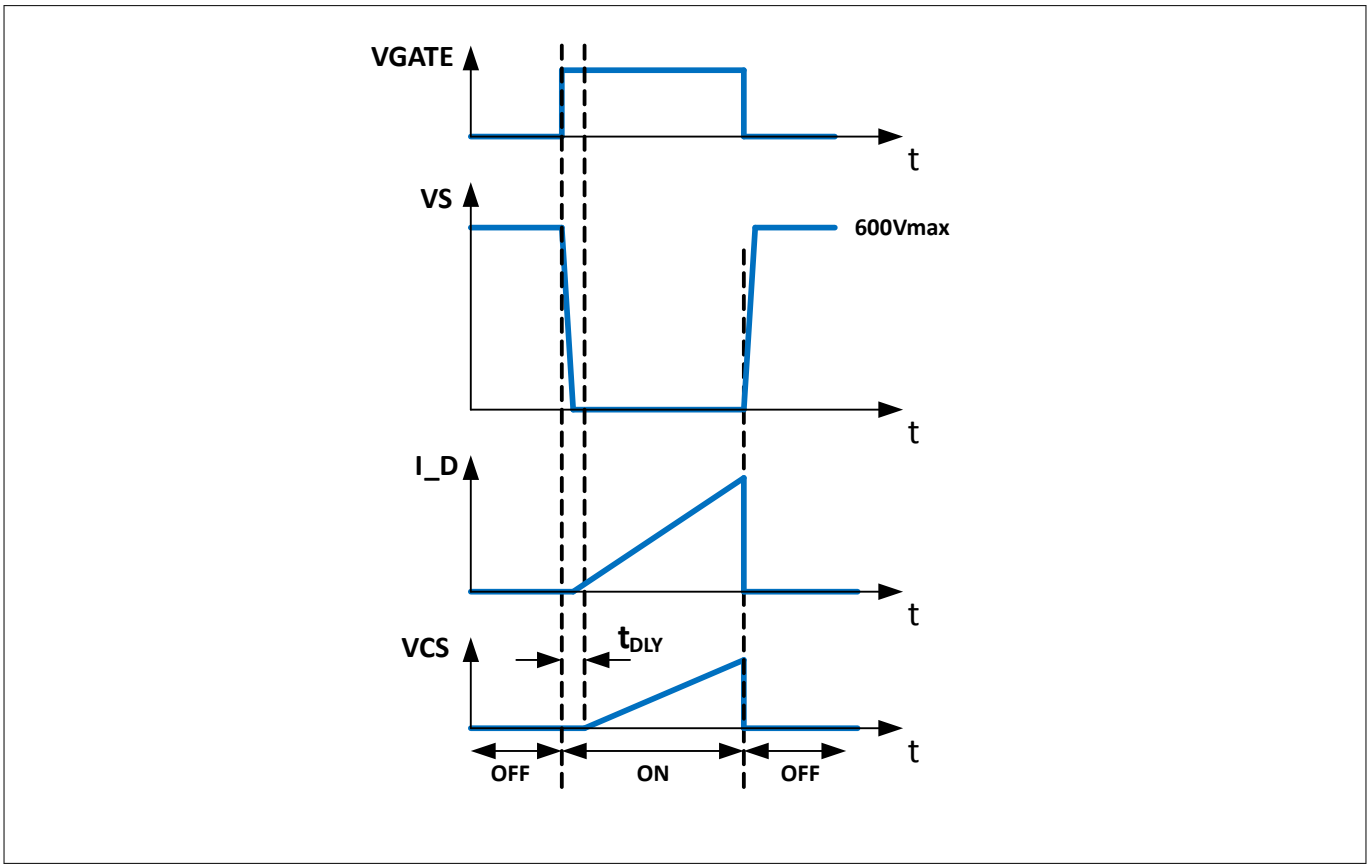

Figure 2 IR25750L timing diagram

2 MOSFET VDS(on) Sensing

A test circuit has been implemented for sensing current in a power MOSFET during switched-mode operation. The circuit includes (***Figure 3***) the power MOSFET (M1), the IR25750L (IC1), a high-current power inductor (L1), a high-current fast diode (D1), a d.c. input voltage (VIN), an output capacitor (C2) and parallel load resistor (RL), and a one-shot on/off gate pulse generator (PGEN). When M1 is turned on at the gate from the PGEN, current flows from the input voltage (VIN+), through L1, through M1, and to ground (VIN-). The inductor current ramps up linearly to a peak level and M1 is then turned off. During the off-time, the current flows through L1, through diode D1, through the output capacitor (C2) and load resistor (RL), and to ground. The IR25750L is connected in parallel to M1 with the drain connected to the VS pin and the source connected to the COM pin. A one-shot pulse generator (PGEN) is then connected through a 47 ohm gate resistor to the GATE pin of the IC and to the gate of the MOSFET. The on-time of the MOSFET can be set using the PGEN and the VDS(on) is then measured between the CS pin (VCS+) and COM (VCS-). Important to note is that the COM pin should be connected with a separate trace to the source of the MOSFET, and, the COM pin trace should also be used as the measurement ground (VCS-) for the VCS measurement. Do not connect the VCS measurement ground to the power ground, otherwise unwanted inductive high-frequency noise can occur on the VCS measurement and can cause voltage spikes, signal distortion, or false triggering of the peak current detection circuitry. Also, the gate resistor must always be placed *before* the IR25750L and the MOSFET gate to ensure that the IR25750L turns on a short delay time (200 nsec) after the MOSFET turns on.

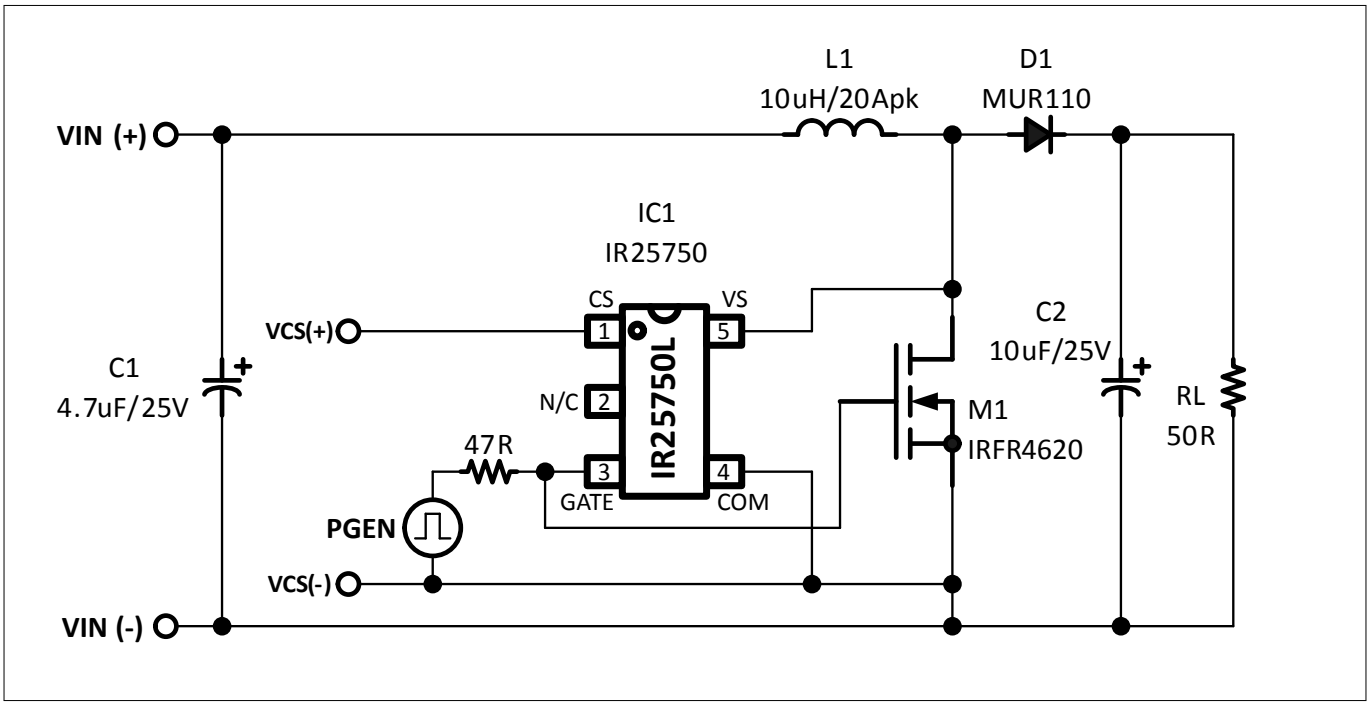

Figure 3 VDS(on) sensing test circuit

The circuit switching waveforms (***Figure 4***) include the GATE pin voltage (V_GATE), the inductor current (I_L1), the MOSFET drain voltage (V_VS), and the CS pin output voltage (V_CS). During the on-time, the inductor current (and MOSFET drain current) ramps up linearly due to the voltage across the inductor. At the end of the on-time, the current reaches a peak level of about 10 Apk. The V_CS output measurement reaches a peak voltage of about 0.7 V. This is close to the expected V_CS voltage level of 0.64 V which is given as:

$$V_{CS} = I_{DRAIN} \cdot RDS(on)$$

The V_CS measurement is slightly higher than the calculated value (0.7 V vs. 0.64 V). This is normal and due to standard RDS(on) tolerances of the MOSFET (MOSFET type = IRFR4620, RDSon = 64 mOhm +/- 25%). Also,

2 MOSFET VDS(on) Sensing

depending on the type of heatsinking used, the RDS(on) can increase slightly due to self-heating as the instantaneous power loss is generated in the MOSFET during the on-time.

When the MOSFET is turned off, a momentary voltage spike typically occurs at the CS pin. This is due to the fast rising of the MOSFET drain voltage that occurs just after the MOSFET turns off. The internal HVFET of the IR25750L has an output capacitance which generates a current from the VS pin to the CS pin depending on the dv/dt rate at the MOSFET drain. This voltage spike, however, occurs during the off-time and can easily be ignored by the detection circuit with proper blanking. If the detection circuit, for example, is synchronized such that it only measures the peak current during the on-time, then the spike occurring during the off-time will be completely ignored.

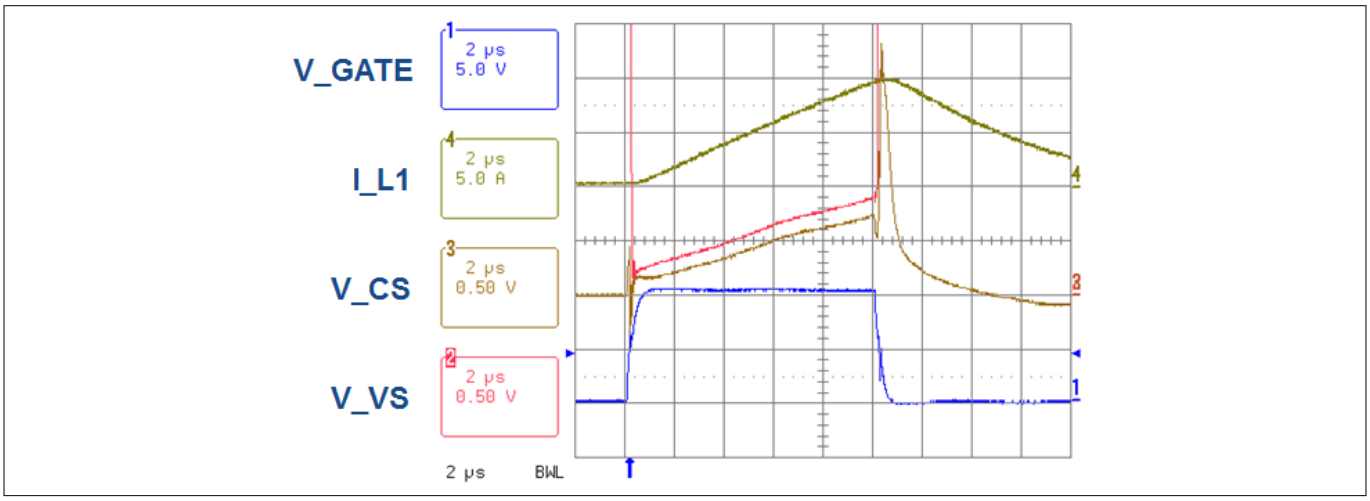

Figure 4 **VDS(on) sensing waveforms (V_GATE=lower blue, V_CS=middle brown, V_VS=middle red, I_L1=upper olive). MOSFET=IRFR4620 (RDSon=64mOhm)**

3 IGBT VCE(on) Sensing

The same test circuit used for VDS(on) sensing was also used to measure the VCE(on) of an IGBT (***Figure 5***). The on-time of the IGBT is set using the PGEN circuit and the resulting VCE(on) voltage at the collector is measured at the CS pin (VCS+). During the on-time, the inductor current ramps up to a peak level and M1 is then turned off. During the off-time, the current flows through L1, through diode D1, through the output capacitor (C2) and load resistor (RL), and to ground. The IR25750L is connected in parallel to M1 with the collector connected to the VS pin and the emitter is connected to the COM pin.

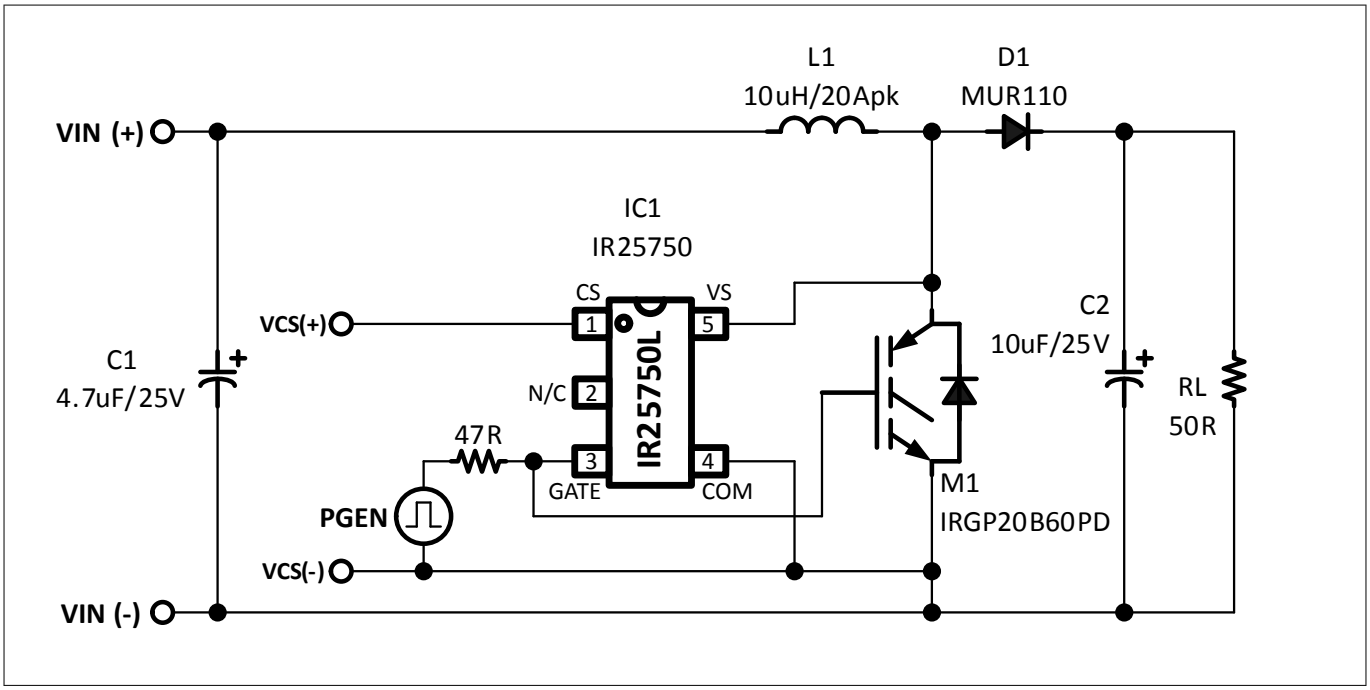

Figure 5 VCE(on) sensing test circuit

From the waveforms (***Figure 6***), it can be seen that the inductor current (top green trace) ramps up to a peak current during the on-time. The VS signal at the collector (middle red trace) has a non-linear shape due to the inherent VCE versus ICE characteristic of the IGBT (***Figure 7***). The CS output signal (VCS+) then follows the VS signal shape after a short internal delay of the IR25750L (200 nsec) at the rising edge of the gate signal (lower blue trace). The collector current ramps up to about 10 Apk and the CS output signal reaches about 2 Vpk. This is the expected voltage at the CS pin as given by the characteristic graph of the IGBT for a peak current level of 10 A and a gate voltage of 15 V (***Figure 7***).

Similar to the VDS(on) measurement of a MOSFET, a momentary spike also occurs at the CS pin at turn off when sensing an IGBT. The dv/dt rate of the collector node (VS pin), together with the output capacitance of the internal HVFET, causes a momentary current to flow from the VS pin to the CS pin. This spike occurs during the off-time so proper blanking of the CS output signal (that is, measuring the CS pin only during the on-time) will ensure that this spike is completely ignored by the peak over-current detection circuit.

3 IGBT VCE(on) Sensing

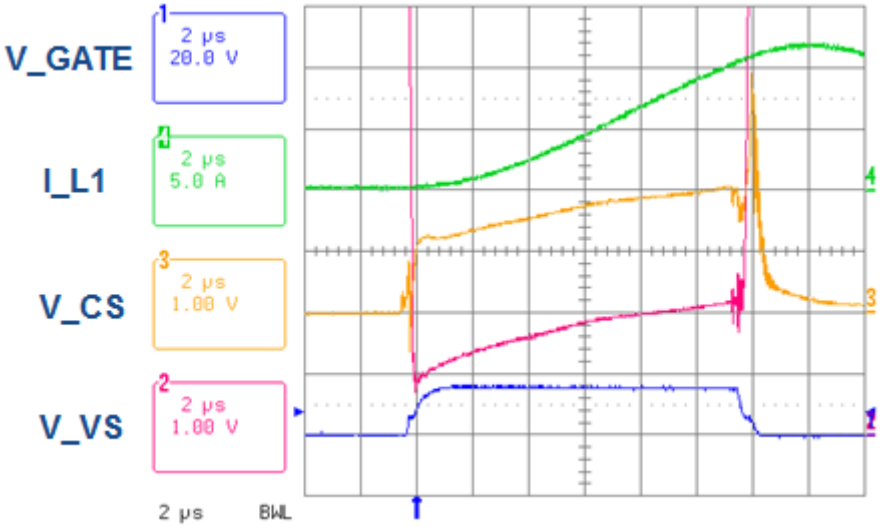

Figure 6 **VCE(on) sensing waveforms**

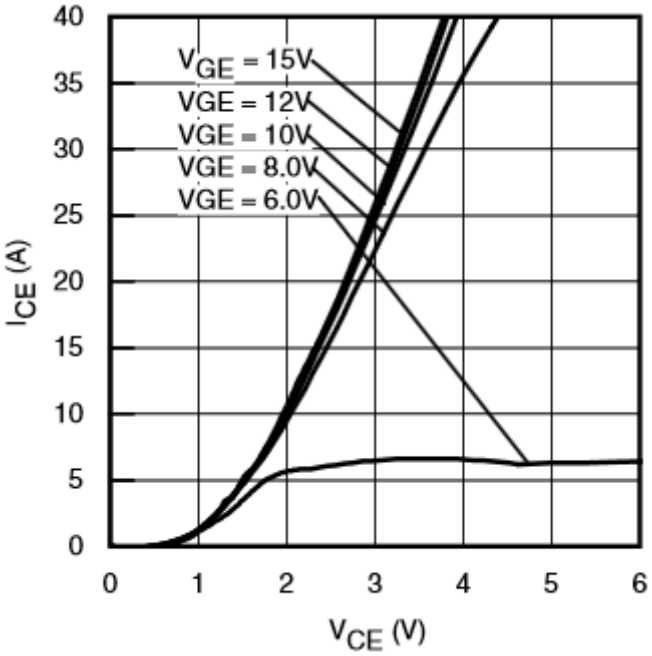

Figure 7 **IGBT VCE(on) vs. ICE datasheet graph (IGBT type = IRGP20B60PD, Tj =25 degC)**

4 Adjustment and Temperature Compensation

It is well known that the VDS(on) of a MOSFET or the VCE(on) of an IGBT can have a temperature coefficient that can give an additional measurement variation over temperature. In order to compensate for ambient temperature variations, and additional resistor and NTC network circuit can be connected at the CS pin (***Figure 8***). The temperature compensation circuit includes a resistor (R1) connected from the GATE pin to the CS pin, two series resistors (R3, R4) connected from the CS pin to COM, and an NTC resistor (R2) connected across resistor R3. This resistor divider circuit allows for the CS pin voltage to be adjusted up or down with an offset, and, the NTC resistor allows for the VDS(on) or VCE(on) temperature variation to be compensated.

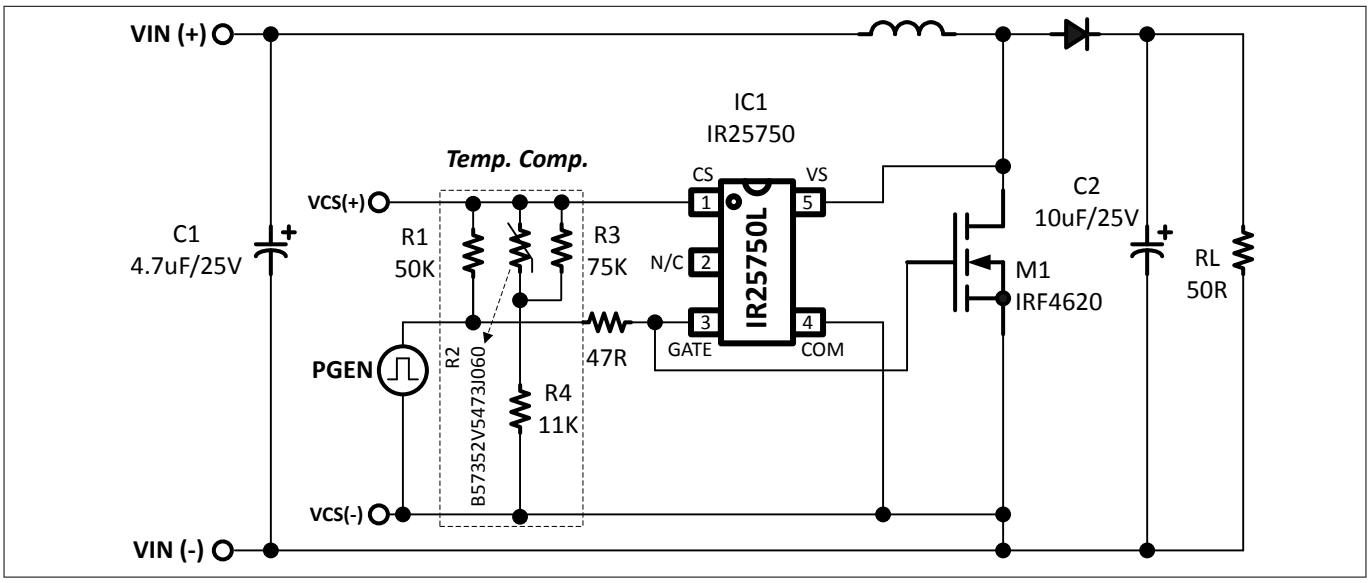

Figure 8 Additional circuit at CS pin for adjusting the CS voltage offset and compensating for VDS(on) temperature variations

Figure 9 and ***Figure 10*** show the comparison graphs for with and without the additional temperature compensation circuit. The curves are the VS pin and CS pin peak voltage levels measured at the end of the on-time. Without the temperature compensation circuit, the CS pin voltage directly follows the VS pin voltage as the VDS(on) of the MOSFET (M1) varies with decreasing or increasing ambient temperature. With the additional compensation circuit, the CS pin voltage is now almost flat over the complete temperature range with a slight positive slope. The ambient temperature variations of the VDS(on) of M1 have been compensated at the CS pin with the resistor divider and NTC. Please note that this compensation circuit only compensates for ambient temperature changes. The self-heating of the MOSFET itself can give an additional variation depending on the type of heatsinking used to thermally manage M1.

4 Adjustment and Temperature Compensation

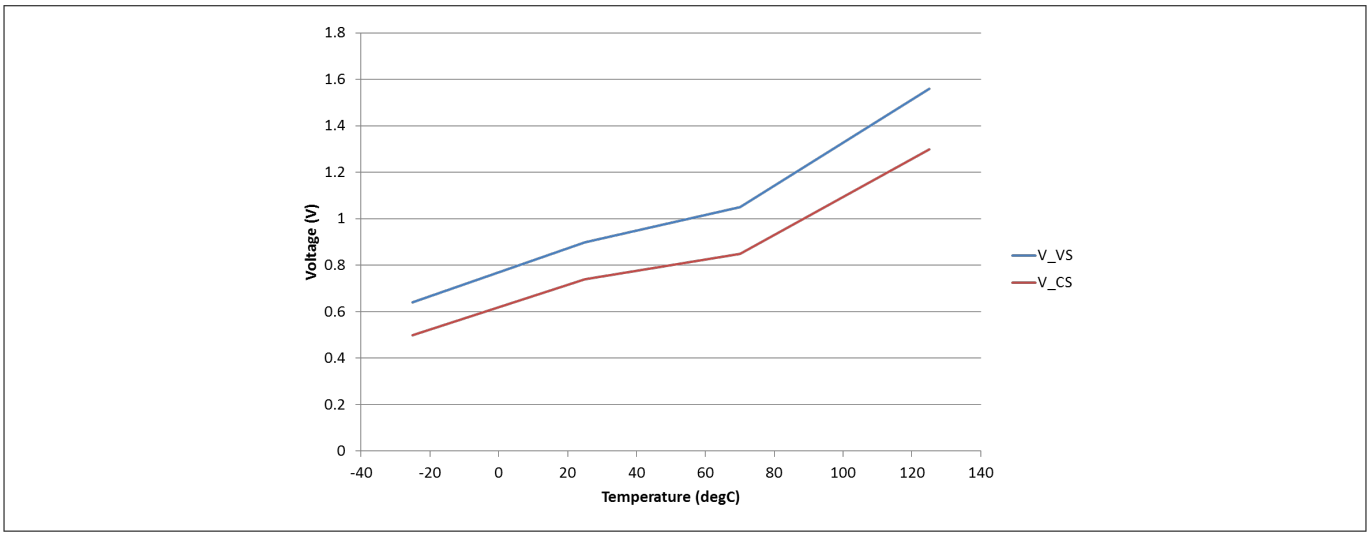

Figure 9 **VS pin voltage (blue trace) and CS pin (red trace) peak voltage levels for VDSon sensing versus temperature without temperature compensation circuit**

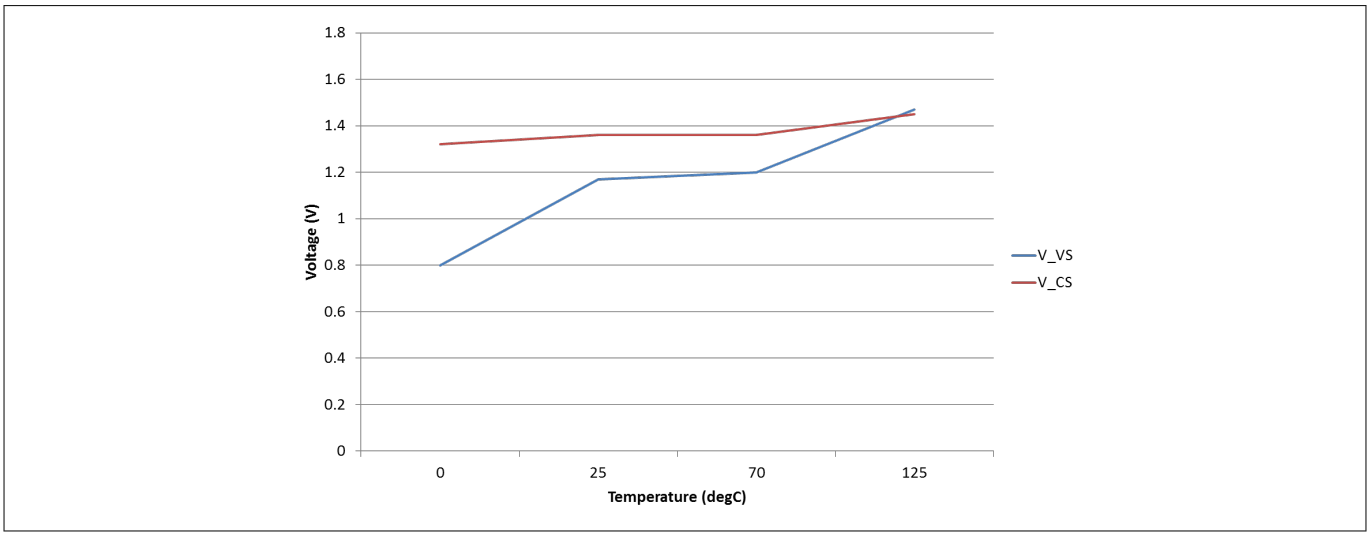

Figure 10 **VS pin voltage (blue trace) and CS pin (red trace) peak voltage levels for VDSon sensing versus temperature with additional temperature compensation circuit**

For the IGBT temperature compensation, the same external compensation circuit was used but the values were changed slightly to better match the IGBT temperature characteristics (***Figure 11***).

4 Adjustment and Temperature Compensation

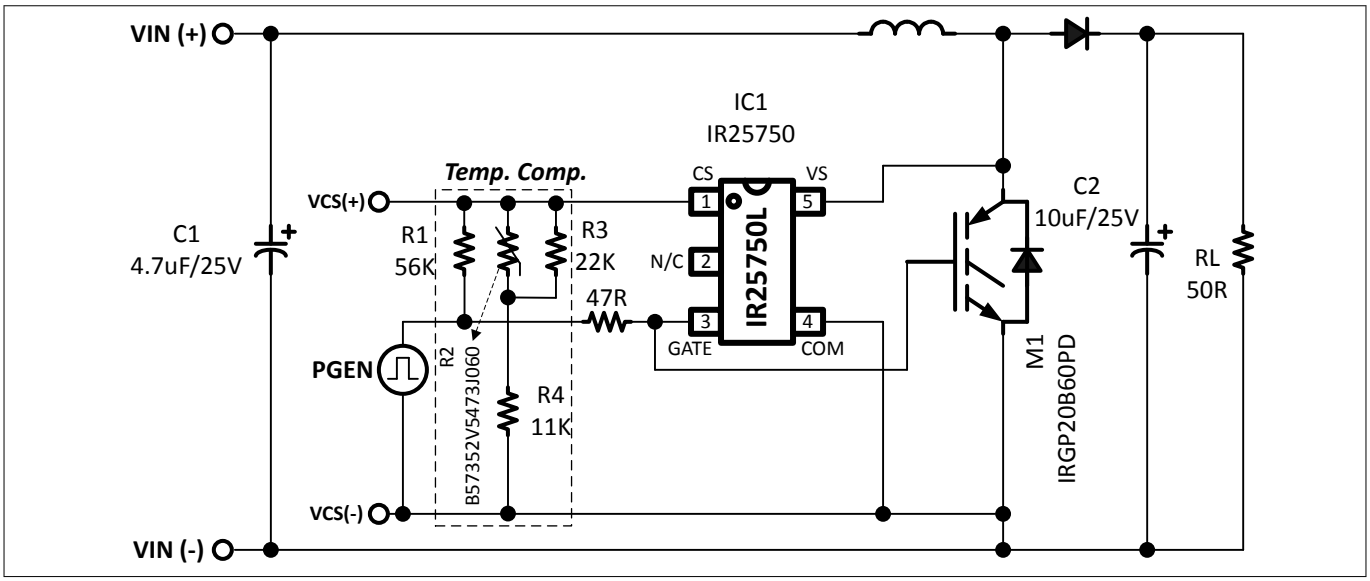

Figure 11 **Additional circuit at CS pin for adjusting the CS voltage offset and compensating VCE(on) temperature variations**

Figure 12 and *Figure 13* show the comparison graphs for an IGBT for with and without the additional temperature compensation circuit. The curves are the peak CS pin and VS pin voltage levels measured at the end of the on-time. As expected, without the temperature compensation circuit, the CS pin voltage directly follows the VS pin voltage as the VCE(on) of the IGBT (M1) varies with decreasing or increasing ambient temperature. With the additional compensation circuit, the CS pin voltage is now almost flat over the complete temperature range, with a slightly negative slope. The ambient temperature variations of the VCE(on) of M1 have been compensated at the CS pin with the resistor divider and NTC. Please note that this compensation circuit only compensates for ambient temperature changes. The self-heating of the IGBT itself can give an additional variation depending on the type of heatsinking used to thermally manage M1.

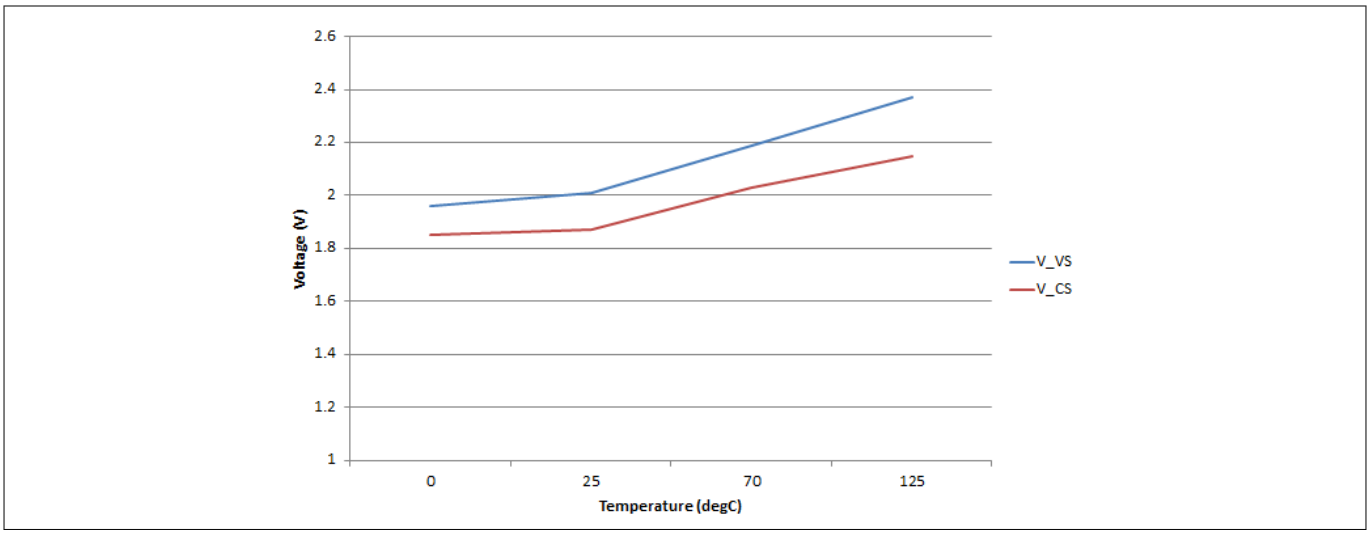

Figure 12 **VS pin voltage (blue trace) and CS pin (red trace) peak voltage levels for VCEon sensing versus temperature without temperature compensation circuit**

4 Adjustment and Temperature Compensation

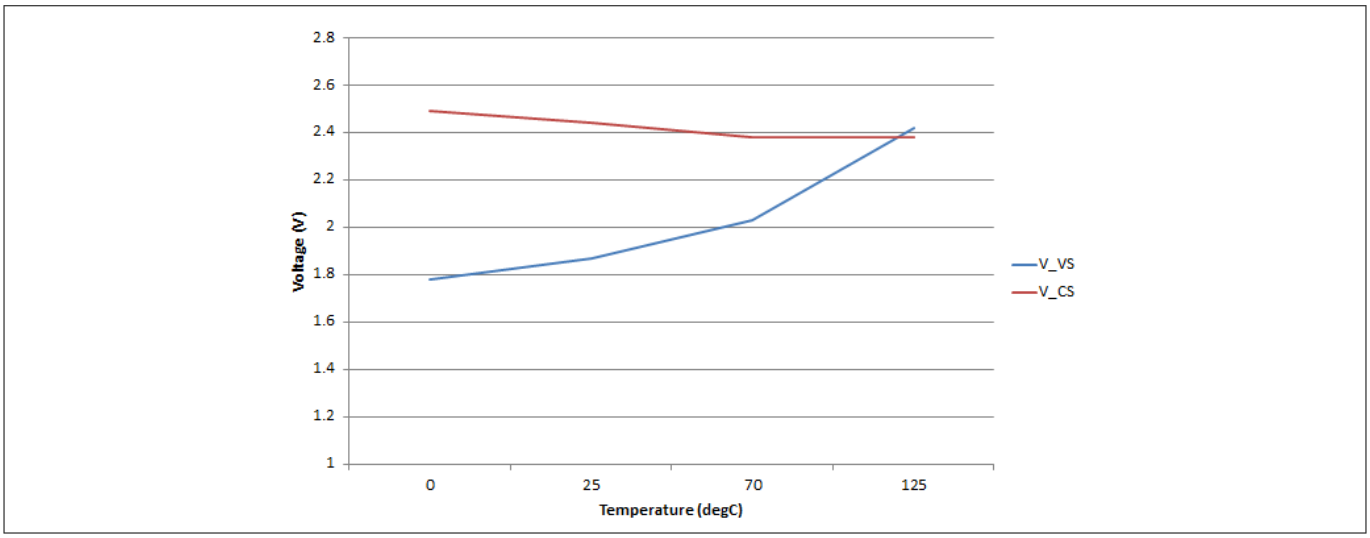

Figure 13 **VS pin voltage (blue trace) and CS pin (red trace) peak voltage levels for VCEon sensing versus temperature with additional temperature compensation circuit**

5 PCB Layout Guidelines

For correct circuit functionality and to avoid high-frequency noise problems, proper care should be taken when designing the pcb layout. Design problems due to poor layout can typically include high-frequency noise, EMC issues, latch-up, abnormal circuit behavior, component failures, low manufacturing yields, and poor reliability. The following layout tips and figures should be followed as early as possible in the design cycle in order to minimize circuit problems, shorten design time, and to increase reliability and manufacturability:

Tip: *Keep VIN-to-drain (or VIN-to-collector) trace as short as possible. This will help reduce parasitic inductance and switching noise.*

Tip: *Do not route the power ground trace through the COM pin of the IR25750L. Connect the IR25750L COM pin with a separate trace and at a single point only to the source of the MOSFET (or emitter of the IGBT). This will prevent high-frequency noise from occurring on IC pins that can cause circuit malfunction or failures.*

Tip: *Keep the distance from the MOSFET or IGBT to the IR25750L as short as possible. This will help reduce the parasitic inductance in the traces and minimize measurement errors due to switching noise.*

Tip: *Keep the distance from the CS pin to the comparator circuit, micro-controller, PWM control IC, etc., as short as possible. This will also help minimize measurement errors or false triggering caused by switching noise.*

Tip: *Place the gate drive resistor before the IR25750L GATE pin and the gate connection of the MOSFET or IGBT. This will ensure that the IR25750L turns on after a short delay (200 nsec) from the MOSFET or IGBT.*

Tip: *VCS measurement ground should be a separate trace connected to the source of the MOSFET or IGBT to minimize switching noise and measurement errors. Do not connect VCS measurement ground to power ground!*

Tip: *Connect VCS measurement ground back to PWM controller ground. Do not connect PWM controller ground to anywhere else except VCS measurement ground!*

See ***Figure 14*** for D2PAK or DPAK pcb layout guidelines.

See ***Figure 15*** for DirectFET pcb layout guidelines.

See ***Figure 16*** for TO-220 or TO-247 pcb layout guidelines.

5 PCB Layout Guidelines

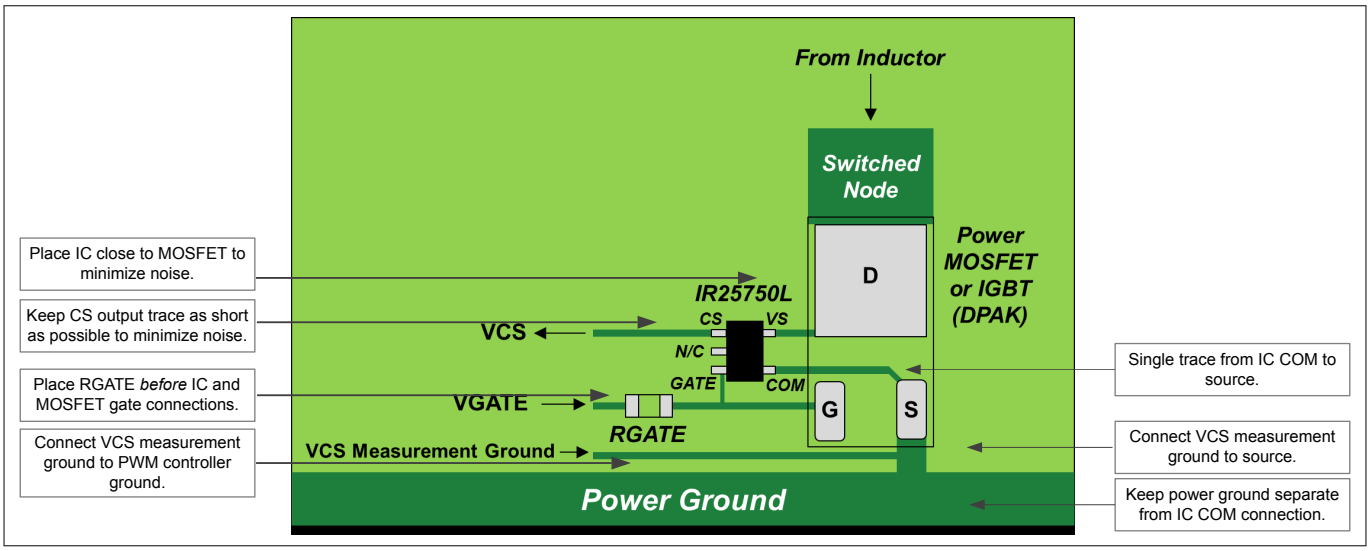

Figure 14 PCB layout for DPAK/D2PAK MOSFET or IGBT (Bottom View)

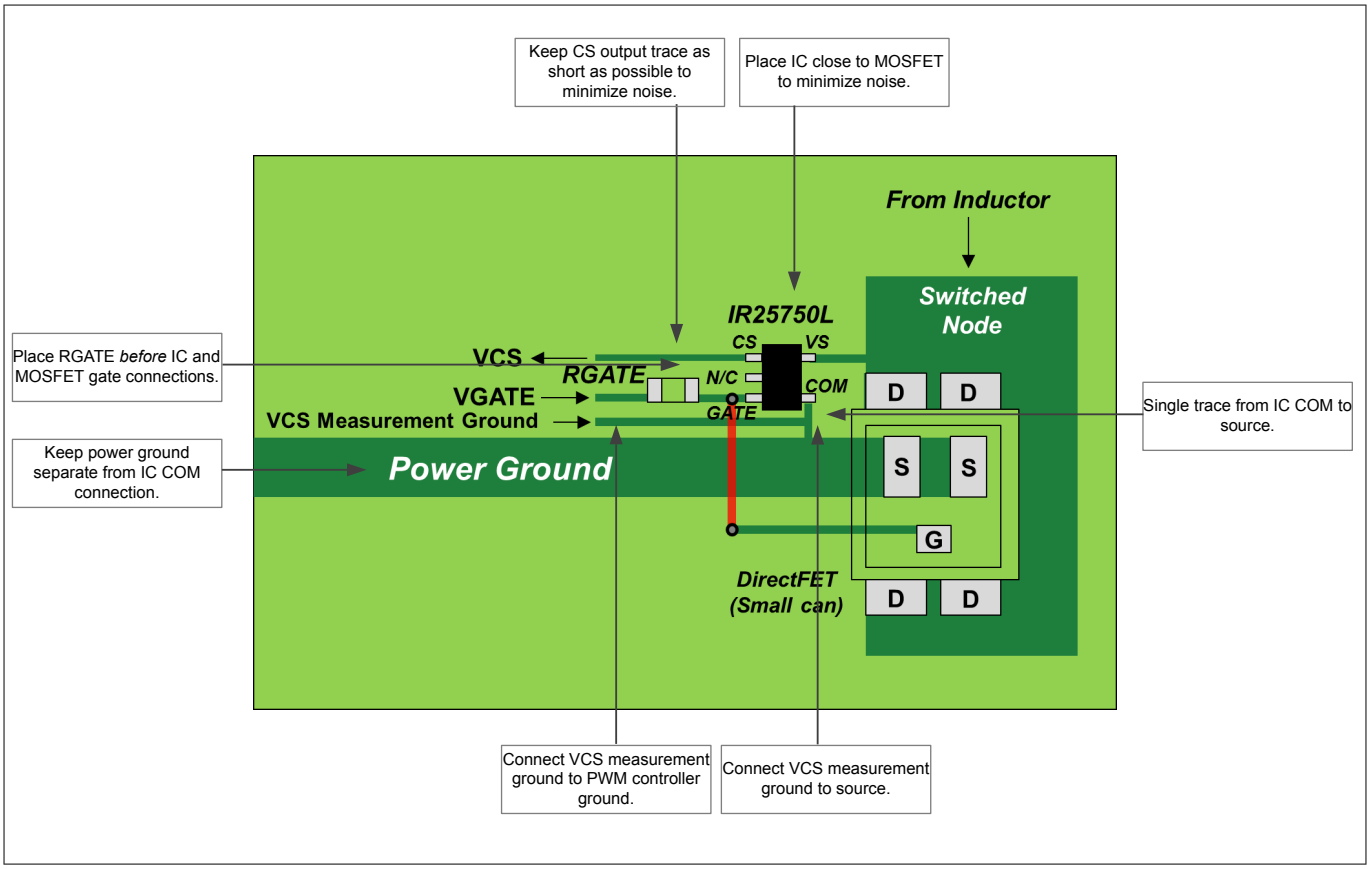

Figure 15 PCB layout for DirectFET MOSFET or IGBT (Bottom View)

5 PCB Layout Guidelines

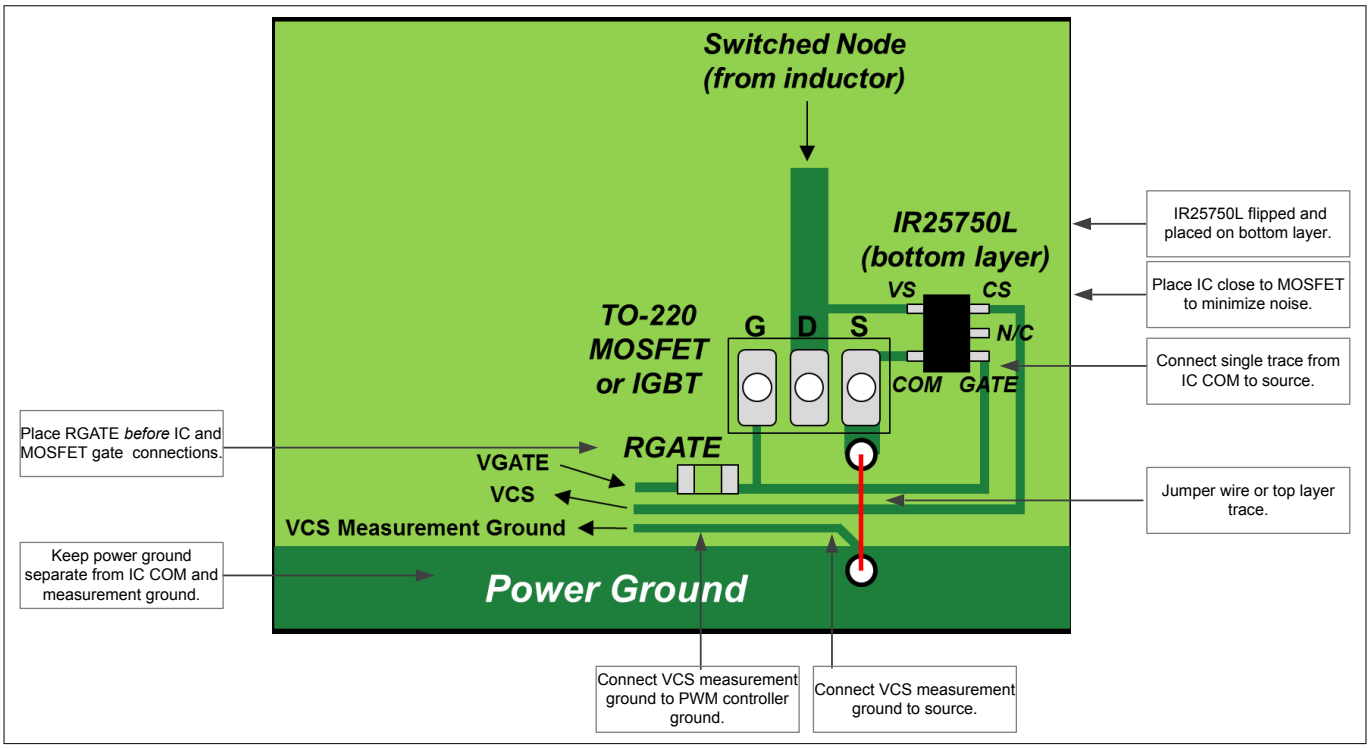

Figure 16 **PCB layout for through-hole TO-220/TO-247 MOSFET or IGBT (Top View). (Please note: IR25750L is flipped and placed on bottom side)**

6 IRuCS1 Adapter Board

A small adapter board ***(IRuCS1)*** is available for testing the IR25750L inside an actual switched-mode application. The board includes (***Figure 17***) the switching power MOSFET or IGBT (M1) footprint for D2PAK or DPAK, the IR25750L SOT-23 Current Sensing IC (IC1), the gate resistor (RG), and optional temperature compensation circuitry (R1, R2, R3, R4). The IR25750L is placed directly next to M1 and connected to the existing gate, drain and source signals of M1. The current sensing circuit does not have a VCC pin so no additional VCC trace or supply voltage is required. The IRuCS1 board includes test points for ease of measurement with an oscilloscope probe and can be easily connected into an existing switched-mode power circuit for fast in-circuit evaluation using the gate drive input, the drain or collector connection pads, and the source or emitter connection pads.

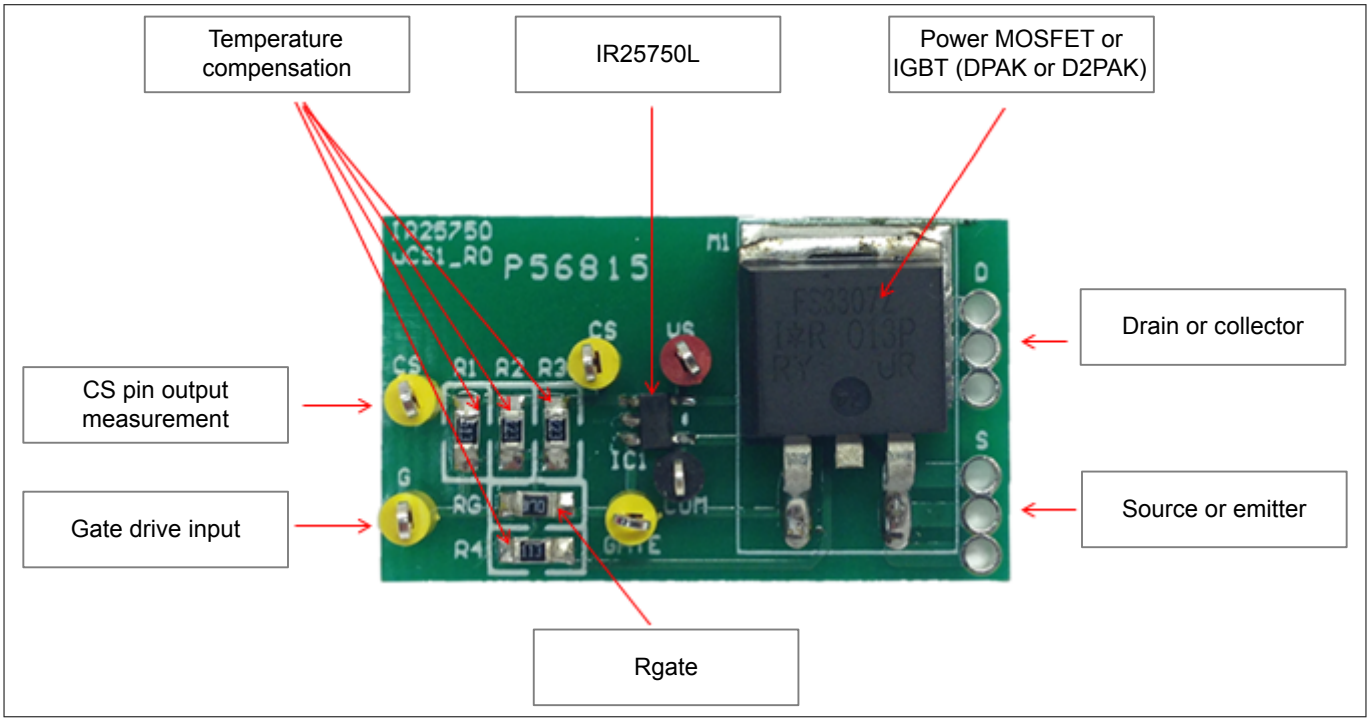

Figure 17 IRuCS1 adapter test board

7 Revision history

Table 1

Document version	Date of release	Description of changes
1.0	2019-04-12	Migration from original and update schematics

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