International
IOR Rectifier

APPLICATION NOTE

# Application Note AN-1167

## Power Factor Correction using IR1153 Fixed Frequency CCM PFC IC

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***Keywords: PFC, Power Factor Correction, THD.***

# 1. Introduction

The IR1153 IC is a fixed 22.2kHz frequency PFC IC designed to operate in continuous conduction mode Boost converters with average current mode control. The IC is packed with an impressive array of advanced features such as programmable soft-start, micro-power startup current, user initiated micro-power Sleep mode for compliance with stand-by energy standards and ultra low bias currents for sensing pins. The fixed internal oscillator ensures stable operation at 22.2kHz switching frequency with very low gate jitter thus eliminating audible noise in PFC magnetics. In addition, the IC offers input-line sensed brown-out protection (BOP), dedicated overvoltage protection, cycle-by-cycle peak current limit, open loop protection (OLP) and VCC under voltage lock-out (UVLO). All these features are offered in a compact 8-pin package making IR1153 the most feature-intensive IC for PFC applications. This application note provides an overview of the IR1153 and demonstrates the design of a universal input 2000W AC-DC Boost PFC Converter. Design & layout tips are also included.

# 2. IR1153 – Detailed Description

## 2.1 Overview of IR1153

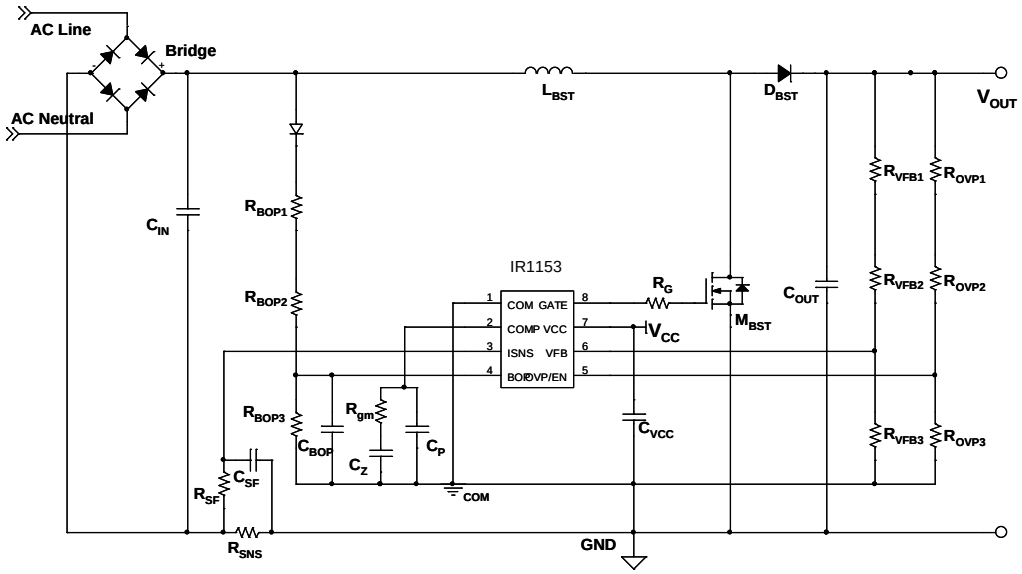


Fig.1: Typical application diagram of IR1153 based PFC converter

Fig.1 shows the system application diagram of the IR1153 based PFC converter. Only 3 pin functionalities - VFB, COMP & ISNS – are actually needed to obtain the necessary diagnostic signals to achieve power factor correction and maintain output voltage regulation. The functions of the abovementioned 3 pins are as follows:

- VFB – provides DC bus voltage sensing for voltage regulation
- COMP – used for compensating the voltage feedback loop to set the correct transient response characteristics
- ISNS – provides sensing of the inductor current, which is used to determine the PFC switch duty cycle

Essentially, there are 2 control loops in the PFC algorithm:

- a slow, outer voltage loop whose function is to simply maintain output voltage regulation
- a fast inner current loop whose function is to determine the instantaneous duty cycle every switching cycle

The current shaping function i.e. power factor correction is achieved primarily by the current loop. The voltage loop is responsible only for controlling the magnitude of the input current in order to maintain DC bus voltage regulation.

## 2.2 Key Features of IR1153

❖ *Fixed 22.2kHz Frequency Internal Oscillator*

IR1153 features a fixed frequency internal oscillator running at 22.2kHz. The gate drive pulse is completely free of jitter and this greatly enables elimination of audible noise in PFC magnetics due to magnetostriction. Also internalization of the oscillator greatly improves noise immunity of the IC.

❖ *Programmable soft-start*

IR1153 facilitates programmability of system soft-start time thus allowing the designer some freedom (taking into consideration the loop compensation characteristics) to choose the converter start-up times appropriate for the application. The soft start time is the time required for the $V_{COMP}$ voltage to charge through its entire dynamic range i.e. 0V through $V_{COMP,EFF}$. As a result, the soft-start time is dependent upon the component values selected for compensation of the voltage loop on the COMP pin – primarily the $C_Z$ capacitor (described in detail in *Soft-Start Design* section of PFC Converter Design portion of this document). As VCOMP voltage rises gradually, the IC allows a higher and higher RMS current into the PFC converter. This controlled increase of the input current contributes to reducing system component stress during start-up. It is clarified that, during soft-start, the IC is capable of full duty cycle modulation (from 0% to MAX DUTY), based on the instantaneous ISNS signal from system current sensing. Furthermore, the internal logic of the IC is designed to ensure that the soft-start capacitor is discharged when the IC enters the Sleep or Stand-by modes in order to facilitate soft-start upon restart.

❖ *User initiated micro-power sleep mode*

The IR1153 has an ENABLE function embedded in the OVP/EN pin. When this pin voltage is actively pulled below $V_{SLEEP}$ threshold, the IC is pushed into the Sleep mode where the current consumption is less than 75uA even when $V_{CC}$ is above $V_{CC,ON}$ threshold. The system designer can use an external logic level signal to access the ENABLE feature since $V_{SLEEP}$ threshold is so low. The IR1153 internal logic ensures that $V_{COMP}$ is discharged before the IC enters Sleep mode in order to enable soft-start upon resumption of operation.

❖ *Protection features*

The IR1153 features a comprehensive array of protection features to safeguard the system. These are explained below.

*1. Dedicated & Programmable Overvoltage protection (OVP)*

The OVP pin is a dedicated pin for overvoltage protection that safeguards the system even if there is a break in the VFB feedback loop due to resistor divider failure etc. An overvoltage fault is triggered when OVP pin voltage exceeds the $V_{OVP}$ threshold of 106%$V_{REF}$. The IC gate drive is immediately disabled and held in that state. The overvoltage fault is removed and gate drive re-enabled only when both pin voltages are below the $V_{OVP,RST}$ threshold of 103% $V_{REF}$. The exact voltage level at which overvoltage protection is triggered can be programmed by the user by carefully designing the OVP pin resistor divider. It is recommended NOT to set the OVP voltage trigger limit less than 106% of DC bus voltage, since this can endanger the situation where the OVP reset limit will be less than the DC bus voltage regulation point – in this condition the voltage loop can become unstable.

*2. Open-Loop protection (OLP)*

The open-loop protection ensures that the IC is restrained in the Stand-by mode if the VFB pin voltage has not exceeded or has dropped below $V_{OLP}$ threshold of 19%$V_{REF}$. In the Stand-by mode, all internal circuitry of the IC are biased, the gate drive is disabled and current consumption is a few milliamps. During start-up, if for some reason the voltage feedback loop is open then IC will remain in Stand-by and not start thus avoiding a potentially catastrophic failure.

*3. Brown-Out protection (BOP)*

IR1153 provides brown-out protection based on direct sensing of AC input line. Information about the rectified AC input voltage is communicated to the BOP pin after scaling it down using a resistor divider network and filtering using a capacitor on BOP pin. During start-up, the IC is held in Stand-by mode when BOP pin voltage is less than $V_{BOP(EN)}$ threshold of 1.56V. When the pin voltage exceeds this threshold, the IC enters normal operation (assuming no OLP condition exists). Subsequently, if the pin voltage falls below $V_{BOP}$ threshold of

0.76V during normal operation, then a brown-out fault is detected and IC is pushed into Stand-by mode. For the IC to exit Stand-by, the pin voltage has to exceed $V_{BOP(EN)}$ threshold again. In the Stand-by mode, all internal circuitry of the IC are biased, the gate drive is disabled and current consumption is a few milliamps.

*4. Cycle-by-cycle peak current limit protection (IPK LIMIT)*

The cycle-by-cycle peak current limit is encountered when $V_{ISNS}$ pin voltage exceeds $V_{ISNS(PK)}$ threshold of -0.51V (in magnitude). When this condition is encountered, the IC gate drive is immediately disabled and held in that state until the ISNS pin voltage falls below $V_{ISNS(PK)}$. Even though the IR1153 operates based on average current mode control, the input to the peak current limit comparator is decoupled from the averaging circuit thus enabling instantaneous cycle-by-cycle protection for peak current limitation.

*5. $V_{CC}$ UVLO*

In the event that the voltage at the $V_{CC}$ pin should drop below that of the VCC UVLO turn-off threshold, $V_{CC(UVLO)}$ the IC is pushed into the UVLO mode, the gate drive is terminated, and the turn on threshold, $V_{CC,\ ON}$ must again be exceeded in order to re start the process. In the UVLO mode, the current consumption is less than 75uA.

# 3. PFC Converter Design Procedure

## 3.1 PFC Converter Specifications

| | |
|---|---|
| AC Input Voltage Range | 170-264VAC |
| Input Line Frequency | 47-63Hz |
| Nominal DC Output Voltage | 385V +/- 5% |
| DC Bus Overvoltage Limit | 425V |
| Nominal Output Power | 2000W |
| Power Factor | 0.99 @ 230VAC/350W |
| Output Holdup Time | 20ms @ $V_{OUT,MIN}$=285V |
| Start-up time | 300ms |

Table 1: Design Specifications for PFC Converter

### 3.2 Power Circuit Design

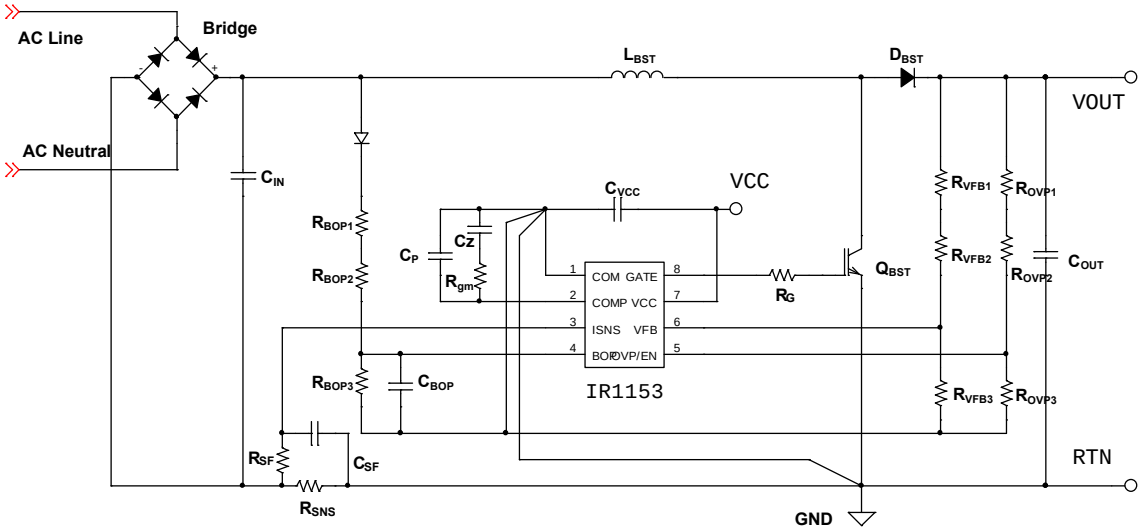


Fig.2: IR1153 based PFC Boost Converter

❖ *Peak Input Current*

It is necessary to determine the maximum input currents (RMS & peak) from the specifications in Table 1 before proceeding with detailed design of the PFC boost converter. The maximum input current is typically encountered at highest load & lowest input line situation (2000W, 170VAC). Assuming a nominal efficiency of 92% at this situation, the maximum input power can be calculated:

$$P_{IN(MAX)} = \frac{P_{O(MAX)}}{\eta_{MIN}} = \frac{2000W}{0.92} = 2174W$$

From this, the maximum RMS AC line current is then calculated:

$$I_{IN(RMS)MAX} = \frac{P_{O(MAX)}}{\eta_{MIN}(V_{IN(RMS)MIN})PF}$$

$$I_{IN(RMS)MAX} = \frac{2000W}{0.92(170V)0.998} = 12.8A$$

The selection of the semiconductor components (bridge rectifier, boost switch & boost diode) is based on $I_{IN(RMS)MAX}$ =12.8A.

Assuming a pure sinusoidal input, the maximum peak AC line current can then be calculated:

$$I_{IN(PK)MAX} = \frac{\sqrt{2}(P_{IN(MAX)})}{V_{IN(RMS)MIN}}$$

$$I_{IN(PK)MAX} = \frac{1.414(2174W)}{170V} = 18.1A$$

❖ *Boost Inductance ($L_{BST}$)*

IR1153 IC is an average current mode controller. An on-chip RC filter is sized to effectively filter the boost inductor current ripple to generate a clean average current signal for the IC. The averaging function in the IC can accommodate a maximum limit of 40% inductor current ripple factor at maximum input current. The boost inductance has to be sized so that the inductor ripple current factor is not more than 40% at maximum input current condition (at peak of AC sinusoid). This is because:

- Higher ripple current factors will interfere with the Average Current Mode operation of One Cycle Control algorithm in IR1153 leading to duty cycle instabilities and pulse skipping which results in current distortion and sometimes even audible noise
- power devices are stressed more with higher ripple currents as the peak inductor current ($I_{L(PK)MAX}$) also increases proportionately

In this calculation, an inductor current ripple factor of 35% is selected (typical ripple factor is ~20% for most PFC designs). The ripple current at peak of AC sinusoid at maximum input current is:

$$\Delta I_L = 0.35 \times I_{IN(PK)MAX}$$
$$\Delta I_L = 0.35 \times 18.1A = 6.3A$$

And, peak inductor current is:

$$I_{L(PK)MAX} = I_{IN(PK)MAX} + \frac{\Delta I_L}{2}$$
$$I_{L(PK)MAX} = 18.1A + \frac{6.3A}{2} = 21.3A$$

In order to determine the boost inductance, the power switch duty cycle at peak of AC sinusoid (at lowest input line of 170VAC) is required.

$$V_{IN(PK)MIN} = \sqrt{2} \times V_{IN(RMS)MIN} = 240V$$

Based on the boost converter voltage conversion ratio,

$$D = \frac{V_O - V_{IN(PK)MIN}}{V_O}$$
$$D = \frac{385V - 240V}{385V} = 0.38$$

The boost inductance is then given by:

$$L_{BST} = \frac{V_{IN(PEAK)MIN} \times D}{f_{SW} \times \Delta I_L} = \frac{240V \times 0.38}{22.2kHz \times 6.3A}$$
$$L_{BST} = 652\mu H$$

A convenient value of 700µH is selected for $L_{BST}$ for this converter.

❖ *High Frequency Input Capacitor ($C_{IN}$)*

The purpose of the high-frequency capacitor is to supply the high-frequency component of the inductor current (the ripple component) via the shortest possible loop. This has the advantage of acting like an EMI filter, since it minimizes the high-frequency current requirement from the AC line. Typically a high-frequency, film type capacitor with low ESL and high-voltage rating (630V) is used.

High-frequency input capacitor design is essentially a trade-off between:

- sizing it big enough to minimize the noise injected back into the AC line
- sizing it small enough to avoid line current zero-crossing distortion (flattening)

The high-frequency input capacitor is determined as follows:

$$C_{IN} = k_{\Delta I_L} \frac{I_{IN(RMS)MAX}}{2\pi \times f_{SW} \times r \times V_{IN(RMS)MIN}}$$

$$C_{IN} = 0.35 \frac{12.8A}{2\pi \times 22.2kHz \times 0.09 \times 170V}$$

$$C_{IN} = 2.1\mu F$$

where:

$k_{\Delta IL}$ = inductor current ripple factor, of 35% as mentioned earlier

*r* = maximum high frequency input voltage ripple factor ($\Delta V_{IN}/V_{IN}$), assumed 9%

A standard 2.2µF, 630V capacitor is selected for $C_{IN}$ for this converter.

❖ Output Capacitor ($C_{OUT}$)

Output Capacitor design is based on hold-up time requirement

For 20ms hold-up time and minimum output voltage of 285V the output capacitance is first calculated:

$$C_{OUT(MIN)} = \frac{2 \cdot P_O \cdot \Delta t}{V_O{}^2 - V_{O(MIN)}{}^2}$$

$$C_{OUT(MIN)} = \frac{2 \cdot 2000W \cdot 20ms}{(385V)^2 - (285V)^2}$$

$$C_{OUT(MIN)} = 1194\mu F$$

Minimum capacitor value must be de-rated for capacitor tolerance (20%) to guarantee minimum hold-up time.

$$C_{OUT} = \frac{C_{OUT(MIN)}}{1 - \Delta C_{TOL}} = \frac{1194\mu F}{1 - 0.2} = 1492.5\mu F$$

3 standard 470µF, 450V capacitors connected in parallel, which yields about 1410uF total can be selected for this converter. The hold-up time will be slightly less than 20ms in the worst case where the DC bus capacitances are at 80% of their rated value.

### 3.3 IR1153 Control Circuit Design

#### 3.3.1 Current Sense Resistor Design (ISNS pin)

In IR1153, there are two levels of current limitation:

- a “soft” current limit, which limits the duty-cycle and causes the DC bus voltage to fold-back i.e. droop
- a cycle-by-cycle “peak” current limit feature which immediately terminates gate drive pulse once the ISNS pin voltage exceeds $V_{ISNS,PEAK}$

❖ “Soft” Current Limit

In IR1153 the COMP pin voltage is directly proportional to the RMS input current into the PFC converter i.e. $V_{COMP}$ is higher at higher RMS current. Clearly its magnitude is highest at maximum load $P_{MAX}$ & minimum AC input voltage, $V_{IN,MIN}$. The dynamic range of $V_{COMP}$ in the IC is defined by $V_{COMP,EFF}$ parameter in the IR1153 datasheet. Once $V_{COMP}$ signal saturated (reaches $V_{COMP,EFF}$), any system requirement causing an additional increase in current will cause the IC to respond by limiting the duty cycle and thereby causing the output voltage to droop. This is called “soft” current limit protection. The selection of $R_{SNS}$ must ensure that “soft” current limit is not encountered at any of the allowable line and load conditions.

❖ $R_{SNS}$ Design

The design of $R_{SNS}$ is performed at the system condition when the inductor current is highest at lowest input line ($V_{IN,MIN}$) and highest load ($P_{MAX}$). Further, the inductor current is highest at the peak of the AC sinusoid. The duty cycle required at peak of AC sinusoid at $V_{IN,MIN}$=170VAC in order to regulate $V_{OUT}$=385V is:

$$D_{PEAK} = \frac{V_{OUT} - \sqrt{2}V_{IN(RMS)MIN}}{V_{OUT}}$$

$$D_{PEAK} = \frac{385V - \sqrt{2}.170V}{385V} = 0.38$$

$R_{SNS}$ design should guarantee that

i. PFC algorithm can deliver this duty cycle at peak of AC sinusoid at $V_{IN,MIN}$ & $P_{MAX}$ condition
ii. soft current limit is encountered whenever there is a further increase in demand for current while operating at $V_{IN,MIN}$ & $P_{MAX}$ condition

To do this, the $V_{ISNS}$ is calculated below.

$$V_{ISNS(MAX)} = \frac{V_{COMP(EFF)} \cdot (1 - D)}{g_{DC}}$$

$$V_{ISNS(MAX)} = \frac{4.7V \cdot (1 - 0.38)}{5.65} = 0.52V$$

The $V_{ISNS(MAX)}$ calculated above is very close to the cycle-by-cycle peak overcurrent limit specification of the IC.

| | | | | | | |
|---|---|---|---|---|---|---|
| Peak Current Limit Protection ISNS Voltage Threshold (IPK LIMIT) | $V_{ISNS(PK)}$ | -0.58 | -0.51 | -0.44 | V | Bias on ISNS pin |

Hence the driving consideration for choosing the current sense resistor for this converter is the Peak Overcurrent Protection and not the "Soft" Current Limit protection.

$$V_{ISNS(\max)} = 0.44V$$

Next the peak inductor current at 2000W, 170VAC condition de-rated with an overload factor $K_{OVL}$=110%, is calculated.

$$I_{IN(PK)OVL} = I_{L(PK)\max} \cdot (1 + K_{OVL})$$

$$I_{IN(PK)OVL} = 21.3 \times 1.1 = 23.4A$$

From this maximum current level and the required voltage on the current sense pin, we now calculate the maximum resistor value that can be used for the PFC converter.

$$R_{SNS,MAX} = \frac{V_{ISNS(\max)}}{I_{IN(PK)OVL}} = \frac{0.44V}{23.4A}$$

$$R_{SNS,MAX} = 0.0188\Omega$$

It is noted that even though IR1153 operates in average current mode it is still safer to use the peak inductor current for current sense resistor design to guarantee avoiding premature fold-back.

Power dissipation in the resistor is now calculated based on worst case RMS input current at minimum input voltage:

$$P_{R_S} = I_{IN(RMS)MAX}{}^2 \cdot R_S$$

$$P_{R_S} = 12.8^2 (0.0188\Omega) = 3.08W$$

❖ Peak Current Limit

The cycle-by-cycle peak current limit is encountered when $V_{ISNS}$ pin voltage exceeds $V_{ISNS,PEAK}$. For the PFC converter, this limit is typically encountered whenever the inductor current exceeds the following:

$$I_{PK\_LMT} = \frac{|-.51V|}{0.0188\Omega} = 27.1A$$

It is clarified that even though the IR1153 operates based on average current mode control, the input to the peak current limit comparator is decoupled from the averaging circuit thus enabling instantaneous cycle-by-cycle protection for peak overcurrent.

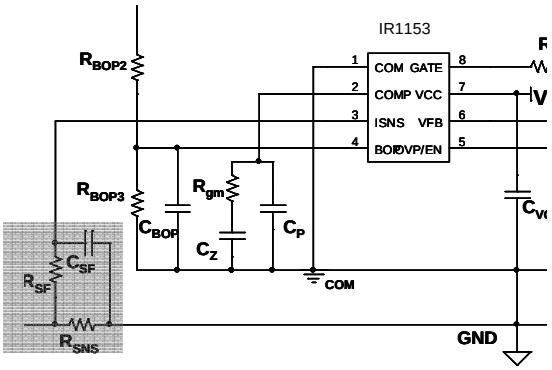


Fig.3: Current Sense Resistor and Filtering

The current sense signal is communicated to the ISNS pin of the IC using a current limiting series resistor, $R_{SF}$. An external RC filtering for ISNS pin can be realized (though not mandatory) by adding a filter capacitor, $C_{SF}$ between the ISNS pin and COM as shown in Fig.3. A corner frequency around 1-1.5MHz will offer a safe compromise in terms of filtering, while maintaining the integrity of the current sense signal for cycle-by-cycle peak overcurrent protection.

$$f_{PSF} = \frac{1}{2\pi \cdot R_{SF} \cdot C_{SF}}$$

With $R_{SF}$=100Ω, we can use $C_{SF}$=1000pF to obtain a cross-over frequency of 1.6MHz. The input impedance of the current sense amplifier is approximately 25KΩ. The $R_{SF}$ resistor will form a divider with this 25KΩ resistor. For $R_{SF}$=100Ω it is noted that the accuracy of the current sense voltage signal communicated to the IC is more than 99.5%.

### 3.3.2 Output Regulation Voltage Divider (VFB pin)

The output regulation voltage of the PFC converter is set by voltage divider on VFB pin - $R_{FB1}$, $R_{FB2}$, and $R_{FB3}$. The total impedance of this divider network must be high enough to reduce power dissipation, but low enough to keep the feedback voltage error (due to finite bias currents into the voltage error amplifier which is less than 1uA) negligible. Around 2MΩ is an acceptable value for the total resistor divider impedance.

A standard 1MΩ, 1% tolerance resistor is selected for $R_{FB1}$ & $R_{FB2}$ for this converter. Then, $R_{FB3}$ is determined based on error amplifier $V_{REF}$ (Typ)=5V and $V_{OUT}$=385V converter specification.

$$R_{FB3} = \frac{V_{REF}(R_{FB1} + R_{FB2})}{(V_{out} - V_{REF})}$$

$$R_{FB3} = \frac{5.0V(2000k)}{(385\text{V} - 5.0\text{V})} = 26.3k\Omega$$

A standard resistor, $R_{FB3}$ = 26.1kΩ, 1% tolerance, is selected for this converter.

The new regulation $V_{OUT}$ value based on actual resistor values is then calculated.

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2} + R_{FB3}) \cdot V_{REF}}{R_{FB3}}$$

$$V_{OUT} = \frac{(2000k + 26.1k) \cdot 5.0V}{26.1k} = 388.1V$$

Power dissipation of divider resistors is given by the following.

$$P_{R_{FB1}} = P_{R_{FB2}} = \frac{(V_{out} - V_{REF})^2}{2(R_{FB1} + R_{FB2})}$$

$$P_{R_{FB1}} = P_{R_{FB2}} = \frac{(388.1V - 5V)^2}{4 \times 1000k} = 37mW$$

VFB is a multi-function pin. The VFB pin is also an input to the open-loop comparator that references a $V_{OLP}$ threshold of 19% of $V_{REF}$. The IC is restrained in the Stand-by Mode whenever VFB pin is less than $V_{OLP}$ or in other words when $V_{OUT}$ drops below ~74V.

### 3.3.3 Dedicated Overvoltage Protection Divider (OVP/EN pin)

The OVP pin is non-inverting input to the overvoltage comparator. The typical overvoltage set-point is $V_{OVP}$=106%$V_{REF}$ and the re-enable set-point is $V_{OVP(RST)}$=103%$V_{REF}$.

$$V_{OVP} = 1.06 \cdot V_{REF} = 5.30V$$

$$V_{OVP(RST)} = 1.03 \cdot V_{REF} = 5.15V$$

The overvoltage protection limit can be programmed by designing the appropriate resistor divider.

If the same resistor divider as VFB pin is used (1Mohm, 1Mohm, 26.1kohm), then the Overvoltage protection limit and re-enable set-point are easily calculated as follows:

$$V_{OVP} = 1.06 \cdot V_{Out}$$
$$V_{OVP} = 1.06 \times 388.1 = 412V$$
$$V_{OVP\,(RST)} = 1.03 \cdot V_{Out}$$
$$V_{OVP\,(RST)} = 1.03 \times 388.1 = 400\,V$$

Alternately, if the overvoltage protection limit is required to be $V_{OVP}$, then the appropriate resistor divider setting can be calculated as follows:

$$R_{OVP3} = \frac{1.06 \cdot V_{REF}\,(R_{OVP1} + R_{OVP2})}{(V_{OVP} - 1.06 \cdot V_{REF})}$$

For example, if $V_{OVP}$ is desired to be 425V (as is the case many times, since the DC bus capacitor is usually rated 450V) and selecting $R_{OVP1}$=$R_{OVP2}$=1Mohm, then $R_{OVP3}$ can be calculated:

$$R_{OVP3} = \frac{1.06 \cdot 5V\,(1Mohm + 1Mohm)}{(425V - 1.06 \cdot 5\mathrm{V})}$$
$$R_{OVP3} = 25.3kohm$$

In this design, the IC will enter OVP when $V_{OUT}$=425V and disable gate output. The gate outputs are re-enabled once the bus voltage drops below the OVP re-enable setpoint, $V_{OVP(RST)}$, which is calculated as follows:

$$V_{OVP\,(RST)} = \frac{1.03}{1.06} \times V_{OVP}$$
$$V_{OVP\,(RST)} = \frac{1.03}{1.06} \times 425\,V$$
$$V_{OVP\,(RST)} = 413V$$

In this converter, for $V_{OVP}$=425V, then the following resistor divider is selected: $R_{OVP1}$ = $R_{OVP2}$ = 1Mohm, $R_{OVP3}$ = 25.3kohm at 1% tolerance level.

Caution: When selecting the overvoltage limit, $V_{OVP}$ and designing the OVP pin resistor divider, it is important to ensure that the resulting re-enable set-point $V_{OVP(RST)}$ does not turn-out to be less than the DC bus regulation voltage, $V_{OUT}$. Such a design can cause hysteretic oscillations whenever the overvoltage situation is encountered and the system attempts to get back into regulation. It is recommended that the minimum OVP limit be at least equal to 106% of the DC bus regulation voltage i.e. Minimum $V_{OVP} \geq 106\% V_{OUT}$. This will ensure that $V_{OVP(RST)}$ is always greater than the DC bus regulation voltage $V_{OUT}$.

### 3.3.4 Brown-Out Protection R/C Circuit (BOP pin)

IR1153 provides brown-out protection based on direct sensing of rectified AC input line. Information about the rectified AC input voltage is communicated to the BOP pin after scaling it down using a resistor divider network and filtering using a capacitor on BOP pin as shown below. This R/C network is essentially a voltage-

division/averaging network. The sinusoidally varying rectified AC voltage is divided by the resistor divider and averaged by the capacitor and presented at the BOP pin as a DC level, $V_{BOP, AVG}$ along with some ripple, $\Delta V_{BOP}$. The BOP pin R/C circuit is illustrated in Fig.4. The BOP pin voltage is illustrated in Fig.5.

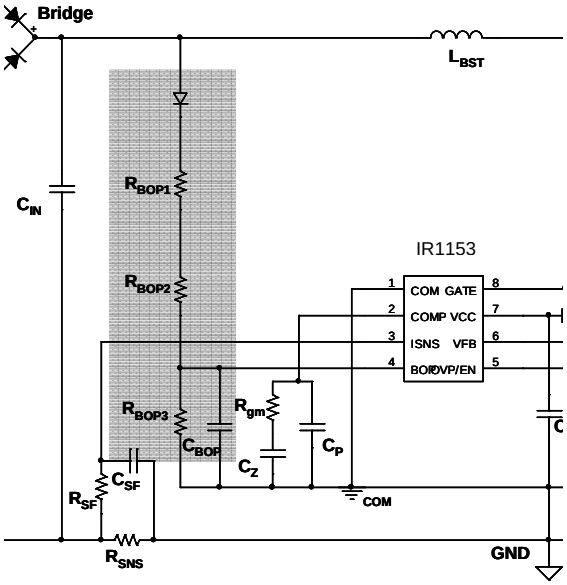


Fig.4: Brown-out protection circuit for IR1153

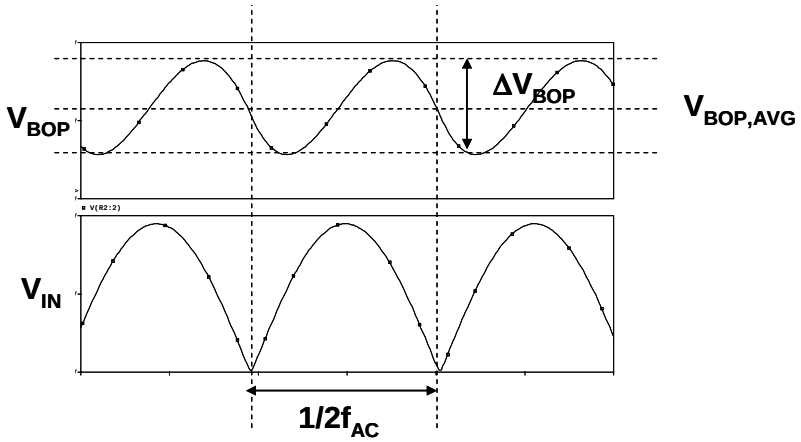


Fig.5: Voltage waveform on the BOP pin is comprises a DC level ($V_{BOP,AVG}$) and a ripple voltage ($\Delta V_{BOP}$)

The DC level $V_{BOP,AVG}$ is given by:

$$V_{BOP,AVG} = \frac{R_{BOP3}}{R_{TOT}} \cdot V_{ACAVG}$$

where

$$R_{TOT} = R_{BOP1}+R_{BOP2}+R_{BOP3}$$

$$V_{AC,AVG} = \frac{2}{\pi}\sqrt{2}\cdot V_{IN(RMS)}$$

Hence:

$$V_{BOP,AVG} = \frac{R_{BOP3}}{R_{TOT}}\cdot\frac{2}{\pi}\sqrt{2}\cdot V_{IN(RMS)}$$

Thus $V_{BOP,AVG}$ depends only on the resistor divider and the AC input voltage.

The ripple $\Delta V_{BOP}$ is given by the transfer function represented by the resistor divider and the capacitor:

$$T(s) = \frac{\Delta V_{BOP}}{V_{AC,PK}} = \frac{R_{BOP3}}{R_{TOT}}\cdot\frac{1}{1+sC_{BOP}\cdot\frac{(R_{BOP1}+R_{BOP2})R_{BOP3}}{R_{TOT}}}$$

Thus:

$$\left|\Delta V_{BOP}\right| = \sqrt{2}\cdot V_{IN(RMS)}\cdot\frac{R_{BOP3}}{R_{TOT}}\cdot\frac{1}{\sqrt{1+(\frac{\omega}{\omega_O})^2}}$$

where:

$$\omega = 2\pi\cdot(2\cdot f_{AC})$$

$$\omega_O = \frac{R_{TOT}}{(R_{BOP1}+R_{BOP2})\cdot R_{BOP3}\cdot C_{BOP}}$$

$\Delta V_{BOP}$ magnitude is related to $C_{BOP}$ – bigger the capacitor, smaller the ripple.

During start-up, the IC is held in Stand-by mode when the BOP pin voltage, $V_{BOP}$ is less than $V_{BOP(EN)}$=1.56V. Next, when the AC voltage is applied and the BOP pin voltage exceeds this threshold, the IC enters normal operation (assuming all other conditions for normal operation are satisfied). If it is assumed that the system is starting under no load, then the rectified AC voltage is essentially a DC voltage and the BOP pin voltage is also DC.

$$V_{BOP} = \frac{R_{BOP3}}{R_{TOT}}\cdot V_{AC,PK} = \frac{R_{BOP3}}{R_{TOT}}\cdot\sqrt{2}\cdot V_{IN(RMS)}$$

Under this condition, the AC voltage at which the IC becomes operational is given by:

$$\frac{R_{BOP3}}{R_{TOT}}\cdot\sqrt{2}\cdot V_{IN,ON(RMS)} > 1.56V$$

However, if the system is starting up under a loaded condition, then the rectified AC voltage is a varying sinusoidal function. In this case, the BOP pin voltage is as described before (DC level + superimposed ripple). In this case, the IC becomes operational when the maxima of $V_{BOP}$ exceeds $V_{BOP(EN)}$=1.56V.

$$V_{BOP,MAX} = V_{BOP,AVG} + \Delta V_{BOP}/2 \;>\; 1.56V$$

Hence the exact AC voltage at which the IC becomes operational depends on the load condition at start-up. $C_{BOP}$ must be big enough to ensure that $\Delta V_{BOP}$ is greater than the BOP hysteresis (1.56-0.76=0.8V) at the required minimum AC input voltage, should the system start-up under a loaded condition.

Once the IC becomes operational and starts boosting the DC voltage, then the rectified AC voltage will show sinusoidal variation. Subsequently, if the AC voltage is reduced then $V_{BOP,AVG}$ & $\Delta V_{BOP}$ both decrease in magnitude. When the minima of the BOP pin voltage encounters the Brown-out trip threshold $V_{BOP}$=0.76V then the IC enters brown-out fault mode.

$$V_{BOP,MIN} = V_{BOP,AVG} - \Delta V_{BOP}/2$$

When a Brown-out fault is encountered, the gate pulse is immediately terminated, the COMP pin is actively discharged, ICC current consumption falls to a few milli-amperes and the BOP pin voltage has to exceed $V_{BOP,EN}$ once again for the IC to restart.

The condition at which IC enters Brown-Out fault is then given by:

$$V_{BOP,MIN} < 0.76V$$

The high input impedance and low bias current (<1uA) of the BOP comparator allows a high impedance to be used for the BOP divider network. 5-10MΩ is an acceptable range. A standard 3MΩ, 1% tolerance resistor is selected for $R_{BOP1}$ & $R_{BOP2}$ for this converter. $R_{BOP3}$ is selected based on $V_{AC,ON}$, the AC input voltage at which the converter is expected to start-up. Assuming $V_{AC,ON}$=160VAC and no-load condition at start-up,

$$R_{BOP3} = \frac{V_{BOP(HI)}(R_{BOP1} + R_{BOP2})}{(\sqrt{2}.V_{AC,ON} - V_{BOP(HI)} - V_{Bridge})}$$

$$R_{BOP3} = \frac{1.56V(3M\Omega + 3M\Omega)}{(\sqrt{2}.160VAC - 1.56\text{V} - 2\text{V})}$$

$$R_{BOP3} = 42k\Omega$$

Next, assuming a target $V_{AC,OFF}$=150VAC, $C_{BOP}$ has to be selected. First $V_{BOP,AVG}$ is calculated at $V_{AC,OFF}$:

$$V_{BOP,AVG} = \frac{\sqrt{2}.V_{AC,OFF}(R_{BOP3})}{(\pi/2).(R_{BOP1} + R_{BOP2} + R_{BOP3})}$$

$$V_{BOP,AVG} = \frac{\sqrt{2}.150VAC.42kohm}{(\pi/2).(3Mohm + 3Mohm + 42kohm)}$$

$$V_{BOP,AVG} = 0.94V$$

Then, forcing $V_{BOP,MIN}$ (=$V_{BOP,AVG}$ - $\Delta V_{BOP}/2$) = 0.76V, we can calculate the required $\Delta V_{BOP}$ at $V_{AC,OFF}$. At $V_{AC,OFF}$=150VAC, this yields

$$\Delta V_{BOP} = 2*(0.94-0.76) = 0.36V$$

In order to calculate $C_{BOP}$, we just have to force the magnitude of the transfer-function at f=2*$f_{AC}$=126Hz to be equal to 0.36V calculated above (maximum $f_{AC}$ is the design condition that needs to be considered to ensure that the IC is guaranteed to terminate operation at $V_{AC,OFF}$. At a lower $f_{AC}$, when there is higher ripple, the IC will cease operation at a higher $V_{AC}$). Thus:

$$\left|\Delta V_{BOP}\right| = \sqrt{2}\cdot V_{AC,OFF}\cdot\frac{R_{BOP3}}{R_{TOT}}\cdot\frac{1}{\sqrt{1+(\frac{\omega}{\omega_O})^2}} = 0.36V$$

where:

$$\omega = 2\pi\cdot(2\cdot f_{AC})$$

$$\omega_O = \frac{R_{TOT}}{(R_{BOP1}+R_{BOP2})\cdot R_{BOP3}\cdot C_{BOP}}$$

$$\frac{1}{\sqrt{1+(\frac{\omega}{\omega_O})^2}} = 0.36V\times\frac{R_{TOT}}{R_{BOP3}}\times\frac{1}{\sqrt{2}\cdot V_{AC,OFF}} = 0.36V\times\frac{6.042Mohm}{0.042Mohm}\times\frac{1}{\sqrt{2}\cdot 150Vac} = 0.244$$

$$\omega = 2\pi\cdot(2\cdot f_{AC}) = 2\pi\cdot(2\cdot 63) = 791.68$$

$\omega_o$ is then calculated to be:

$\omega_o$ = 199

From $\omega_o$, $C_{BOP}$ is calculated:

$$C_{BOP} = \frac{R_{TOT}}{(R_{BOP1}+R_{BOP2})\cdot R_{BOP3}\cdot\omega_O} = \frac{6.042Mohm}{6Mohm\times 0.042Mohm\times 199} = 120nF$$

For the converter, we can choose the following:

$R_{BOP1}$ = $R_{BOP2}$ = 3Mohm

$R_{BOP3}$ = 42kohm

$C_{BOP}$=150nF

Since selected $C_{BOP}$ is higher than what was calculated, $V_{AC,OFF}$ will be lower than 150VAC (~141VAC).

### 3.3.5 Voltage Loop Compensation (COMP pin)

The voltage feedback loop monitors the DC bus voltage ($V_{OUT}$) via the $V_{FB}$ resistor divider whose transfer function is $H_1(s)$. Comparison of the $V_{FB}$ pin voltage and internal reference voltage of the IC by voltage error amplifier yields a control signal ($V_m$ = $V_{COMP}$-$V_{COMP,START}$). The transfer function of the error amplifier and compensation network is $H_2(s)$. The IR1153 output voltage error amplifier is a trans-conductance type amplifier and output of the error amplifier is connected to the COMP pin. The control signal directly controls the magnitude of the boost inductor current ($I_L$), which is also the input current of the PFC converter. The transfer function between $I_L$ and control signal $V_m$ is given by $H_3(s)$. The power stage of the PFC converter along with DC bus capacitor, maintains a constant voltage ($V_{OUT}$) at the converter output where the system load draws energy from the converter. The power stage + DC bus capacitor + system load transfer function is given by G(s). The small-signal model of the voltage feedback loop is depicted below in Fig.6. The overall loop gain transfer function *T(s)* is given by:

$$T(s) = H_1(s).H_2(s).H_3(s).G(s)$$

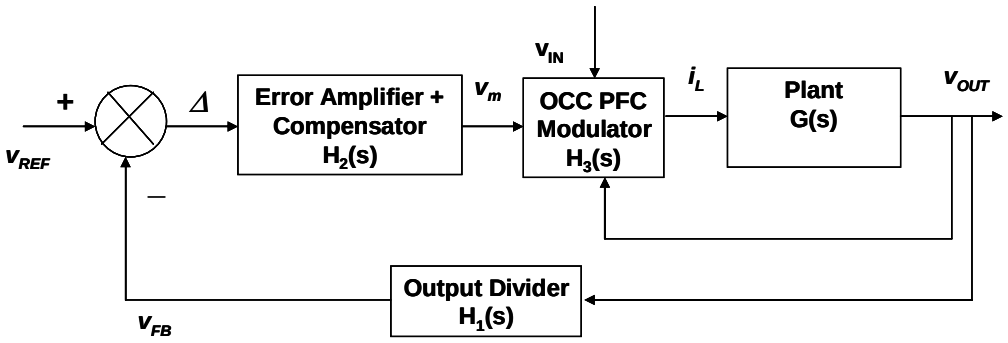


Fig.6: Small-signal modeling of the PFC voltage feedback loop

Voltage loop compensation is performed by adding R/C components between COMP and COM pins in order to:

i. Achieve the appropriate dynamic response characteristics during load/line fluctuations
ii. Ensure that the 2*$f_{AC}$ ripple in $V_{OUT}$ at steady state conditions, does not cause too much current distortion

In order to evaluate the overall loop gain transfer function *T(s)*, the small-signal transfer function of each of the blocks has to be evaluated first.

❖ Plant Gain, *G(s)*

The plant gain G(s) models the small signal variation in the DC bus voltage when a small perturbation occurs in the boost inductor current.

$$G(s) = v_{OUT}/i_L = (v_{OUT}/i_{CHG}).(i_{CHG}/i_L)$$

where the small signal parameters are italicized and $i_L$ is the boost inductor current, $v_{OUT}$ is the bus voltage and $i_{CHG}$ is the current sourced at the output of the boost converter power stage (i.e. boost diode current).

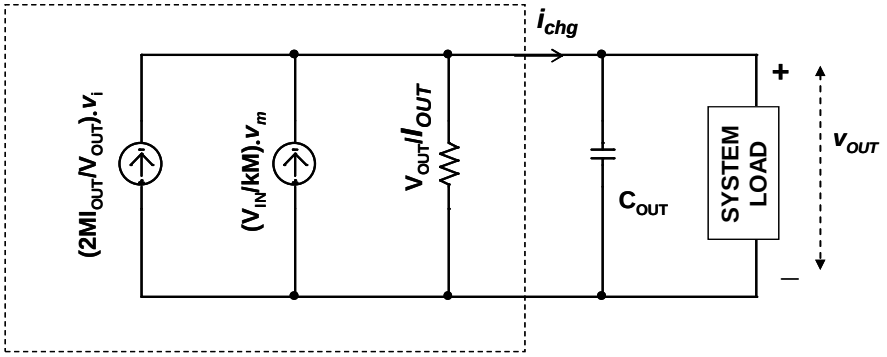


Fig.7: Small-signal model of PFC converter power stage

If the system load is a **Resistive Load**, the transfer function is:

$$\frac{v_{out}}{i_{chg}} = \frac{R_L/2}{1 + sC_{out}\frac{R_L}{2}}$$

In the power stage transfer function, this is represented by a pole:

$$f_{PS} = \frac{1}{2\pi \cdot C_{out}\frac{R_L}{2}}$$

For a **Constant Power Load**, the shunt impedance and the system load cancel each other out and the equivalent impedance is infinite, in which case the transfer function reduces to:

$$\frac{v_{out}}{i_{chg}} = \frac{1}{sC_{out}}$$

In the power stage transfer function, this is represented by a pole at the origin.

Under a **Constant Current Load**, since the impedance of a current source is infinitely high, the equivalent impedance is effectively just the shunt impedance:

$$\frac{v_{out}}{i_{chg}} = \frac{R_L}{1 + sC_{out}R_L}$$

In the power stage transfer function, this is represented by a pole:

$$f_{PS} = \frac{1}{2\pi \cdot C_{out} R_L}$$

Next *($i_{CHG}/i_L$)* transfer function has to be evaluated. Assuming 100% efficiency, recognize that:

$$V_{IN}.I_L = V_{OUT}I_{OUT}$$

$I_{OUT}$ is same as the DC component of the boost diode current ($I_{CHG}$). Hence

$$V_{IN}.I_L = V_{OUT}I_{CHG}$$

Applying linearization and small-signal analysis, for a given DC operating point defined by $V_{IN}$ & $V_{OUT}$ yields the relationship between $i_{CHG}$ & $i_L$:

$$i_{CHG}/i_L = V_{IN}/V_{OUT}$$

Assuming a resistive load, the overall power stage transfer function can now be written as:

$$G(s) = \frac{V_{IN}}{V_{OUT}} \times \frac{R_L/2}{1 + sC_{out}\frac{R_L}{2}}$$

❖ OCC PFC Modulator, *$H_3(s)$*

In order to derive $i_L/v_m$, the One Cycle Control PWM modulator control law is employed:

$$G_{DC} \cdot R_S \cdot i_L = \frac{v_m}{M(d)}$$

where M(d) = $V_{OUT}/V_{IN}$ for a given DC operating point defined by the DC bus voltage $V_{OUT}$ and RMS input voltage $V_{IN}$. This ultimately yields

$$H_3(s) = \frac{i_L}{v_m} = \frac{V_{in}}{V_{OUT} R_S G_{DC}}$$

❖ Output voltage sensor Resistor-Divider, *$H_1(s)$*

The output divider scales the output voltage to be compared with the reference voltage in the error amplifier.

Therefore:

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2} + R_{FB3})V_{REF}}{R_{FB3}}$$

$$H_1(s) = \frac{V_{REF}}{V_{OUT}}$$

The uncompensated loop gain and phase is shown in Fig.8 for 170-264VAC at 2000W load condition (assuming resistive load). This is simply the

$H_1(s).H_3(s).G(s)$ transfer function product illustrating the pole due to the plant gain.

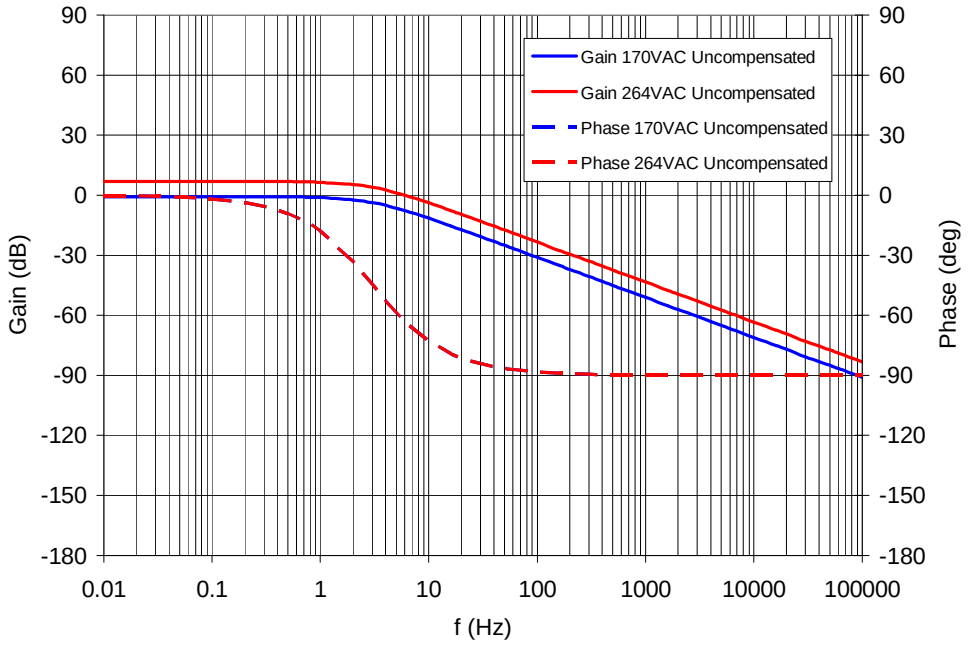


Fig.8 The uncompensated transfer function [=$H_1(s).H_3(s).G(s)$] at 170/264VAC & 2000W

❖ Error Amplifier & Compensation, *$H_2(S)$*

The compensation scheme typically employed for a first-order, single-pole system aims to:

- add a pole at the origin in order to increase the low frequency gain and improve DC regulation
- add a low-frequency zero to boost phase margin near cross-over frequency and partially compensate the pole
- add a high-frequency pole to attenuate switching frequency noise and ripple effects

The above 3 requirements can be achieved in case of the transconductance type voltage error amplifier with the compensation scheme shown in Fig.9. However, as mentioned earlier, for the PFC converter, the most important criterion for basing the selection of the compensation component values is the voltage loop bandwidth.

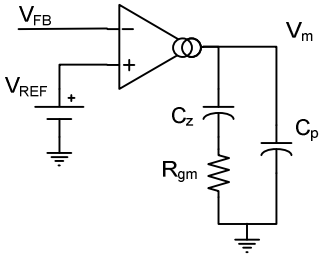


Fig.9: Voltage Loop error amplifier compensation network

The error amplifier transfer function is given by:

$$H_2(s) = \frac{g_m \cdot (1 + sR_{gm}C_Z)}{s(C_Z + C_P + sR_{gm}C_ZC_P)}$$

where $g_m$ is the transconductance of the voltage error amplifier. The compensation network adds a zero and a pole in the transfer function at:

$$f_{Z0} = \frac{1}{2\pi \cdot R_{gm} \cdot C_Z}$$

$$f_{P0} = \frac{1}{2\pi \cdot R_{gm} \frac{Cz \cdot Cp}{Cz + Cp}}$$

The gain and phase of the error amplifier + compensation transfer function is illustrated in Fig.10.

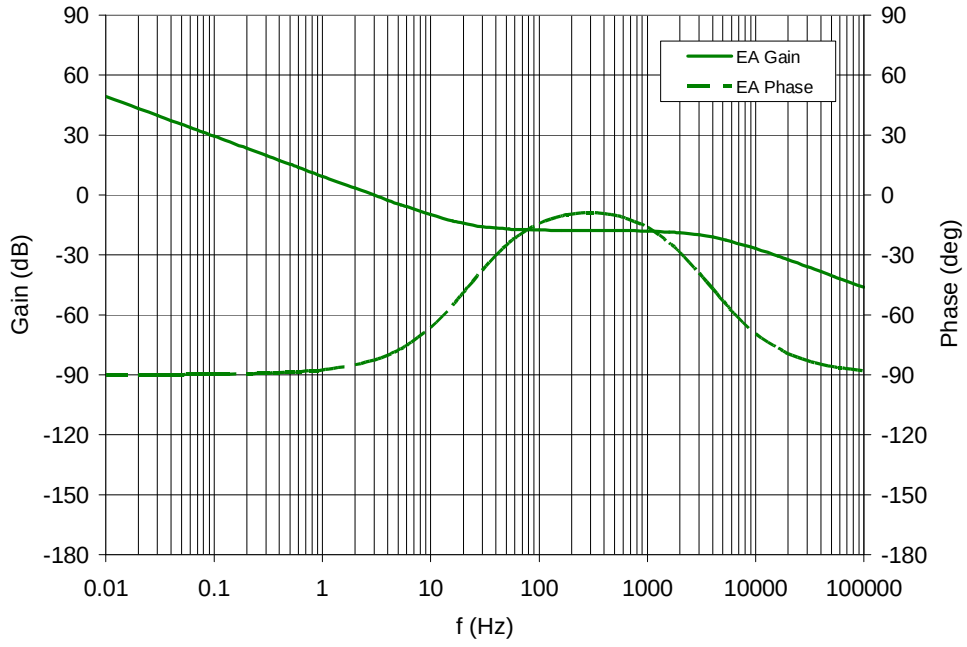


Fig.10: Error Amplifier + compensation transfer function characteristics

❖ Voltage Loop Compensation procedure

Step 1: Choose Cz based on soft-start time:

A soft-start time of 300ms is selected. The soft-start time represents the time needed by the controller to ramp $V_{COMP}$ from zero to the maximum value. In other words, even when current demand at start-up is highest (lowest line and highest load start-up situation), the system will take no more than 300ms to achieve near-regulation.

$$C_Z = \frac{t_{SS} \cdot i_{OVEA}}{V_{COMP(EFF)}(MIN)}$$

$i_{OVEA}$ and $V_{COMP(EFF)}$(MIN) are taken from the datasheet.

$$C_Z = \frac{300ms \times 44\mu A}{4.7V} = 2.8\mu F$$

Step 2: Choose $R_{gm}$ to ensure that $H_1(s).H_2(s)$ attenuation at 2xfAC frequency is small enough to avoid current distortion:

The amount of $2xf_{AC}$ ripple on the output capacitor is calculated first. The minimum $f_{AC}$ of 47Hz is considered here, since the ripple is the maximum at the lowest AC frequency. The peak-to-zero ripple $V_{OPK}$ is given by:

$$V_{OPK} = \frac{P_{in,MAX}}{2\pi \cdot 2 \cdot f_{AC} \cdot C_O \cdot V_{out}}$$

$$V_{OPK} = \frac{2173W}{2\pi \cdot 2 \cdot 47 \cdot 1410\mu F \cdot 385V}$$

$$V_{OPK} = 6.8V$$

The peak-to-peak ripple in $V_{OUT}$ is $2xV_{OPK}$. This ripple in $V_{OUT}$ is reflected in the $V_{COMP}$ voltage based on the attenuation provided by the resistor divider and error amplifier compensation network combined i.e. $H_1(s).H_2(s)$ at $2xf_{AC}$. The ripple in $V_{COMP}$ i.e. $\Delta V_{COMP}$ has to be small compared with the value of the error amplifier output voltage swing ($V_{COMP,EFF}$). Typical values for $\Delta V_{COMP}/V_{COMP}$ range from 0.5% to 1%. 0.5% is recommended if current shaping has to be excellent while 1% is recommended for higher phase margin and low-oscillation response to load steps. 0.5% attenuation demands a ($G_{VA}$) of:

$$G_{VA} = \frac{V_{COMP(EFF)} \cdot 0.005}{2 \cdot V_{OPK}}$$

$$G_{VA} = \frac{4.7V \cdot 0.005}{2 \cdot 6.8V} = 0.00173$$

$$G_{VA} = -55.2dB$$

This is the required attenuation in $H_1(s).H_2(s)$ at $2xf_{AC}$ frequency.

$H_1(s)$, given by $V_{REF}/V_{OUT,}$ is next calculated:

$$H_1 = \frac{5V}{385V} = 0.013 = -37.7dB$$

The required attenuation from $H_2(s)$ alone at 2x47Hz is then given by:

$$G_{VA} - H_1 = -17.5dB$$

Since the error amplifier pole will be set at a much higher frequency than $2xf_{AC}$ (and consequently $C_z >> C_p$), the error amplifier transfer function at $2xf_{AC}$ can be approximated to:

$$H_2(s) \cong \frac{g_m \cdot (1 + sR_{gm}C_Z)}{sC_Z}$$

Since $C_Z$ has already been determined, only $R_{gm}$ needs to be calculated by forcing:

$$\left|H_2(j2\pi \cdot f_{AC})\right| = G_{VA} - H_1 = -17.5dB = 0.133$$

$$R_{gm} = \sqrt{\left(\frac{G_{VA} - H_1}{g_m}\right)^2 - \left(\frac{1}{2\pi \cdot 2 \cdot f_{AC} \cdot C_Z}\right)^2}$$

Substituting $f_{AC}$=47Hz, $g_m$=49µS, $C_Z$=2.8µF yields

$$R_{gm} = 2.65k\Omega$$

The location of the zero in the compensation scheme can now be estimated:

$f_z = 1/(2*\pi*R_{gm}.C_z) = 1/(2*3.14*2.65kohm*2.8\mu F) = 21.4Hz$

The location of the pole in the power stage transfer function (assuming a resistive load) is:

$f_{PS} = 1/(2*\pi*C_{OUT}*R_L/2) = 1/[2*\pi*1410uF*(385V*385V/2000W)/2] = 3Hz$

The location of compensation zero is a less than a decade away from that of the pole. The phase boost from this compensation zero will result in greater than 45 degrees phase margin.

Step 3: Choose Cp based on high-frequency pole location

The pole frequency should be chosen higher than the cross over frequency and significantly lower than the switching frequency in order to attenuate switching noise and switching frequency ripple in the output capacitor: typical value is 1/6 to 1/10 of the switching frequency. Choosing $1/6xf_{SW}$ (=0.166*22.2kHz=3.7kHz) for this converter:

$$f_{P0} = \frac{1}{2\pi \cdot R_{gm} \dfrac{Cz \cdot Cp}{Cz + Cp}} \cong \frac{1}{2\pi \cdot R_{gm} \cdot Cp}$$

$$C_p = \frac{1}{2\pi \cdot 2.65k\Omega \cdot 22.2kHz \cdot 0.166} = 16nF$$

Step 4: Estimate bandwidth & phase margin

The voltage loop response for 170VAC and 264VAC is plotted at full load condition in Fig.11. At 170VAC/2000W the cross-over frequency is 2.1Hz and phase margin is 61°. At 264VAC/2000W the cross-over frequency is 3.9Hz and phase margin is 48°. This compensation scheme ensures that PFC converter has cross-over frequency less than ½x$f_{AC}$, low magnitude of 2x$f_{AC}$ ripple on VCOMP and adequate phase margin. It satisfies all the requirements of the design.

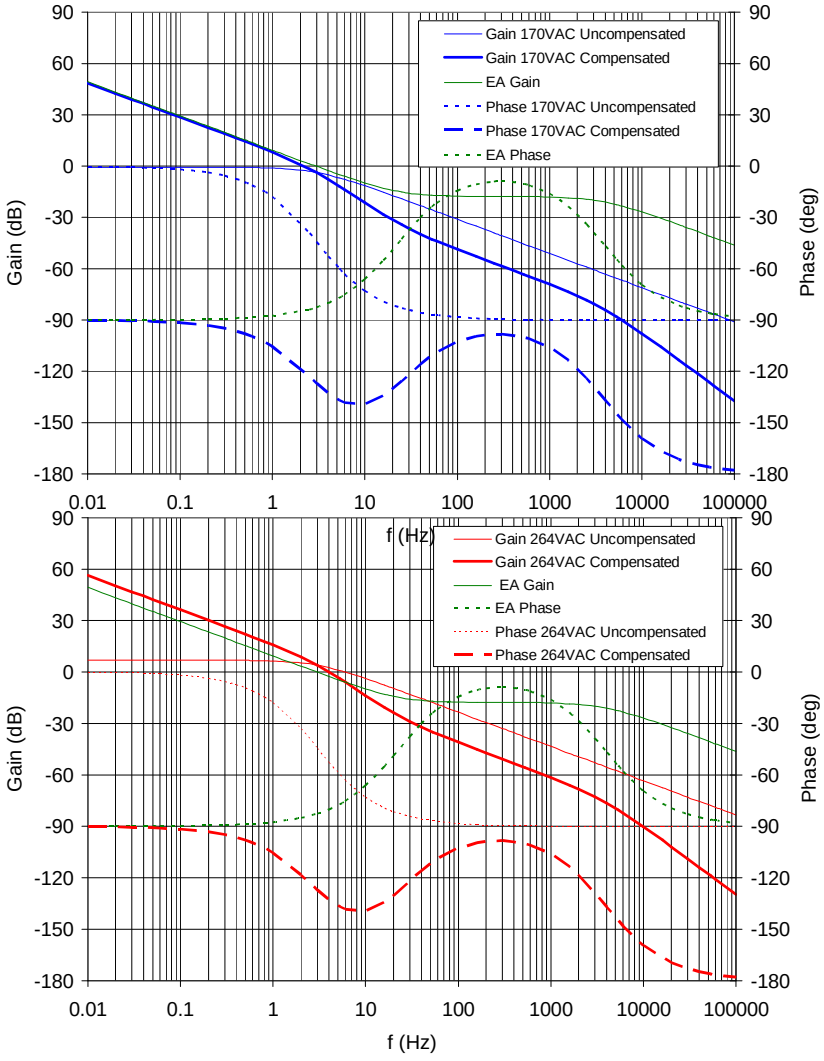


Fig.11: Overall Loop Gain at 170/264VAC & 2000W

It is instructive to study the compensation for slightly different system designs:

Case1: What happens if the system is designed for a much smaller start-up time? For example, if the soft-start time is decreased to 100ms (1/3x reduction), then re-calculating according to the procedure described above yields Cz=0.93uF, Rgm=2kohm, Cp=21nF. The cross-over frequency and phase margin are 4.3Hz & 38° at 170VAC and 7.1Hz and 28° at 264VAC as seen in Fig.12 below. Due to the lower Cz capacitor, the low frequency gain is increased and hence the band-width is increased. But the location of the zero is further away from the power stage pole, so the phase margin will be reduced resulting in a more oscillatory response to $V_{OUT}$ when there is a load step.

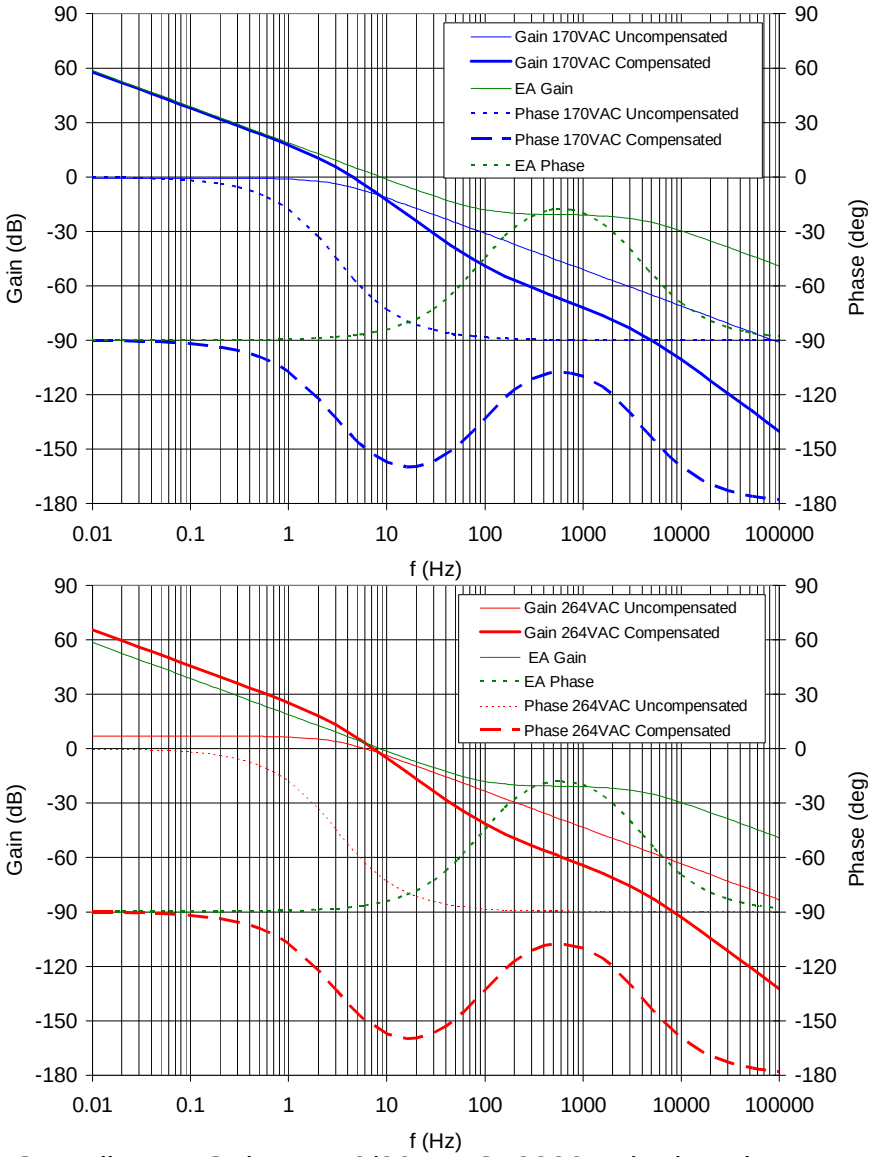


Fig.12: Overall Loop Gain at 170/264VAC, 2000W (reduced start-up time causes lower phase margin)

Case2: What happens if the system is designed for a much smaller hold-up time? For example, if the bus capacitor is reduced to 2x470uF=940uF. Running the calculations again

$$V_{OPK} = \frac{2173W}{2\pi \cdot 2 \cdot 47 \cdot 940\mu F \cdot 385V}$$
$$V_{OPK} = 10.2V$$

$$G_{VA} = \frac{4.7V \cdot 0.005}{2 \cdot 10.2V} = 0.00115$$
$$G_{VA} = -58.7dB$$

The required attenuation from $H_2(s)$ alone at 2x47Hz is then given by:

$$G_{VA} - H_1 = -21dB$$

Recalculating the compensation components according to the procedure above:

Assuming a start-up time of 100ms yields $C_z$=0.93uF. Next, $R_{gm}$ is determined using:

$$R_{gm} = \sqrt{\left(\frac{G_{VA} - H_1}{g_m}\right)^2 - \left(\frac{1}{2\pi \cdot 2 \cdot f_{AC} \cdot C_Z}\right)^2}$$

If the math is performed, it will be seen that the $R_{gm}$ calculation using above equation will yield an imaginary value. What this means is that the attenuation provided by the error amplifier's origin pole is not quite enough to achieve the 0.5% $2xf_{AC}$ ripple requirement in $V_{COMP}$ for current distortion considerations [The $2xf_{AC}$ ripple in $V_{COMP}$ pin must be restricted to less than 0.5% ($\Delta V_{COMP}/V_{COMP}$) in order to avoid any noticeable current distortion]. In this case, there is no choice but to decrease the low frequency gain of the error amplifier $H_2(s)$, by increasing $C_z$ capacitor. However this will result in higher start-up time. A minimum start-up time of 111ms (corresponding to $C_z$=1.04uF) is required to yield a real value for $R_{gm}$ in order to meet the $V_{COMP}$ $2xf_{AC}$ ripple requirement.

Recalculating the compensation for soft-start time=111ms yields: Cz=1.04uF, Rgm=800ohms and Cp=54nF. The loop response plots can now be generated (Fig.13) and studied. The cross-over frequency and phase margin are 4.6Hz & 46° at 170VAC and 7.9Hz and 32° at 264VAC as seen in Fig.13 below.

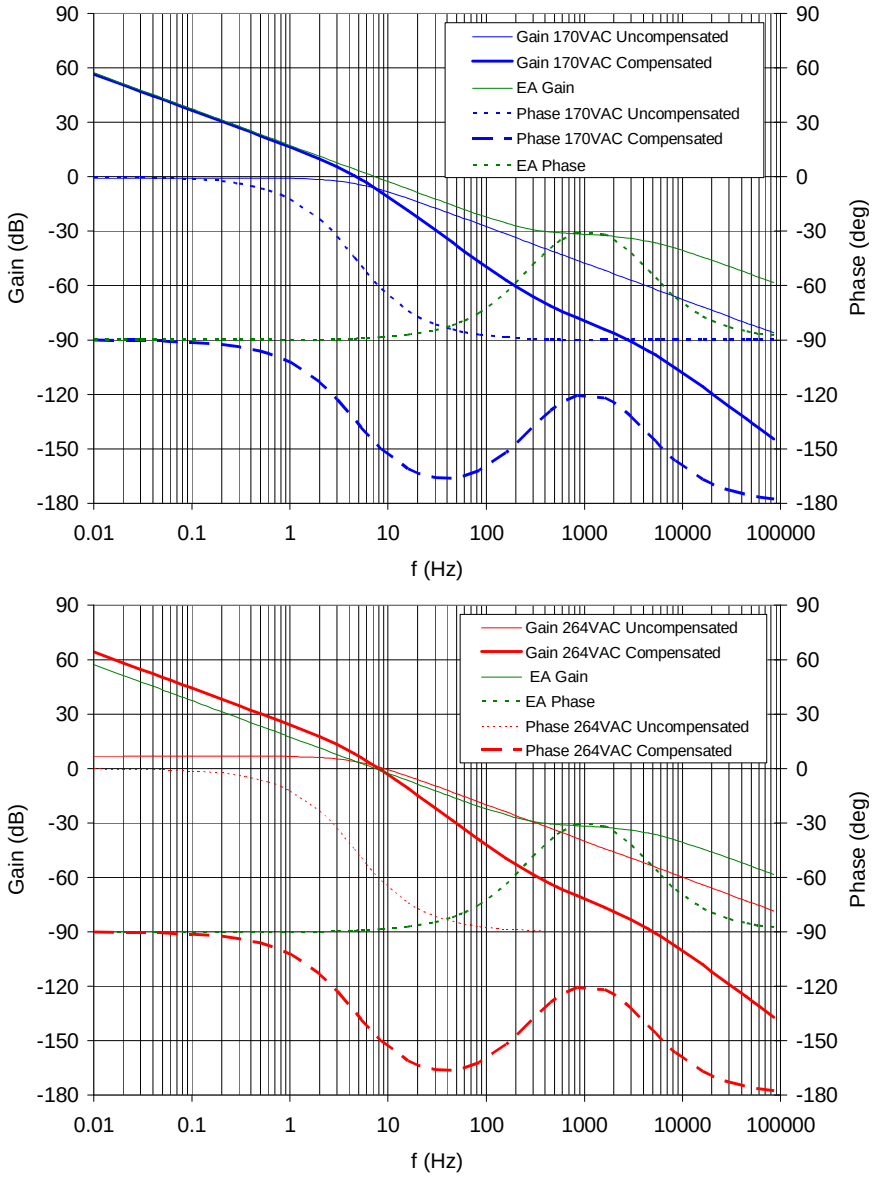


Fig.13: Overall Loop Gain at 170/264VAC, 2000W (reduced start-up time causes lower phase margin)

For more phase margin discussion and PCB layout guidelines, please refer to IR1152 application note AN-1150.

**References**

[1] IR1153S datasheet

[2] AN-1150 application note