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APPLICATION NOTE

Application Note AN-1166

Power Factor Correction using IR1155 CCM PFC IC

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Keywords: PFC, Power Factor Correction, THD.

1. Introduction

The IR1155 IC is a fixed frequency PFC IC designed to operate in continuous conduction mode Boost converters with average current mode control. The IC is packed with an impressive array of advanced features such as programmable switching frequency, programmable soft-start, micro-power startup current, user initiated micro-power Sleep mode for compliance with stand-by energy standards, ultra low bias currents for sensing pins. The switching frequency can be programmed from 48KHz to 200Khz. It has very low gate jitter thus eliminating audible noise in PFC magnetics. In addition, dedicated overvoltage protection, cycle-by-cycle peak current limit, open loop protection (OLP) and VCC under voltage lock-out (UVLO). All these features are offered in a compact 8-pin package making IR1155 the most feature-intensive IC for PFC applications. This application note provides an overview of the functionality of IR1155 and demonstrates the design of a universal input 300W AC-DC Boost PFC Converter.

2. IR1155 – Detailed Description

2.1 Overview of IR1155

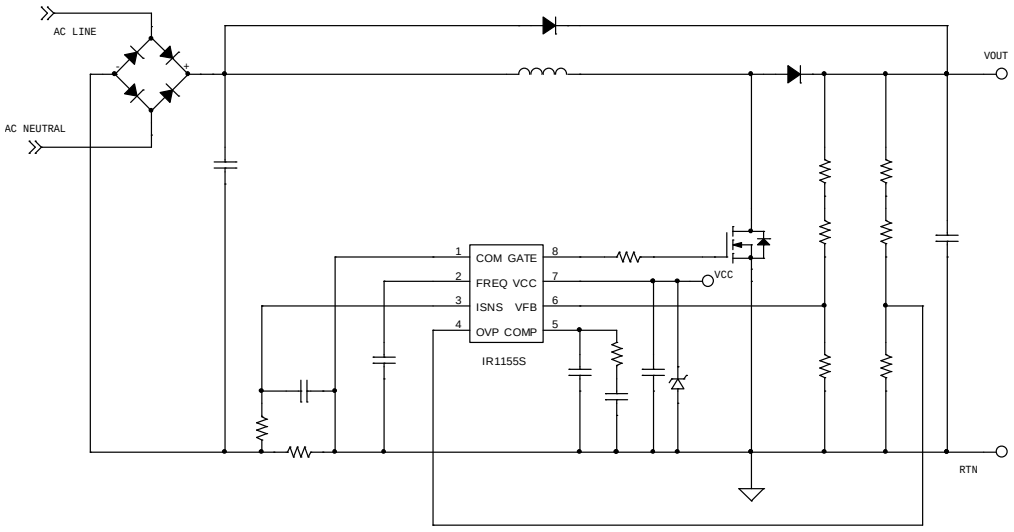

Fig.1: Typical application diagram of IR1155 based PFC converter

Fig.1 shows the system application diagram of the IR1155 based PFC converter. Only 3 pin functionalities - VFB, COMP & ISNS – are actually needed to obtain the necessary diagnostic signals to achieve power factor correction and maintain output voltage regulation. The functions of the abovementioned 3 pins are as follows:

- VFB – provides DC bus voltage sensing for voltage regulation

- COMP – used for compensating the voltage feedback loop to set the correct transient response characteristics
- ISNS – provides sensing of the inductor current, which is used to determine the PFC switch duty cycle

Essentially, there are 2 control loops in the PFC algorithm:

- a slow, outer voltage loop whose function is to simply maintain output voltage regulation
- a fast inner current loop whose function is to determine the instantaneous duty cycle every switching cycle

The current shaping function i.e. power factor correction is achieved primarily by the current loop. The voltage loop is responsible only for controlling the magnitude of the input current in order to maintain DC bus voltage regulation.

2.2 Key Features of IR1155

❖ *Programmable Oscillator*

The switching frequency of IR1155 is programmed by a capacitor (Cf) that connected to the FREQ pin. The switching frequency can be set from 48KHz to 200KHz with capacitor value from 430pF to 2nF. A 200uA constant current source $I_{OSC(CHG)}$ is used to charge the capacitor voltage from $V_{OSC\ VAL}$ (2V typ.) to $V_{OSC\ PK}$ (4V typ.). Once the voltage on Cf capacitor reaches 4V, the charging current is disconnected and a 6.6mA discharging current source $I_{OSC(DCHG)}$ is turned on to discharge Cf capacitor. When Cf voltage is discharged to 2V, the discharging current is discontinued and the charging current source will be turned on again. A sawtooth waveform is presented on FREQ pin as shown in Fig. 2.

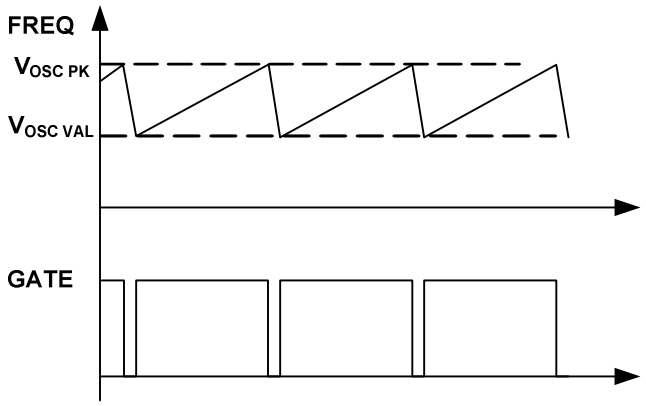

Fig.2. FREQ and GATE pin waveforms
(Gate pin demonstrates an example of maximum duty-cycle)

The rising slop of the sawtooth defines the maximum duty-cycle of GATE output, which is demonstrated in Fig.2. In system the actual duty in each switching cycle

is determined by the One Cycle Control modulator, and could vary from minimum 0% to maximum 96%~99%.

The relationship between Cf capacitor and the switching frequency can be found in Fig 3. Higher Cf value results in lower switching frequency.

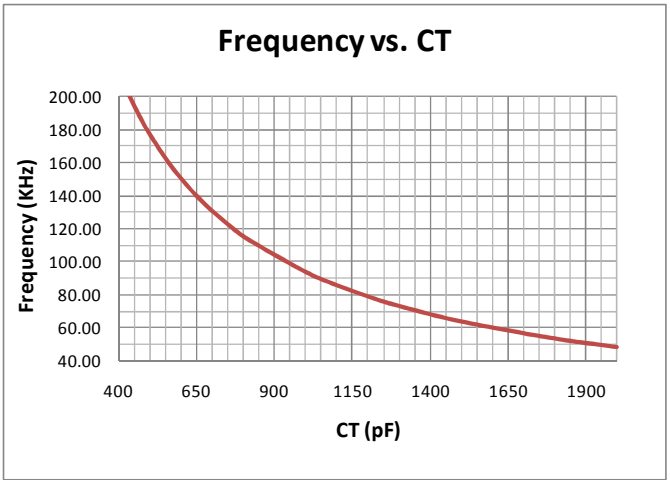

Fig.3: IR1155 Programmable Switching Frequency

Using capacitor to program frequency improves oscillator noise immunity. It also provides possibility to synchronize IR1155 with external clock. The clock should be a narrow pulse with 1%~5% duty-cycle. The duty-cycle of Sync pulse defines the dead-time of GATE output. 1% Sync duty-cycle results in 99% maximum PFC GATE output. Thus smaller Sync duty-cycle is preferred to achieve lower Total Harmonic Distortion (THD). However keep in mind that the minimum Clock pulse should longer than 100ns to guarantee a reliable operation. The amplitude of Sync signal should higher than $V_{OSC\ PK}$.

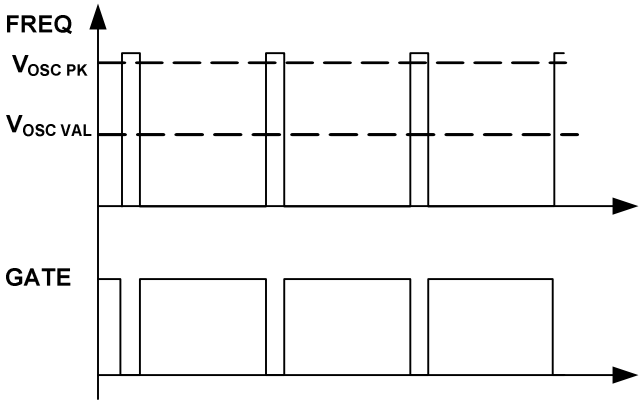

Fig.4. Sync IR1155 with Ext. signal
(Gate pin demonstrates an example of maximum duty-cycle)

❖ *Programmable soft-start*

IR1155 facilitates programmability of system soft-start time thus allowing the designer enough freedom to choose the converter start-up times appropriate for the application. The soft start time is the time required for the V_{COMP} voltage to charge through its entire dynamic range i.e. 0V through $V_{COMP,EFF}$. As a result, the soft-start time is dependent upon the component values selected for compensation of the voltage loop on the COMP pin – primarily the C_Z capacitor (described in detail in *Soft-Start Design* section of PFC Converter Design portion of this document). As VCOMP voltage rises gradually, the IC allows a higher and higher RMS current into the PFC converter. This controlled increase of the input current contributes to reducing system component stress during start-up. It is clarified that, during soft-start, the IC is capable of full duty cycle modulation (from 0% to MAX DUTY), based on the instantaneous ISNS signal from system current sensing. Furthermore, the internal logic of the IC is designed to ensure that the soft-start capacitor is discharged when the IC enters the Sleep or Stand-by modes in order to facilitate soft-start upon restart.

❖ *User initiated micro-power sleep mode*

The IR1155 has an ENABLE function embedded in the OVP/EN pin. When this pin voltage is actively pulled below V_{SLEEP} threshold, the IC is pushed into the Sleep mode where the current consumption is less than 200uA even when V_{CC} is above $V_{CC,ON}$ threshold. The system designer can use an external logic level signal to access the ENABLE feature since V_{SLEEP} threshold is so low. The IR1155 internal logic ensures that V_{COMP} is discharged before the IC enters Sleep mode in order to enable soft-start upon resumption of operation.

❖ *Protection features*

The IR1155 features a comprehensive array of protection features to safeguard the system. These are explained below.

1. Dedicated Overvoltage protection (OVP)

The OVP pin is a dedicated pin for overvoltage protection that safeguards the system even if there is a break in the VFB feedback loop due to resistor divider failure etc. An overvoltage fault is triggered when OVP pin voltage exceeds the V_{OVP} threshold of 106.5%V_{REF}. The IC gate drive is immediately disabled and held in that state. The overvoltage fault is removed and gate drive re-enabled only when both pin voltages are below the $V_{OVP,RST}$ threshold of 102.2% V_{REF}.

The overvoltage protection level can be programmed through external resistor divider.

2. Open-Loop protection (OLP)

The open-loop protection ensures that the IC is restrained in the Stand-by mode

if the VFB pin voltage has not exceeded or has dropped below V_{OLP} threshold of 19%V_{REF}. In the Stand-by mode, all internal circuitry of the IC are biased, the gate drive is disabled and current consumption is a few milliamps. During start-up, if for some reason the voltage feedback loop is open then IC will remain in Stand-by and not start thus avoiding a potentially catastrophic failure.

3. Cycle-by-cycle peak current limit protection (IPK LIMIT)

The cycle-by-cycle peak current limit is encountered when V_{ISNS} pin voltage exceeds $V_{ISNS(PK)}$ threshold of -0.77V (in magnitude). When this condition is encountered, the IC gate drive is immediately disabled and held in that state until the ISNS pin voltage falls below $V_{ISNS(PK)}$. Even though the IR1155 operates based on average current mode control, the input to the peak current limit comparator is decoupled from the averaging circuit thus enabling instantaneous cycle-by-cycle protection for peak current limitation.

4. V_{CC} UVLO

In the event that the voltage at the V_{CC} pin should drop below that of the VCC UVLO turn-off threshold, $V_{CC(UVLO)}$ the IC is pushed into the UVLO mode, the gate drive is terminated, and the turn on threshold, $V_{CC,\ ON}$ must again be exceeded in order to re start the process. In the UVLO mode, the current consumption is less than 175uA.

3. PFC Converter Design Procedure

3.1 PFC Converter Specifications

AC Input Voltage Range	85-264VAC
Input Line Frequency	47-63Hz
Nominal DC Output Voltage	388V
Maximum Output Power	300W
Power Factor	0.99 @ 115VAC/300W 0.99 @ 230VAC/300W
Minimum Output Holdup Time	20ms @ $V_{OUT,MIN}$=300V
Maximum Soft Start Time	40msec
Switching Frequency	100kHz
Over Voltage Protection	420V

Table 1: Design Specifications for PFC Converter

3.2 Power Circuit Design

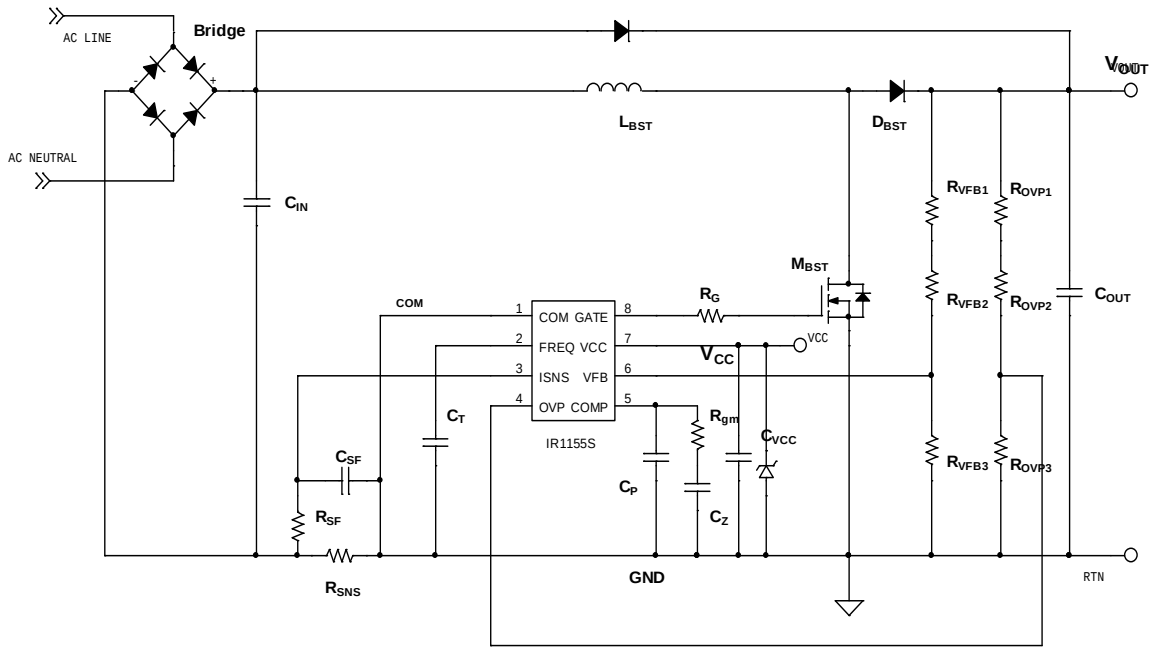

Fig.5: IR1155 based PFC Boost Converter

❖ *Peak Input Current*

It is necessary to determine the maximum input currents (RMS & peak) from the specifications in Table 1 before proceeding with detailed design of the PFC boost converter. The maximum input current is typically encountered at highest load & lowest input line situation (300W, 85VAC). Assuming a nominal efficiency of 92% at this situation, the maximum input power can be calculated:

$$P_{IN(MAX)} = \frac{P_{O(MAX)}}{\eta_{MIN}} = \frac{300W}{0.92} = 326W$$

From this, the maximum RMS AC line current is then calculated:

$$I_{IN(RMS)MAX} = \frac{P_{O(MAX)}}{\eta_{MIN}(V_{IN(RMS)MIN})PF}$$

$$I_{IN(RMS)MAX} = \frac{300W}{0.92(85V)0.998} = 3.84A$$

The selection of the semiconductor components (bridge rectifier, boost switch & boost diode) is based on $I_{IN(RMS)MAX}$ =3.84A.

Assuming a pure sinusoidal input, the maximum peak AC line current can then be calculated:

$$I_{IN(PK)MAX} = \frac{\sqrt{2}(P_{IN(MAX)})}{V_{IN(RMS)MIN}}$$

$$I_{IN(PK)MAX} = \frac{1.414(326W)}{85V} = 5.4A$$

❖ *Boost Inductance (L_{BST})*

IR1155 IC is an average current mode controller. An on-chip RC filter is sized to effectively filter the boost inductor current ripple to generate a clean average current signal for the IC. The averaging function in the IC can accommodate a maximum limit of 40% inductor current ripple factor at maximum input current. The boost inductance has to be sized so that the inductor ripple current factor is not more than 40% at maximum input current condition (at peak of AC sinusoid). This is because:

- Higher ripple current factors will interfere with the Average Current Mode operation of One Cycle Control algorithm in IR1155 leading to duty cycle instabilities and pulse skipping which results in current distortion and sometimes even audible noise
- power devices are stressed more with higher ripple currents as the peak inductor current ($I_{L(PK)MAX}$) also increases proportionately

In this calculation, an inductor current ripple factor of 20% is selected. The ripple current at peak of AC sinusoid at maximum input current is:

$$\Delta I_L = 0.2 \times I_{IN(PK)MAX}$$

$$\Delta I_L = 0.2 \times 5.4A = 1.1A$$

And, peak inductor current is:

$$I_{L(PK)MAX} = I_{IN(PK)MAX} + \frac{\Delta I_L}{2}$$

$$I_{L(PK)MAX} = 5.4A + \frac{1.1A}{2}$$

$$I_{L(PK)MAX} = 5.95A$$

In order to determine the boost inductance, the power switch duty cycle at peak of AC sinusoid (at lowest input line of 85VAC) is required.

$$V_{IN(PK)MIN} = \sqrt{2} \times V_{IN(RMS)MIN} = 120V$$

Based on the boost converter voltage conversion ratio,

$$D = \frac{V_O - V_{IN(PK)MIN}}{V_O}$$

$$D = \frac{388V - 120V}{388V} = 0.69$$

The boost inductance is then given by:

$$L_{BST} = \frac{V_{IN(PEAK)MIN} \times D}{f_{SW} \times \Delta I_L} = \frac{120V \times 0.69}{100kHz \times 1.1A}$$

$$L_{BST} = 754\mu H$$

A convenient value of 750µH is selected for L_{BST} for this converter.

❖ *High Frequency Input Capacitor (C_{IN})*

The purpose of the high-frequency capacitor is to supply the high-frequency component of the inductor current (the ripple component) via the shortest possible loop. This has the advantage of acting like an EMI filter, since it minimizes the high-frequency current requirement from the AC line. Typically a high-frequency, film type capacitor with low ESL and high-voltage rating (630V) is used.

High-frequency input capacitor design is essentially a trade-off between:

- sizing it big enough to minimize the noise injected back into the AC line
- sizing it small enough to avoid line current zero-crossing distortion (flattening)

The high-frequency input capacitor is determined as follows:

$$C_{IN} = k_{\Delta I_L} \frac{I_{IN(RMS)MAX}}{2\pi \times f_{SW} \times r \times V_{IN(RMS)MIN}}$$

$$C_{IN} = 0.2 \frac{3.84A}{2\pi \times 100kHz \times 0.06 \times 85V}$$

$$C_{IN} = 0.24\mu F$$

where:

$k_{\Delta IL}$ = inductor current ripple factor, of 20% as mentioned earlier

r = maximum high frequency input voltage ripple factor ($\Delta V_{IN}/V_{IN}$), assumed 6%

A standard 0.270µF, 630V capacitor is selected for C_{IN} for this converter.

❖ Output Capacitor (C_{OUT})

Output Capacitor design is based on hold-up time requirement

For 20ms hold-up time and minimum output voltage of 300V the output capacitance is first calculated:

$$C_{OUT(MIN)} = \frac{2 \cdot P_O \cdot \Delta t}{V_O{}^2 - V_{O(MIN)}{}^2}$$

$$C_{OUT(MIN)} = \frac{2 \cdot 300W \cdot 20ms}{(388V)^2 - (300V)^2}$$

$$C_{OUT(MIN)} = 198\mu F$$

Minimum capacitor value must be de-rated for capacitor tolerance (20%) to guarantee minimum hold-up time.

$$C_{OUT} = \frac{C_{OUT(MIN)}}{1 - \Delta C_{TOL}} = \frac{198\mu F}{1 - 0.2} = 248\mu F$$

A standard 270µF, 450V capacitor is selected for C_{OUT} for this converter.

3.3 IR1155 Control Circuit Design

3.3.1 Current Sense Resistor Design (ISNS pin)

In IR1155, there are two levels of current limitation:

- a "soft" current limit, which limits the duty-cycle and causes the DC bus voltage to fold-back i.e. droop
- a cycle-by-cycle "peak" current limit feature which immediately terminates gate drive pulse once the ISNS pin voltage exceeds $V_{ISNS,PEAK}$

❖ "Soft" Current Limit

In IR1155 the COMP pin voltage is directly proportional to the RMS input current into the PFC converter i.e. V_{COMP} is higher at higher RMS current. Clearly its magnitude is highest at maximum load P_{MAX} & minimum AC input voltage, $V_{IN,MIN}$. The dynamic range of V_{COMP} in the IC is defined by $V_{COMP,EFF}$ parameter in the IR1155 datasheet. Once V_{COMP} signal saturated (reaches $V_{COMP,EFF}$), any system requirement causing an additional increase in current will cause the IC to respond by limiting the duty cycle and thereby causing the output voltage to droop. This is called "soft" current limit protection. The selection of R_{SNS} must ensure that "soft" current limit is not encountered at any of the allowable line and load conditions.

❖ R_{SNS} Design

The design of R_{SNS} is performed at the system condition when the inductor current is highest at lowest input line ($V_{IN,MIN}$) and highest load (P_{MAX}). Further, the inductor current is highest at the peak of the AC sinusoid. The duty cycle required at peak of AC sinusoid at $V_{IN,MIN}$=85VAC in order to regulate V_{OUT}=388V is:

$$D_{PEAK} = \frac{V_{OUT} - \sqrt{2}V_{IN(RMS)MIN}}{V_{OUT}}$$

$$D_{PEAK} = \frac{388V - \sqrt{2}.85V}{385V} = 0.69$$

R_{SNS} design should guarantee that

i. PFC algorithm can deliver this duty cycle at peak of AC sinusoid at $V_{IN,MIN}$ & P_{MAX} condition
ii. soft current limit is encountered whenever there is a further increase in demand for current while operating at $V_{IN,MIN}$ & P_{MAX} condition

To do this, the V_{ISNS} is calculated below.

$$V_{ISNS(MAX)} = \frac{V_{COMP(EFF)(MIN)} \cdot (1-D)}{g_{DC}}$$

$$V_{ISNS(MAX)} = \frac{4.6V \cdot (1-0.69)}{3.1} = 0.46V$$

Note: if the calculated $V_{ISNS(MAX)}$ is higher than the cycle-by-cycle peak overcurrent limit threshold of the IC, the $V_{ISNS(PK)}$ value should be used to determine R_{SNS}. In this example, $V_{ISNS(MAX)}$ is lower than the minimum $V_{ISNS(PK)}$ value that specified in data sheet (0.69V), thus 0.47V is used for R_{SNS} calculation.

Next the peak inductor current at maximum peak AC line current, derated with an overload factor (K_{OVL}=5%), is calculated.

$$I_{IN(PK)OVL} = I_{L(PK)\max} \cdot (1 + K_{OVL})$$

$$I_{IN(PK)OVL} = 5.95 \times 1.05 = 6.25A$$

From this maximum current level and the required voltage on the current sense pin, we now calculate the maximum resistor value that can be used for the PFC converter.

$$R_{SNS,MAX} = \frac{V_{SNS(\max)}}{I_{IN(PK)OVL}} = \frac{0.46V}{6.25A}$$

$$R_{SNS,MAX} = 0.074\Omega$$

It is noted that even though IR1155 operates in average current mode it is still safer to use the peak inductor current for current sense resistor design to guarantee avoiding premature fold-back.

Power dissipation in the resistor is now calculated based on worst case RMS input current at minimum input voltage:

$$P_{R_S} = I_{IN(RMS)MAX}{}^2 \cdot R_S$$

$$P_{R_S} = 3.84^2 (0.074\Omega) = 1.09W$$

A standard 70mΩ resistor can be selected for R_{SNS} for the PFC converter.

❖ Peak Current Limit

The cycle-by-cycle peak current limit is encountered when V_{ISNS} pin voltage exceeds $V_{ISNS,PEAK}$. For the PFC converter, this limit is encountered whenever the inductor current exceeds the following:

$$I_{PK\_LMT} = \frac{|-.77V|}{0.07\Omega} = 11A$$

It is clarified that even though the IR1155 operates based on average current mode control, the input to the peak current limit comparator is decoupled from the averaging circuit thus enabling instantaneous cycle-by-cycle protection for peak overcurrent.

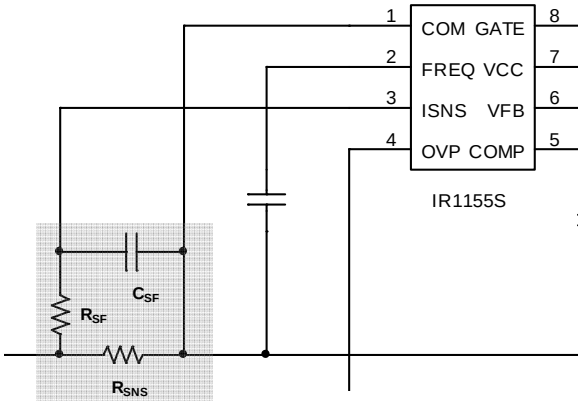

Fig 6: Current Sense Resistor and Filtering

The current sense signal is communicated to the ISNS pin of the IC using a current limiting series resistor, R_{SF}. An external RC filtering for ISNS pin can be realized (though not necessary for IR1155) by adding a filter capacitor, C_{SF} between the ISNS pin and COM as shown in Fig.6. A corner frequency around 1-1.5MHz will offer a safe compromise in terms of filtering, while maintaining the integrity of the current sense signal for cycle-by-cycle peak overcurrent protection.

$$f_{PSF} = \frac{1}{2\pi \cdot R_{SF} \cdot C_{SF}}$$

With R_{SF}=100Ω, we can use C_{SF}=1000pF to obtain a cross-over frequency of 1.6MHz. The input impedance of the current sense amplifier is approximately 25KΩ. The R_{SF} resistor will form a divider with this 25KΩ resistor. For R_{SF}=100Ω it is noted that the accuracy of the current sense voltage signal communicated to the IC is more than 99.5%.

3.3.2 Output Regulation Voltage Divider (VFB pin)

The output regulation voltage of the PFC converter is set by voltage divider on VFB pin - R_{FB1}, R_{FB2}, and R_{FB3}. The total impedance of this divider network must be high enough to reduce power dissipation, but low enough to keep the feedback voltage error (due to finite bias currents into the voltage error amplifier

which is less than 0.2uA) negligible. Around 2MΩ is an acceptable value for the total resistor divider impedance.

A standard 499kΩ, 1% tolerance resistor is selected for R_{FB1} & R_{FB2} for this converter. Then, R_{FB3} is determined based on error amplifier V_{REF} (Typ)=5V and V_{OUT}=388V converter specification.

$$R_{FB3} = \frac{V_{REF}(R_{FB1} + R_{FB2})}{(V_{out} - V_{REF})}$$

$$R_{FB3} = \frac{5.0V(499k \times 2)}{(388\text{V} - 5.0\text{V})} = 13.03k\Omega$$

A standard resistor, R_{FB3} = 13.0kΩ, 1% tolerance, is selected for this converter.

Power dissipation of divider resistors is given by the following.

$$P_{R_{FB1}} = P_{R_{FB2}} = \frac{(V_{out} - V_{REF})^2}{2(R_{FB1} + R_{FB2})}$$

$$P_{R_{FB1}} = P_{R_{FB2}} = \frac{(388V - 5V)^2}{2 \times 998k} = 73.5mW$$

3.3.3 Dedicated Overvoltage Protection Divider (OVP/EN pin)

IR1155 features a dedicated overvoltage sensing input pin (OVP/EN). User can use the same resistor divider that calculated earlier with FB control. This will give a fixed overvoltage protection level which is 106.5% of regulated output voltage. If a different overvoltage level is desired, a separated OVP resistor divider can be calculated. Here is an example:

Assume standard 499kΩ, 1% tolerance resistor is selected for R_{OVP1} & R_{OVP2} for this converter. The overvoltage protection threshold is 420V:

$$R_{OVP3} = \frac{1.065 \times V_{REF}(R_{OVP1} + R_{OVP2})}{(V_{OV} - 1.065 \times V_{REF})}$$

$$R_{FB3} = \frac{5.325V(998k)}{(420\text{V} - 5.325\text{V})} = 12.8k\Omega$$

The OVP reset point can be calculated:

$$V_{OVPREST} = \frac{1.022 \times V_{OV}}{1.065} = 403V$$

3.3.4 Timing Capacitor (FREQ pin)

The timing capacitor Cf can be obtained per the following formula:

$$C_f = \frac{(\frac{1}{Fsw} - 0.45us) \times 0.194mA}{2V}$$

For 100kHz target switching frequency, Cf is calculated 0.93nF. A standard 1nF capacitor will be used and it programs the switching frequency to 93kHz.

3.3.5 Voltage Loop Compensation (COMP pin)

The voltage feedback loop monitors the DC bus voltage (V_{OUT}) via the V_{FB} resistor divider whose transfer function is $H_1(s)$. Comparison of the V_{FB} pin voltage and internal reference voltage of the IC by voltage error amplifier yields a control signal (V_m = V_{COMP}-$V_{COMP,START}$). The transfer function of the error amplifier and compensation network is $H_2(s)$. The IR1155 output voltage error amplifier is a trans-conductance type amplifier and output of the error amplifier is connected to the COMP pin. The control signal directly controls the magnitude of the boost inductor current (I_L), which is also the input current of the PFC converter. The transfer function between I_L and control signal V_m is given by $H_3(s)$. The power stage of the PFC converter along with DC bus capacitor, maintains a constant voltage (V_{OUT}) at the converter output where the system load draws energy from the converter. The power stage + DC bus capacitor + system load transfer function is given by G(s). The small-signal model of the voltage feedback loop is depicted below in Fig.7. The overall loop gain transfer function *T(s)* is given by:

$$T(s) = H_1(s).H_2(s).H_3(s).G(s)$$

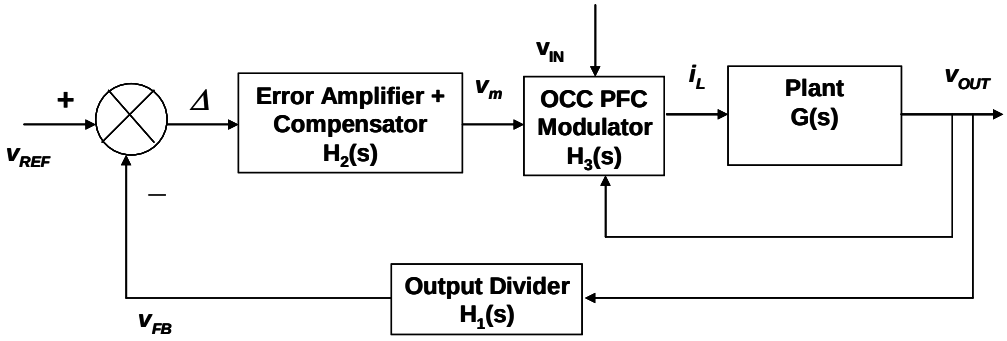

Fig.7: Small-signal modeling of the PFC voltage feedback loop

Voltage loop compensation is performed by adding R/C components between COMP and COM pins in order to:

i. Achieve the appropriate dynamic response characteristics during load/line fluctuations
ii. Ensure that the $2*f_{AC}$ ripple in V_{OUT} at steady state conditions, does not cause too much current distortion

In order to evaluate the overall loop gain transfer function *T(s)*, the small-signal transfer function of each of the blocks has to be evaluated first.

❖ Plant Gain, *G(s)*

The plant gain G(s) models the small signal variation in the DC bus voltage when a small perturbation occurs in the boost inductor current.

$$G(s) = v_{OUT}/i_L = (v_{OUT}/i_{CHG}).(i_{CHG}/i_L)$$

where the small signal parameters are italicized and i_L is the boost inductor current, v_{OUT} is the bus voltage and i_{CHG} is the current sourced at the output of the boost converter power stage (i.e. boost diode current).

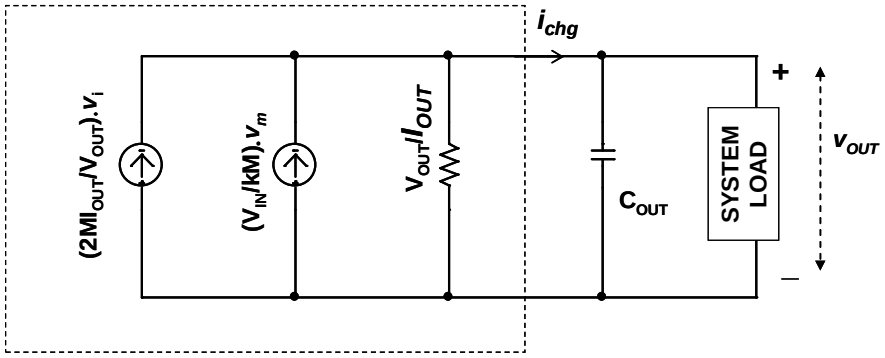

Fig.8: Small-signal model of PFC converter power stage

If the system load is a **Resistive Load**, then the shunt impedance and the system load are in parallel and equal in magnitude hence the equivalent impedance is $R_L/2$. In this case, the transfer function is:

$$\frac{v_{out}}{i_{chg}} = \frac{R_L/2}{1 + sC_{out}\frac{R_L}{2}}$$

In the power stage transfer function, this is represented by a pole:

$$f_{PS} = \frac{1}{2\pi \cdot C_{out}\frac{R_L}{2}}$$

For a **Constant Power Load**, the shunt impedance and the system load cancel each other out and the equivalent impedance is infinite, in which case the transfer function reduces to:

$$\frac{v_{out}}{i_{chg}} = \frac{1}{sC_{out}}$$

In the power stage transfer function, this is represented by a pole at the origin.

Under a **Constant Current Load**, since the impedance of a current source is infinitely high, the equivalent impedance is effectively just the shunt impedance:

$$\frac{v_{out}}{i_{chg}} = \frac{R_L}{1 + sC_{out}R_L}$$

In the power stage transfer function, this is represented by a pole:

$$f_{PS} = \frac{1}{2\pi \cdot C_{out}R_L}$$

Next *(i_{CHG}/i_L)* transfer function has to be evaluated. Assuming 100% efficiency, recognize that:

$$V_{IN}.I_L = V_{OUT}I_{OUT}$$

I_{OUT} is same as the DC component of the boost diode current (I_{CHG}). Hence

$$V_{IN}.I_L = V_{OUT}I_{CHG}$$

Applying linearization and small-signal analysis, for a given DC operating point defined by V_{IN} & V_{OUT} yields the relationship between i_{CHG} & i_L:

$$i_{CHG}/i_L = V_{IN}/V_{OUT}$$

Assuming a resistive load, the overall power stage transfer function can now be written as:

$$G(s) = \frac{V_{IN}}{V_{OUT}} \times \frac{R_L/2}{1 + sC_{out}\frac{R_L}{2}}$$

❖ OCC PFC Modulator, $H_3(s)$

In order to derive i_L/v_m, the One Cycle Control PWM modulator control law is employed:

$$G_{DC} \cdot R_S \cdot i_L = \frac{v_m}{M(d)}$$

where M(d) = V_{OUT}/V_{IN} for a given DC operating point defined by the DC bus voltage V_{OUT} and RMS input voltage V_{IN}. This ultimately yields

$$H_3(s) = \frac{i_L}{v_m} = \frac{V_{in}}{V_{OUT}R_S G_{DC}}$$

❖ Output voltage sensor Resistor-Divider, $H_1(s)$

The output divider scales the output voltage to be compared with the reference voltage in the error amplifier.

Therefore:

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2} + R_{FB3})V_{REF}}{R_{FB3}}$$

$$H_1(s) = \frac{V_{REF}}{V_{OUT}}$$

❖ Error Amplifier & Compensation, $H_2(S)$

The compensation scheme typically employed for a first-order, single-pole system aims to:

- add a pole at the origin in order to increase the low frequency gain and improve DC regulation
- add a low-frequency zero to boost phase margin near cross-over frequency and partially compensate the pole
- add a high-frequency pole to attenuate switching frequency noise and ripple effects

The above 3 requirements can be achieved in case of the transconductance type voltage error amplifier with the compensation scheme shown in Fig.9. However, as mentioned earlier, for the PFC converter, the most important criterion for basing the selection of the compensation component values is the voltage loop bandwidth.

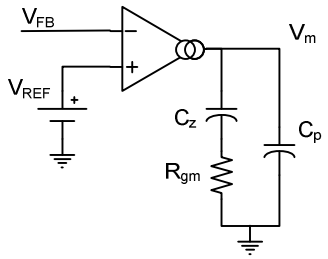

Fig9: Voltage Loop error amplifier compensation network

The error amplifier transfer function is given by:

$$H_2(s) = \frac{g_m \cdot (1 + sR_{gm}C_Z)}{s(C_Z + C_P + sR_{gm}C_ZC_P)}$$

where g_m is the transconductance of the voltage error amplifier. The compensation network adds a zero and a pole in the transfer function at:

$$f_{Z0} = \frac{1}{2\pi \cdot R_{gm} \cdot C_Z}$$

$$f_{P0} = \frac{1}{2\pi \cdot R_{gm} \frac{Cz \cdot Cp}{Cz + Cp}}$$

The gain and phase of the error amplifier + compensation transfer function is illustrated in Fig.10.

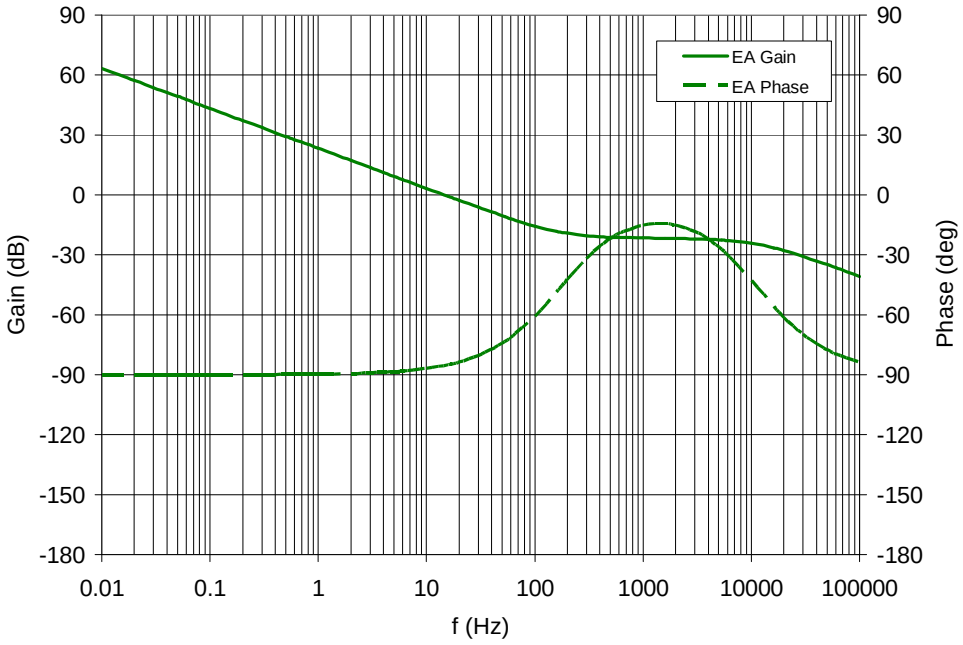

Fig.10: Error Amplifier + compensation transfer function characteristics

❖ Voltage Loop Compensation procedure

Step 1: Choose C_z based on soft-start time:

A soft-start time of 40ms is selected. Typical soft start values range from 20ms to a few hundred ms, depending upon the application. The soft-start time represents the time needed by the controller to ramp V_{COMP} from zero to the maximum value. The system will take no more than 40ms to achieve near-regulation.

$$C_Z = \frac{t_{SS} \cdot i_{OVEA}}{V_{COMP(EFF)}}$$

i_{OVEA} and $V_{COMP(EFF)}$ are taken from the datasheet.

$$C_Z = \frac{40ms \times 44\mu A}{4.9V} = 0.36\mu F$$

A standard value of 0.33uF can be selected for the converter for C_Z.

Step 2: Choose R_{gm} to ensure that $H_1(s).H_2(s)$ attenuation at $2xf_{AC}$ frequency is small enough to avoid current distortion:

The amount of $2xf_{AC}$ ripple on the output capacitor is calculated first. The minimum f_{AC} of 47Hz is considered here, since the ripple is the maximum at the lowest AC frequency. The peak-to-zero ripple V_{OPK} is given by:

$$V_{OPK} = \frac{P_{in,MAX}}{2\pi \cdot 2 \cdot f_{AC} \cdot C_O \cdot V_{out}}$$

$$V_{OPK} = \frac{326W}{2\pi \cdot 2 \cdot 47 \cdot 270\mu F \cdot 388V}$$

$$V_{OPK} = 5.27V$$

The peak-to-peak ripple in V_{OUT} is $2xV_{OPK}$. This ripple in V_{OUT} is reflected in the V_{COMP} voltage based on the attenuation provided by the resistor divider and error amplifier compensation network combined i.e. $H_1(s).H_2(s)$ at $2xf_{AC}$. The ripple in V_{COMP} i.e. ΔV_{COMP} has to be small compared with the value of the error amplifier output voltage swing ($V_{COMP,EFF}$). Typical values for $\Delta V_{COMP}/V_{COMP}$ range from 0.5% to 1%. 0.5% is recommended if current shaping has to be excellent while 1% is recommended for higher phase margin and low-oscillation response to load steps. 1% attenuation demands a (G_{VA}) of:

$$G_{VA} = \frac{V_{COMP(EFF)} \cdot 0.01}{2 \cdot V_{OPK}}$$

$$G_{VA} = \frac{4.9V \times 0.01}{2 \times 5.27V} = 0.00465$$

$$G_{VA} = -46.7dB$$

This is the required attenuation in $H_1(s).H_2(s)$ at $2xf_{AC}$ frequency.

$H_1(s)$, given by $V_{REF}/V_{OUT,}$ is next calculated:

$$H_1 = \frac{5V}{388V} = 0.0129 = -37.8dB$$

The required attenuation from $H_2(s)$ alone at 2x47Hz is then given by:

$$G_{VA} - H_1 = -8.9dB = 0.36$$

Since the error amplifier pole will be set at a much higher frequency than $2xf_{AC}$ (and consequently $C_z >> C_p$), the error amplifier transfer function at $2xf_{AC}$ can be approximated to:

$$H_2(s) \cong \frac{g_m \cdot (1 + sR_{gm}C_Z)}{sC_Z}$$

Since C_Z has already been determined, only R_{gm} needs to be calculated by forcing:

$$\left|H_2(j2\pi \cdot f_{AC})\right| = G_{VA} - H_1 = -8.9dB = 0.36$$

$$R_{gm} = \sqrt{\left(\frac{G_{VA} - H_1}{g_m}\right)^2 - \left(\frac{1}{2\pi \cdot 2 \cdot f_{AC} \cdot C_Z}\right)^2}$$

Substituting f_{AC}=47Hz, g_m=50µS, C_Z=0.33µF yields

$$R_{gm} = 5.1k\Omega$$

The location of the zero in the compensation scheme can now be estimated:

$f_z = 1/(2*\pi*R_{gm}.C_z) = 1/(2*\pi*5.1kohm*0.33\mu F) = 95Hz$

The location of the pole in the power stage transfer function (assuming a resistive load) is:

$f_{PS} = 1/(2*\pi*C_{OUT}*R_L/2) = 1/[2*\pi*270uF*(388V*388V/300W)/2] = 2.3Hz$

Step 3: Choose Cp based on high-frequency pole location

The pole frequency should be chosen higher than the cross over frequency and significantly lower than the switching frequency in order to attenuate switching noise and switching frequency ripple in the output capacitor: typical value is 1/6 to 1/10 of the switching frequency. Choosing $1/6xf_{SW}$ (=0.166*100kHz=16kHz) for this converter:

$$f_{P0} = \frac{1}{2\pi \cdot R_{gm} \frac{Cz \cdot Cp}{Cz + Cp}} \cong \frac{1}{2\pi \cdot R_{gm} \cdot Cp}$$

$$C_p = \frac{1}{2\pi \cdot 5.1k\Omega \cdot 100kHz \cdot 0.166} = 1.88nF$$

Step 4: Estimate bandwidth & phase margin

The voltage loop response for 85VAC and 264VAC is plotted at full output power condition of 300W in Fig.11. At 85VAC/350W the cross-over frequency is 5Hz and phase margin is about 33°. At 264VAC/350W the cross-over frequency is 16Hz and phase margin is about 23°. This result satisfies the cross-over frequency and phase margin requirements of the design.

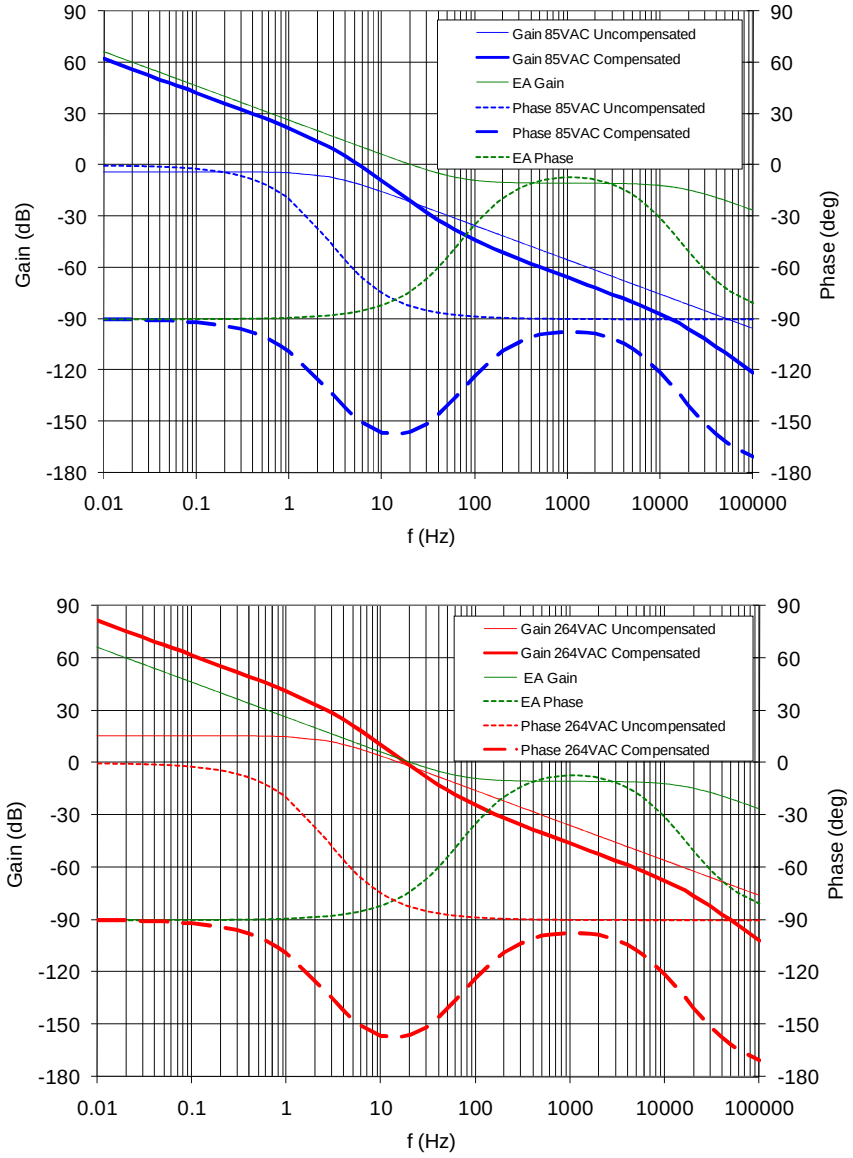

Fig.11: Overall Loop Gain at 85/264VAC & 300W (fast loop + low phase margin)

For more phase margin discussion and PCB layout guidelines, please refer to IR1152 application note AN-1150.

References

[1] IR1155S datasheet

[2] AN-1150 application note