Application Note AN-1160

Design of Resonant Half-Bridge converter using IRS2795(1,2) Control IC

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1. Introduction and Device Overview

The IRS2795(1,2) is a self oscillating half-bridge driver IC for resonant half-bridge DC-DC converter applications for use up to 600V. It has a fixed 50% duty-cycle and very wide operating frequency range. The maximum switching frequency can go up to 500kHz. The frequency can be programmed externally through the RT and CT pins. The IC offers flexibility to program the minimum operating frequency, the maximum operating frequency and the frequency sweep at power up for the soft-start function.

The dead time is programmed by the CT capacitor. The programmable dead-time allows the user to optimize the system with the minimum body-diode conduction time for higher efficiency under full load, while keeping ZVS switching under no load condition.

The IC offers over current protection using the on-state resistance of the low-side MOSFET. The protection threshold is 2V for IRS27951 and it is 3V for IRS27952 IC.

The IC can be disabled by externally pulling the voltage at the CT/SD pin below its enable voltage threshold. The IC enters “sleep” mode and only consumes micro-power when disabled.

IRS2795(1,2) packing in a 8-pin package, it’s easy to use, and drastically reduces external component count for a high efficiency low cost power supply.

**Figure 1** is the typical application schematic of IRS2795(1,2):
The pinout of IRS2795(1,2) is shown below.

<table>
<thead>
<tr>
<th>Lead Assignment</th>
<th>Pin#</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>VB</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>2</td>
<td>RT</td>
<td>HO</td>
<td>Oscillator timing resistor</td>
</tr>
<tr>
<td>3</td>
<td>CT/SD</td>
<td>VS</td>
<td>Oscillator timing capacitor/Shutdown</td>
</tr>
<tr>
<td>4</td>
<td>COM</td>
<td>LO</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>LO</td>
<td></td>
<td>Low-side gate drive</td>
</tr>
<tr>
<td>6</td>
<td>VS</td>
<td></td>
<td>High-side gate drive return/ HV Current Sense</td>
</tr>
<tr>
<td>7</td>
<td>HO</td>
<td></td>
<td>High-side gate drive</td>
</tr>
<tr>
<td>8</td>
<td>VB</td>
<td></td>
<td>High-side floating supply voltage</td>
</tr>
</tbody>
</table>

Figure 2: IRS2795(1,2) IC pin assignment

2. LLC Resonant Half-Bridge Converter Operation

The increasing popularity of the LLC resonant converter in its half-bridge implementation is due to its high efficiency, low switching noise and ability to achieve high power density. This topology is also the most attractive topology for front-end DC bus conversion. It utilizes the magnetizing inductance of the transformer to construct a complex resonant tank with Buck Boost transfer characteristics in the soft-switching region. The typical power stage schematic for this topology is shown below.

![Typical schematic of a DC-DC half-bridge resonant converter](image)

Figure 3: Typical schematic of a DC-DC half-bridge resonant converter

Devices M1 and M2 operate at 50% duty cycle and the output voltage is regulated by varying the switching frequency of the converter. The converter has two resonant frequencies – a lower resonant frequency (given by $L_m$, $L_r$, $C_r$ and the load) and a fixed higher series resonant frequency $F_{r1}$ (given by $L_r$ and $C_r$ only). The two bridge devices M1 and M2 can be soft-switched for the entire
load range by operating the converter under inductive load mode (ZVS region). It can be either above or below the resonant frequency $F_{r1}$.

The typical AC transfer characteristics\(^1\) for a LLC tank resonant converter are shown in Figure 4. The group of curve indicates the gain under different load conditions.

![Figure 4: Typical frequency response of a LLC resonant converter](image)

The characteristics of a LLC resonant converter can be divided into three regions based on the 3 different modes of operation.

The first region is for switching frequency above the resonant frequency $F_{r1}$.

$$F_{r1} = \frac{1}{2\pi \sqrt{L_r \cdot C_r}}$$

In region ① (the purple shaded area) the switching frequency is higher than resonant frequency $F_{r1}$. The converter operation is very similar to a series resonant converter. Here $L_m$ never resonates with resonant capacitor $C_r$; it is clamped by the output voltage and acts as the load of the series resonant tank. This is the inductive load region and the converter is always under ZVS operation regardless of the load condition.

In the 2\(\text{nd}\) region, the switching frequency is higher than the lower resonant frequency but lower than $F_{r1}$. Region ② is in the pink shaded area in Figure 4. The lower resonant frequency varies with load, so the boundary of region ② and region ③ traces the peak of the family load vs. gain curves. In this complex region, the LLC resonant operation can be divided into two time intervals. In the first time interval, $L_r$ resonates with $C_r$ and $L_m$ is clamped by output voltage. When the current in the resonant

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\(^1\) For this AC analysis, only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to output. The transformer, rectifier and filter are replaced by an equivalent AC resistance, $R_{ac}$. 

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inductor \(L_r\) resonates back to the same level as the magnetizing current, \(L_r\) and \(C_r\) stop resonating. \(L_m\) now participates in the resonant operation and the second time interval begins. During this time interval, dominate resonant components change to \(C_r\) and \(L_m\) in series with \(L_r\). The ZVS operation in region 2 is guarantees by operating the converter to the right side of the load gain curve. For a switching frequency below resonant \(F_{r1}\), it could falls in either region 2 or region 3 depends on the load condition.

In the ZCS range 3 below \(f_{r1}\), the LLC resonant converter operates in capacitive mode; M1 and M2 are under hard switching and have high switching losses. So ZCS operation should always be avoided.

The typical operating waveforms of the 3 modes are demonstrated in Figure 5 to Figure 7.

![Figure 5: Typical waveform of above resonant ZVS switching](image)

![Figure 6: Typical waveform of below resonant ZVS switching](image)
The waveforms indicate that the current in secondary rectifier diodes moves from continuous current mode (CCM) to discontinuous current mode (DCM) when the switching frequency varies from above resonant ZVS to below resonant ZVS due to load increasing. The ripple voltage on the resonant capacitor \( C_r \) also increases in the below resonant ZVS mode.

**Figure 7:** Typical waveform of below resonant ZCS switching

In ZCS mode, the two switching devices M1 and M2 are turned off under zero current condition. The turn-on of the two switches is hard switching (none ZVS). The turn-on switching loss is high especially under high voltage bus voltage. The resonant capacitor \( C_r \) also has high voltage stress. ZCS operation should always be avoided.

The typical voltage conversion ratio of a LLC resonant converter is shown in **Figure 8**.

**Figure 8:** Typical voltage conversion ratio of a LLC resonant converter
With a fixed input voltage, the converter varies switching frequency to regulate the output voltage over load range – keeping the same conversion ratio over the family of curves with different Q.

Given a fixed load condition, the converter varies switching frequency along that load line to regulate output voltage over input voltage range – the conversion ratio increases when input voltage decreases.

To design the LLC resonant half-bridge converter, we use the First Harmonic Approximation (FHA) to get equivalent circuit. All the components are put to primary side to simply the analysis. The load equals to a resistor $R_{ac}$ that is in parallel with transformer primary inductance $L_m$.

![Diagram of LLC resonant half-bridge converter](image)

**Figure 9:** The FHA equivalent circuit

The input voltage of the resonant tank is a square wave with amplitude equals to the input DC voltage $V_{in}$. The fundamental component of the square waveform is:

$$\frac{2 \cdot V_{in}}{\pi} \sin(\sigma \cdot t)$$

The output voltage of the resonant tank is the voltage across $L_m$. It is very close to a square waveform with amplitude swinging from $-n \cdot V_{out}$ to $+n \cdot V_{out}$. So the fundamental component of the output square waveform is:

$$\frac{4 \cdot n \cdot V_{out}}{\pi} \sin(\sigma \cdot t)$$
The power dissipation on the equivalent AC resistor is equal to the power dissipation of $R_{LOAD}$ resistor, thus it can be written as:

$$\frac{V_{out}^2}{R_{LOAD}} = \left(\frac{4 \cdot n \cdot V_{out}}{\sqrt{2\pi}}\right)^2 \frac{1}{R_{ac}}$$

Rearrange the formula and get the equivalent AC resistor:

$$R_{ac} = \frac{8 \cdot n^2}{\pi^2} R_{LOAD}$$

The transfer ratio of the equivalent circuit can be obtained as following:

$$M = \left| \begin{array}{c} \frac{j \omega L_m R_{ac}}{j \omega L_m + R_{ac}} \\ \frac{j \omega L_r + \frac{1}{j \omega C_r} + \frac{j \omega L_m R_{ac}}{j \omega L_m + R_{ac}}}{1 + \frac{1}{\omega^2 L_m C_r} + \frac{j \omega L_r}{R_{ac}} - \frac{j}{\omega C_r R_{ac}}} \end{array} \right|$$

Re-write the formula,

$$M = \left| \begin{array}{c} 1 \\ 1 + \frac{L_r}{L_m} - \frac{1}{\omega^2 L_m C_r} + \frac{j \omega L_r}{R_{ac}} - \frac{j}{\omega C_r R_{ac}} \end{array} \right|$$

With the following definitions, M can be simplified.

$$F_{r1} = \frac{1}{2\pi \sqrt{L_r \cdot C_r}}, \quad x = \frac{F_{SW}}{F_{r1}}, \quad \sigma = 2\pi F_{SW} = 2\pi \cdot x \cdot F_{r1} = \frac{x}{\sqrt{L_r \cdot C_r}},$$

$$k = \frac{L_m}{L_r}, \quad R_{ac} = \frac{8 \cdot n^2 \cdot R_{LOAD}}{\pi^2}, \quad Q = \frac{2\pi F_{r1} \cdot L_r}{R_{ac}} = \frac{1}{2\pi F_{r1} \cdot C_r \cdot R_{ac}}$$

$$M = \left| \begin{array}{c} 1 \right| \frac{1}{1 + \frac{1}{k} \left(1 - \frac{1}{x^2}\right) + jQ \left(x - \frac{1}{x}\right)}$$

Or,

$$M = \frac{1}{\sqrt{\left[1 + \frac{1}{k} \left(1 - \frac{1}{x^2}\right)\right]^2 + [Q \left(x - \frac{1}{x}\right)]^2}}$$
Per Figure 9, M is also equals to the output voltage to input voltage ratio:

\[ M = \frac{n \cdot \text{Vout} \cdot \frac{4}{\pi}}{\frac{2 \cdot \text{Vin}}{\pi}} = \frac{\text{Vout}}{\text{Vin}} \cdot \frac{2}{n} \]

So we have the conversion ratio of output voltage Vout to input voltage Vin:

\[ \frac{\text{Vout}}{\text{Vin}} = \frac{M}{2 \cdot n} \]

3. Transformer and Resonant Circuit Design

This section provides the details of how to calculate the key components of a LLC converter, take a 24V output 240W power supply as an example.

The system input data

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin(_{\text{max}})</td>
<td>V</td>
<td>The maximum DC bus voltage</td>
<td>430</td>
</tr>
<tr>
<td>Vin(_{\text{min}})</td>
<td>V</td>
<td>The minimum DC bus voltage</td>
<td>350</td>
</tr>
<tr>
<td>Vin(_{\text{nom}})</td>
<td>V</td>
<td>The nominal DC bus voltage</td>
<td>390</td>
</tr>
<tr>
<td>Vout</td>
<td>V</td>
<td>The DC output voltage</td>
<td>24</td>
</tr>
<tr>
<td>Iout</td>
<td>A</td>
<td>The output load current</td>
<td>10</td>
</tr>
<tr>
<td>Fr(_{1})</td>
<td>KHz</td>
<td>The resonant frequency</td>
<td>100</td>
</tr>
<tr>
<td>Fmax</td>
<td>KHz</td>
<td>The maximum switching frequency</td>
<td>150</td>
</tr>
<tr>
<td>Dmax</td>
<td></td>
<td>The maximum duty-cycle</td>
<td>0.5</td>
</tr>
<tr>
<td>Tss</td>
<td>ms</td>
<td>The soft start time</td>
<td>10</td>
</tr>
<tr>
<td>Fss</td>
<td>KHz</td>
<td>The soft start frequency</td>
<td>300</td>
</tr>
<tr>
<td>Transformer</td>
<td></td>
<td></td>
<td>ETD49</td>
</tr>
</tbody>
</table>

Note: Typically set Fmax < 2xF\(_{r1}\) as the parasitic capacitance in the system introduced a 3rd resonant frequency which could cause the output voltage to increase with switching frequency at no load if the maximum switching frequency is higher than the limit.

Step 1: Calculate the transformer turns ratio

\[ n = \frac{\text{Vin}_{\text{max}}}{2 \cdot \text{Vout}} \]

\[ n = \frac{430}{2 \cdot 24} = 8.96 \]

The transformer turns ratio is calculated with the maximum input voltage to make sure the output is always under regulation, including the worst case - high-line voltage and no load condition.
Usually the transfer ratio of the power stage is higher than the theoretical calculated value. This is because of the parasitic capacitance in the system (the coupling capacitor between transformer windings and the junction capacitors of output diodes) affects the resonance, especially at zero load where the switching frequency is much higher than the resonant frequency. So it’s recommended to choose the \( n \) to be slightly higher than the calculated value especially if the controller has no burst mode to keep regulation at high line and zero load condition.

\[ n = 9 \]

**Step 2: Choose \( k \) value**

\( k \) is the ratio between the transformer magnetic inductance and the resonant inductance. Smaller \( k \) value gives steeper Gain curve, especially at the below resonant ZVS region as shown in Figure 10. The output voltage is more sensitive to frequency variation with smaller \( k \) factor.

![Figure 10: \( k \) factor](image)

A higher \( k \) value results in higher magnetic inductance and thus lower magnetizing current in the transformer primary winding – that means lower circulating power losses. However, higher magnetic inductance could also cause non-ZVS switching at high line and zero load condition where the circulating current is too small to fully charge / discharge the VS node during dead-time.

The recommend range of \( k \) is from 3 to 10. Here \( k = 5 \) is chosen.

**Step 3: Calculate \( Q_{\text{max}} \) to stay in ZVS operation at the maximum load under the minimum input voltage**

The input impedance of the equivalent resonant circuit (Figure 9) is given by:
To keep the converter working in soft switching mode, the operating point should always in the ZVS region as shown in Figure 4. The ZVS ZCS boundary line is defined by the phase angle of \( \Phi(Zin) = 0 \) (the boundary condition between capacitive and inductive load), i.e. the imaginary part of \( Zin \) is zero. With this condition we can calculate the maximum \( Q \) which allows the converter to stay in ZVS. The maximum \( Q \) happens at the minimum input voltage and the maximum load.

\[
\begin{align*}
Q_{\text{max}} &= \frac{1}{k} \sqrt{\frac{1 + k \left(1 - \frac{1}{M_{\text{max}}^2}\right)}{M_{\text{max}}^2 - 1}} \\
&= \frac{1}{k} \sqrt{\frac{1 + k \left(1 - \frac{1}{M_{\text{max}}^2}\right)}{M_{\text{max}}^2 - 1}} \cdot \frac{1}{2n \left(\frac{V_{\text{out}}}{V_{\text{in}} - V_{\text{min}}}\right)^2} - 1
\end{align*}
\]

Where \( M_{\text{max}} \) is the maximum conversion ratio at the minimum input voltage,

\[ Q_{\text{max}} = 0.456 \]

**Step 4: Calculate the minimum switching frequency**

The minimum switching frequency happens at the maximum load and minimum input voltage with the previous calculated maximum \( Q_{\text{max}} \). As \( Q_{\text{max}} \) is defined by \( \text{Im}(Zin) = 0 \),

\[
\begin{align*}
\left(\frac{x - 1}{x} + \frac{xk}{1 + k^2 \cdot x^2 \cdot Q_{\text{max}}^2}\right) &= 0
\end{align*}
\]

The \( F_{\text{min}} \) can be calculated with:

\[
\begin{align*}
x_{\text{min}} &= \frac{1}{\sqrt{1 + k \left(1 - \frac{1}{M_{\text{max}}^2}\right)}} = \sqrt{\frac{1}{1 + k \left(1 - \frac{1}{M_{\text{max}}^2}\right)}} \\
&= \sqrt{\frac{1}{1 + k \left(1 - \frac{1}{M_{\text{max}}^2}\right)}} \cdot \frac{1}{2n \left(\frac{V_{\text{out}}}{V_{\text{in}} - V_{\text{min}}}\right)^2} - 1
\end{align*}
\]

\[ x_{\text{min}} = 0.607 \]

\[ F_{\text{min}} = x_{\text{min}} \cdot F_{r_1} = 60.7 kHz \]

**Step 5: Calculate \( L_r, C_r \) and \( L_m \)**

As \( Q_{\text{max}} \) happens at the maximum load, so the resonant components \( L_r, C_r \) and \( L_m \) can be calculated per the \( Q_{\text{max}} \) value that had obtained in step 3:
\[ R_{\text{LOAD}} = \frac{V_{\text{out}}}{I_{\text{out}}} = \frac{24V}{10A} = 2.4\Omega \]

\[ R_{\text{ac}} = \frac{8 \cdot n^2 \cdot R_{\text{LOAD}}}{\pi^2} = \frac{8 \times 9^2 \times 2.4}{\pi^2} = 157.57\Omega \]

\[ L_r = \frac{Q_{\text{max}} \cdot R_{\text{ac}}}{2 \cdot \pi \cdot F_{r1}} = \frac{0.456 \times 157.57}{2 \cdot \pi \cdot 100K} = 114uH \]

\[ C_r = \frac{1}{2 \cdot \pi \cdot F_{r1} \cdot Q_{\text{max}} \cdot R_{\text{ac}}} = \frac{1}{2 \cdot \pi \cdot 100K \times 0.456 \times 157.57} = 22.2nF \]

Choose the nearest standard capacitor value for \( C_r \), \( C_r = 22nF \)

Recalculate \( F_{r1} \) to keep the same \( Q_{\text{max}} \) with the selected \( C_r \) capacitor.

\[ F_{r1} = \frac{1}{2 \cdot \pi \cdot C_r \cdot Q_{\text{max}} \cdot R_{\text{ac}}} = 100.7Khz \]

Recalculate \( L_r \) with the selected \( C_r \) and \( F_{r1} \).

\[ L_r = \frac{Q_{\text{max}} \cdot R_{\text{ac}}}{2 \cdot \pi \cdot F_{r1}} = 113uH \]

The actual \( L_r \) value should be lower than the calculated value to stay in ZVS region.

Now calculate \( L_m \) value based on \( L_r \) and the \( k \) factor that preset in step 2:

\[ L_m = L_r \cdot k = 113 \times 5 = 565uH \]

Please note that \( L_m \) is the magnetizing inductance of the transformer. The total primary inductance value \( L_p \) is the sum of \( L_m \) and \( L_r \).

\[ L_p = L_m + L_r = 678uH \]

To simplify the power stage, the resonant inductor can be integrated into the power transformer by using slotted bobbin, also called two-section or two-chamber bobbin. By separate the primary winding and the secondary winding in the two chambers, the coupling between primary and secondary is much worse than the single section bobbin. Thus the leakage inductance is high and can be used as resonant inductor. The component count is lower and the copper loss is also smaller. Figure 11 is the picture of a two-section bobbin.

Figure 11: 2-section Transformer
When measure the inductance of a transformer, the primary inductance $L_p$ is measured with all secondary windings opened. And the leakage inductance is measured with all the secondary windings shorted.

**Step 6: Calculate transformer primary and secondary turns**

The standard half-bridge equation for the transformer turns number calculation is used here:

$$N_p = \frac{Vin \text{ min} \cdot D \text{ max}}{2 \cdot \Delta B \cdot Ae \cdot F \text{ min}}$$

With $\Delta B = 0.2T$, $Ae = 2.11cm^2$ (ETD49), $F \text{ min} = 60KHz$, $Vin \text{ min} = 350V$, $D \text{ max} = 0.5$

$$N_p = \frac{350 \cdot 0.5}{2 \cdot 0.2 \cdot 2.11 \cdot 60} \times 10 = 35$$

$$N_s = \frac{N_p}{n} = \frac{35}{9} = 3.89$$

The number of turns must be an integer and should be higher than the calculated value, so choose $N_s = 4$

Then recalculate $N_p$:

$$N_p = N_s \cdot n = 4 \times 9 = 36$$

**Step 7: Calculate transformer primary and secondary current**

Most LLC converters design the minimum switching frequency to be below the resonant frequency $F_{r1}$, in order to maintain output voltage regulation at low line and full load. When the switching frequency is lower than the resonant frequency $F_{r1}$, the current waveform is shown as in **Figure 12**.

![Figure 12: Transformer primary current at full load and minimum input voltage](image)

$I_1$ is the current where the resonant current in $L_r$ meets the magnetizing current in $L_m$. This is also the point where $C_r$ and $L_r$ finish resonance for the first half-period of $F_{r1}$. At this point, there is no more energy delivered to the load and the output diodes are off. The $C_r$ starts to resonate with $L_r + L_m$ until the switching MOSFETs change states. $I_1$ can be calculated as:
The peak and RMS value of primary current can be estimated as:

\[ I_{pri}(pk) = \sqrt{\left(\frac{I_{out} \cdot \pi}{2 \cdot n}\right)^2 + I_1^2} = 1.99\,A \]

\[ I_{pri\,RMS} = \frac{I_{pri}(pk)}{\sqrt{2}} = 1.4\,A \]

The RMS current is calculated by assuming pure sinusoid current waveform. So the actual primary RMS current is higher than the calculated value.

The current in each secondary winding is very close to half-sinusoid, thus the peak and RMS current can be estimated by:

\[ I_{spk} = \frac{I_{out} \cdot \pi}{2} = 15.7\,A \]

\[ I_{srms} = \frac{I_{out} \cdot \pi}{4} = 7.85\,A \]

The wire gauge of primary and secondary windings should be selected properly according to the calculated RMS current.

**Step 8: Calculate resonant capacitor voltage**

The \( C_r \) waveform is shown as in **Figure 13**: 

**Figure 13**: Typical resonant tank voltage and current waveforms

\( I_{L_m} \) is the magnetizing current of transformer primary, not including the current which is delivered to the secondary load through an ideal transformer in parallel with \( L_m \). The difference between \( I_{L_r} \) and \( I_{L_m} \) is the output current.
The VC\textsubscript{r} voltage reaches its peak when L\textsubscript{r} current is crossing zero and it is at the mid of input voltage when L\textsubscript{r} current reached its peak. The C\textsubscript{r} voltage is at the maximum value when VS node is zero and it is at the minimum value when VS node is equals to Vin. So VC\textsubscript{rmin} and VC\textsubscript{rmax} can be calculated as:

\[
VC_{r_{\text{max}}} = n \cdot Vout + Ipri(pk) \times \sqrt{\frac{L_r}{C_r}}
\]

\[
VC_{r_{\text{min}}} = Vin - n \cdot Vout - Ipri(pk) \times \sqrt{\frac{L_r}{C_r}}
\]

The peak to peak voltage ripple of VC\textsubscript{r} is VC\textsubscript{r_{pk}} - VC\textsubscript{r_{pk}}.

\[
VC_{r_{pk}} = 2n \cdot Vout + 2 \cdot Ipri(pk) \times \sqrt{\frac{L_r}{C_r}} - Vin
\]

It can be seen that the maximum peak-to-peak voltage happens at the maximum load and the minimum DC input Vin\textsubscript{min}, the switching frequency is at the minimum F\textsubscript{min}.

In this example:

\[
V_{cr_{pk}} = 2 \times 9 \times 24V + 2 \times 1.99A \times \sqrt{\frac{113uH}{22nF}} - 350V = 368V
\]

The resonant capacitor C\textsubscript{r} can be selected according to the capacitance value, together with its voltage and current rating. Polypropylene film capacitor is preferred to use for lower power loss. Please note the polypropylene film capacitor is rated under DC voltage or 50Hz AC voltage and has voltage derating at high frequency and high ambient temperature. The ability of withstanding high frequency voltage is limited by thermal (power dissipation) and peak current capability. Usually the derating starts at 85~90C ambient and is not a concern. But a capacitor with higher voltage rating
should be chosen if the ambient temperature is higher than 85°C. Below is an example of EPCOS MKP capacitor B32621 (630Vdc/400Vac).

![Graph showing Vrms vs. frequency curve of MKP capacitor B32621 @ Ta<=90°C](image)

**Figure 15:** Vrms vs. frequency curve of MKP capacitor B32621 @ Ta<=90°C

### 4. IRS2795 Passive Components Design

**Step 9: Calculate the minimum dead-time to keep ZVS switching at zero load at the maximum input voltage**

For resonant half-bridge converter, the switching frequency goes to the maximum under no load at the maximum input voltage. Theoretically when the switching frequency is above the resonant frequency Fr1, the operation is ZVS switching. However, above resonance is only one of the necessary conditions for ZVS. The other condition is the equivalent parasitic capacitor of the half-bridge midpoint (junction capacitor of VS node) to be fully (dis-)charged within the dead-time period. **Figure 16** demonstrates if the dead-time is not sufficient, the turn-on of the MOSFET has hard-switching even though the converter is working under the below resonant ZVS mode.
Figure 16: ZVS and none-ZVS waveform of region 2 operation

To keep the converter always working under ZVS condition, it is necessary to calculate the minimum time that required to fully (dis-)charging the VS equivalent capacitor during the two switches interleaving period (dead-time).

As the equivalent capacitor is (dis-)charged by the circulating current in the transformer primary winding, so the worst case happens at the maximum input voltage and zero load condition where the transformer current is at minimum. At zero load, there is no current transfer to the secondary side and the current in the tank is just the magnetizing current of transformer. In each half-cycle, it is a linear straight line as shown in Figure 17.

Figure 17: Transformer primary current at zero load

So the primary current under this condition can be calculated as:

\[
I'_{pri}(pk) = \frac{n \cdot V_{out}}{4F \max \cdot (L_r + L_m)}
\]

\[
I'_{pri}(pk) = 0.53A
\]
The total equivalent junction capacitor $C_{HB}$ of VS node is shown in Figure 18.

![Figure 18: VS Equivalent junction capacitor](image)

$$C_{HB} = 2 \cdot C_{oss\_eff} + C_{rss\_eff} + C_{well} + C_s$$

It includes:

- The effective $C_{oss}$ of the two MOSFETs (both high-side and low-side);
  - The $C_{oss\_eff}$ as defined in the MOSFET datasheet is the effective capacitance of MOSFET that gives the same charging time as a fixed capacitor while $V_{DS}$ is rising from 0 to 80% of $V_{DS}$. So the $C_{oss\_eff}$ of a 500V MOSFET is defined under 0 to 400V $V_{DS}$ which fits to this application.

- The effective $C_{rss}$ of the low-side MOSFET;
  - The $C_{rss}$ of MOSFET is typically defined at $V_{DS}=25V$. The $C_{rss}$ capacitance value reduces as $V_{DS}$ voltage increasing. So the effective $C_{rss}$ can be chose as $\frac{1}{2}$ or $\frac{1}{3}$ of $C_{rss}$.

- The stray capacitance $C_{well}$ of IRS2795(1,2);
  - The stray capacitance of IRS2795(1,2) is the high-side well capacitance of the 600V driver. The value of the stray capacitor is around 5pF.

- The snubber capacitor $C_s$ (if any) that is connected to the VS node.

For example, the $C_{oss\_eff}$ of MOSFET STF13NM50N is 110pF, $C_{rss}$ is 5pF, and there is no snubber capacitor to the VS node, the (dis-)charging time of VS node can be calculated as:

$$C_{oss\_eff} = 110\, pF, \quad C_{rss\_eff} = 2.5\, pF, \quad C_{well} = 5\, pF, \quad C_s = 0\, pF$$

$$T_{ch} = \frac{C_{HB} \cdot V_{in\, max}}{I'\, pri\, (pk)}$$

$$T_{ch} = 185\, ns$$

The dead-time calculation should also include the gate driver falling time. The MOSFET turn-off timing diagram is shown in Figure 19, which using LO and M2 as an example. In the first time interval $t_1$, gate voltage discharges to a plateau voltage $V'\, m$, and both $V_{DS}$ voltage and $I_D$ current...
stay unchanged in t1. As long as MOSFET gate voltage reaches the miller plateau V’m, miller cap Cgd is discharged and VDS voltage starts increasing. Due to the nonlinearity of Coss capacitor, VDS voltage increase slowly at the beginning, then the slope becomes steeper at higher VDS voltage. The miller plateau is the flat portion of gate driver curve. It varies with drain current. MOSFET turns off at a relative low current level in LLC application, the miller plateau is very close to the gate turn off threshold Vgs(th).

The timing that is interested for the dead time calculation is t1, as the charging time of the VS node (i.e. VDS of M2) starting from t2 is already included in the Tch calculation. In t1, VDS voltage is 0V, and MOSFET gate equals to a constant capacitor load to the IC. So the discharge time t1 can be calculated based on the RC time constant of the gate drive loop.

\[
t_1 = -RC_{eq} \ln \frac{V’m}{V_G}
\]

Where, 
\[
R = R_{down \_eff} + R_g + R_{gFET}
\]

\[
C_{eq} = \frac{(Q_g - Q_{gd} - Q_{gs})}{Vgs - Vm}, \text{ Please refer to Figure 21.}
\]

\[
V’m \approx Vgs(th)
\]

\[
V_G = Vcc, \text{ IRS2795(1,2) gate output voltage is clamped to Vcc voltage}
\]

R_{down \_eff} : IRS2795(1,2) gate driver effective pull down resistance (6Ω)
R_g is the external MOSFET gate drive resistor
R_{gFET}: MOSFET gate input resistance

Figure 19: MOSFET turn-off equivalent circuit and timing diagram

STF13NM50 gate equivalent capacitor is 2.32nF, MOSFET internal gate resistor is 5Ω, Vgs(th) is 3V. Thus if Vcc=15V, Rg=10Ω, gate discharge time t1 is:

\[
t_1 = 78.4ns
\]

The dead-time should be longer than the sum of Tch and t1. For experience, it is recommended to add 50ns to the calculated value. The minimum dead-time TDT is then given by:

\[
T_{DT} = Tch + t_1 + 50ns = 313ns
\]

For most of the design, it’s not recommended to have a dead-time that is longer than 1us, as longer dead-time leads to higher body-diode power losses at full load. So if the calculated dead-time is too long, go back to step 2 and choose a smaller k value.

Once the system parameters are defined, the passive components around the IRS2795(1,2) as shown in Figure 20 can be calculated.
Calculate \( R_{ss} \) with the desired soft-start frequency:

\[
R_{ss} = \frac{RT \cdot Rsseq}{RT - Rsseq}
\]

Calculate \( C_{ss} \) based on the desired soft-start time:

\[
C_{ss} = \frac{T_{ss}}{3 \cdot R_{ss}}
\]

In sleep mode or fault mode, RT pin is discharged to 0V. A diode Dss is put in parallel with Rsseq to fast discharge Css when IC is shutdown or in fault mode. This is to make sure the system still has soft start when IRS2795(1,2) restarts quickly. Dss can be any general purpose low voltage (10V) and low current (100mA) diode.

The bootstrap capacitor \( C_{bs} \) is used to hold \( V_{bs} \) supply voltage for the high-side driver. The value of \( C_{bs} \) is recommended to be 100nF to 220nF. Bigger \( C_{bs} \) capacitor causes higher charging current.
during startup and should be avoided. IRS2795(1,2) doesn’t have integrated bootstrap MOSFET. A 600V/1A fast recovery diode is required for bootstrap.

5. IRS2795 Power Loss Calculation

5.1 Low voltage static loss that caused by quiescent current

\[ P_{d1} = V_{cc} \times I_{qcc} \]

where \( I_{qcc} \) is 2.5mA maximum per IRS2795(1,2) datasheet.

5.2 The gate driver power losses

The gate driver losses of IRS2795(1,2) are the losses when driving the two external MOSFETs M1 and M2. In ZVS mode, MOSFET \( V_{DS} \) voltage is 0V prior to the gate turns on, so the “Miller” charge \( Q_{gd} \) should be subtracted from the total gate charge. Further, at ZVS operation, the MOSFET is as a constant capacitor load to the driver. The equivalent capacitor value equals to the \( C_{gs}+C_{gd} \) at \( V_{DS}=0V \) condition, which can be obtained from the gate charge curve in a MOSFET data sheet. It is indeed the slope factor of the gate charge curve where \( V_{GS} \) is above the miller plateau voltage \( V_m \).

\[ C_{seq} = \frac{(Q_{g} - Q_{gd} - Q_{gs})}{V_{gs} - V_m} \]

Typically the \( Q_g, Q_{gd} \) and \( Q_{gs} \) value are specified under 10V \( V_{GS} \) voltage, \( V_m \) is the flat portion voltage of the gate charge curve. For example, STF13NM50 \( Q_g=30nC, Q_{gd}=15nC, Q_{gs}=5nC, V_m=5.7V \), its gate equivalent capacitor in ZVS is 2.32nF.

The total gate charge in ZVS mode is proportional to the gate voltage:

\[ Q_{gz} = C_{geq} \cdot V_g \]

Figure 21: MOSFET gate charge curve and equivalent gate capacitance at ZVS mode
IRS2795(1,2) gate output voltage is clamped to Vcc voltage. So the total gate driver losses of both high-side and low-side can be calculated by:

\[
P_{dr} = P_{dr1} + P_{dr2} = 2 \cdot C_{geq} \cdot Vcc^2 \cdot F_{sw}
\]

The total gate driver losses are dissipated in driver IC IRS2795(1,2) and the external gate driver resistor including the MOSFET internal gate resistor. The power loss in IRS2795(1,2) is proportional to the resistor divider value:

\[
P_{d2} = \frac{R_{up\_eff}}{R_{up\_eff} + R_g + R_{FET}} + \frac{R_{down\_eff}}{R_{down\_eff} + R_g + R_{FET}} \times \frac{P_{dr}}{2}
\]

Where,
- \(R_g\): is the external MOSFET gate drive resistor
- \(R_{up\_eff}\): IRS2795(1,2) gate driver effective pull up resistance (40Ω)
- \(R_{down\_eff}\): IRS2795(1,2) gate driver effective pull down resistance (6Ω)
- \(R_{FET}\): MOSFET gate input resistance

The gate driver pull-up and pull-down resistance used for power loss calculation are given below: \(R_{up} = 40Ω, R_{down} = 6Ω\). They are bigger than datasheet specification (with is defined under 20mA current) as they are the equivalent pull-up and pull-down resistance under high gate current.

### 5.3 The CMOS switching losses

The switching loss in low voltage logic circuit is proportional to the switching frequency and supply voltage Vcc:

\[
P_{d3} = Vcc \times F_{sw} \times Q_{cmos}
\]

For IRS2795(1,2),

\[
Q_{cmos} = 6nC \sim 10nC
\]

### 5.4 The high voltage switching losses

The switching losses in high voltage level-shift circuit:

\[
P_{d4} = (Vcc + Vin) \times F_{sw} \times Q_p
\]

Vin is the input bus voltage. Qp is the charge absorbed by the level shifter. For IRS2795(1,2), Qp is 2nC under 300V to 430V bus voltage.

### 5.5 An example of power loss calculation

The total power loss in IRS2795(1,2) is the sum of Pd1 to Pd4.

\[
P_{d\_total} = P_{d1} + P_{d2} + P_{d3} + P_{d4}
\]

An example of power loss calculation with Vcc=15V, maximum switching frequency =150KHz, MOSFETs =STF13NM50N, input bus voltage = 400V, external gate resistor = 10ohm:

\[
P_{d1} = 37.5mW
\]

\[
P_{dr} = 157mW, P_{d2} = 79.5mW
\]

\[
P_{d3} = 18mW
\]

\[
P_{d4} = 124.5mW
\]

\[
P_{d\_total} = 259.5mW
\]
It can be seen that the high voltage switching loss $P_{d4}$ and gate driver loss $P_{d2}$ are the main source of total power losses. $P_{d4}$ is proportional to switching frequency and HV bus voltage. For 400V DC BUS voltage, IRS2795(1,2) can directly drives big MOSFETs ($C_{geq} \leq 4.7\text{nF}$) up to 250KHz switching frequency. It is necessary to clamp the Vcc supply voltage to 15V or lower to reduce gate driver losses when the frequency goes to 300KHz while driving big MOSFETs. For 300KHz to 500KHz switching frequency and 400V applications, it is recommended to use external driver.

IC operation current $I_{cc}$ can be obtained by the total low-voltage power loss and Vcc voltage:

$$I_{cc} = \frac{(P_{d1} + P_{dr} + P_{d3})}{V_{cc}}$$

6. MOSFET Selection Guide

The power MOSFET should be selected per the breakdown voltage and $R_{D\text{SON}}$ value. In addition, the body diode reverse recovery characteristic also plays important role to the selection. The converter usually has a few switching cycles that is under hard switching at the beginning of startup. This is because the resonant capacitor and output capacitors are fully discharged. In this case, longer reverse recovery time could cause shoot through between the two MOSFETs. Thus a MOSFET with fast reverse recovery diode is preferred.

As the resonant half-bridge has ZVS switching, the turn-on loss is negligible. If not switching under very high frequency ($\leq 150$KHz), the major power loss in MOSFET comes from the conduction loss. The maximum conduction loss can be calculated as:

$$P_{con} = I_{qrms}^2 \times R_{dson@Tj}$$

Where $I_{qrms} = \frac{I_{p_{pri}}(pk)}{2}$, and $R_{dson@Tj}$ is the MOSFET on-state resistance at the system maximum allowable junction temperature.

The calculation of the turn-off loss of MOSFET is complicated due to none linearity of $C_{oss}$ under different VDS voltage. Thus we use the estimated formula:

$$P_{off} = C_{IB} \times V_{in}^2 \times F_{sw} \times \frac{24}{2}$$

The total power loss in each MOSFET equals to $P_{con} + P_{off}$.

IRS2795(1,2) uses the $R_{dson}$ of low side MOSFET for current sensing and over current protection. The product family provides two choices on different over current protection level: the OCP threshold of IRS27951 is 2V and IRS27952 is 3V. Typically the IRS27951 is good for oversized MOSFET where a lower $R_{dson}$ for better efficiency and the IRS27952 is good for cost effective MOSFET where the $R_{dson}$ is bigger. A quick estimation for OCP threshold is to use 2.5 to 3 times of the maximum drain current times the $R_{dson}$ of MOSFET.

At startup, the MOSFET current could be a few times higher than the normal working current. To prevent false triggering of over current protection when using large $R_{dson}$ MOSFET, it is recommended to extend the soft-start time to tens of milliseconds.
7. Operating Waveforms and Efficiency of the Reference Design

The specification of the reference design:

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<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value</th>
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<td>$V_{\text{in}_{\text{min}}}$</td>
<td>The minimum DC bus voltage</td>
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<td>$I_{\text{out}_1}$</td>
<td>The output load current</td>
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<tr>
<td>$V_{\text{out}_2}$</td>
<td>The DC output voltage</td>
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<tr>
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<td>The maximum switching frequency</td>
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Design analysis result:

<table>
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<tr>
<th>Component</th>
<th>Details</th>
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<tbody>
<tr>
<td>Resonant tank components</td>
<td>$C_r=22\text{nF}, L_r=125\text{uH}, L_m=500\text{uH}, k=4$</td>
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<tr>
<td>Transformer</td>
<td>$N_p=36, N_{24\text{V}}=4, N_{12\text{V}}=2, n=9$</td>
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<td>IRS27951 components</td>
<td>$C_T=390\text{pF}, R_T=18\text{k}, R_{\text{max}}=14\text{k}, R_{\text{ss}}=3.9\text{k}, C_{\text{ss}}=3.3\text{uF}$</td>
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</table>
7.1 Schematic

Figure 22 – IRS27951 Reference Design Schematic

The reference board has input rectifier and filter, so it can take either DC or AC input. The DC input range is 350V~430V, the AC input voltage range is 250Vac~300Vac. The dummy loads at 24V and 12V output are for cross-regulation purpose.
## 7.2 BOM

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<td>1206 SMD Film RED 1/4W 1%</td>
<td>3</td>
<td>270k</td>
<td>DIGIKEY</td>
<td>RHM270KFCCT-ND</td>
</tr>
<tr>
<td>RT</td>
<td>1206 SMD Film RED 1/4W 1%</td>
<td>1</td>
<td>18k</td>
<td>DIGIKEY</td>
<td>RHM18.0KFCCT-ND</td>
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<tr>
<td>RVcc</td>
<td>1206 SMD Film RED 1/4W 5%</td>
<td>1</td>
<td>65</td>
<td>DIGIKEY</td>
<td>RHM65ERCCT-ND</td>
</tr>
<tr>
<td>Rx1, Rx2</td>
<td>1206 SMD Film RED 1/4W 5%</td>
<td>2</td>
<td>4.7</td>
<td>DIGIKEY</td>
<td>RHM4.7KFCCT-ND</td>
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<tr>
<td>TX</td>
<td>Resonant Power Transformer</td>
<td>1</td>
<td></td>
<td>DIGIKEY</td>
<td>ETD49</td>
</tr>
<tr>
<td>U1</td>
<td>IRS2751 Control IC</td>
<td>1</td>
<td></td>
<td>IR</td>
<td>IRS2751S</td>
</tr>
<tr>
<td>U2</td>
<td>Photocoupler TRANS-OUT 4-DIP</td>
<td>1</td>
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<td>DIGIKEY</td>
<td>TLP621</td>
</tr>
<tr>
<td>U3</td>
<td>Programmable Voltage Regulator SOT23-3</td>
<td>1</td>
<td></td>
<td>DIGIKEY</td>
<td>TL431</td>
</tr>
<tr>
<td>W1</td>
<td>Jumper for Primary Current Sensing Loop</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
7.3 Typical Operating Waveforms

Figure 23 – 400Vdc input, 0W load startup

Figure 24 - 400Vdc input, 220W load startup

Figure 25 - 400Vdc input, 220W load operation
Figure 26 – 350Vdc input, 220W load operation

Figure 27 – 420Vdc input, 220W load operation

Figure 28 – 420Vdc input, 0W load operation
7.4 Short circuit protection

Figure 29 – 260Vac input, short 12V, IC latched shut down

7.5 Efficiency

The average efficiency of the board at 25%, 50%, 75% and 100% load is 92% at 270Vac input:

<table>
<thead>
<tr>
<th>24Vout</th>
<th>24V Iout(A)</th>
<th>12Vout</th>
<th>12V Iout(A)</th>
<th>Pout(W)</th>
<th>270Vac Efficiency</th>
<th>400Vdc Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>24.176</td>
<td>1.5</td>
<td>11.97</td>
<td>1.5</td>
<td>54.2</td>
<td>90.8%</td>
<td>91.0%</td>
</tr>
<tr>
<td>24.2</td>
<td>3</td>
<td>11.92</td>
<td>3</td>
<td>108.4</td>
<td>92.6%</td>
<td>92.6%</td>
</tr>
<tr>
<td>24.22</td>
<td>4.5</td>
<td>11.9</td>
<td>4.5</td>
<td>162.5</td>
<td>92.4%</td>
<td>92.9%</td>
</tr>
<tr>
<td>24.24</td>
<td>6</td>
<td>11.86</td>
<td>6</td>
<td>216.6</td>
<td>92.2%</td>
<td>92.7%</td>
</tr>
<tr>
<td>23.517</td>
<td>6</td>
<td>12.26</td>
<td>0</td>
<td>141.1</td>
<td>92.8%</td>
<td></td>
</tr>
<tr>
<td>24.814</td>
<td>0</td>
<td>11.63</td>
<td>6</td>
<td>69.8</td>
<td>89.5%</td>
<td></td>
</tr>
</tbody>
</table>
8. Layout guidelines and example

- **Ground Plane:**
  In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

- **Gate Drive Loops:**
  Current loops behave like antennas and are able to receive and transmit EM noise. In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. For the low-side driver, the return of the drive loop must be directly connected to the COM pin of the IC and separate with signal ground (power ground and signal ground have star connection at COM pin).

- **Supply Capacitor:**
  It is recommended to place a bypass capacitor (CVCC) between the VCC and COM pins. A 1µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

- **CBS Capacitor:**
  The CBS capacitor should be placed as close as possible to the VB and VS pins.

- **Routing and Placement:**
  1) The 8-pin IC has only one COM pin for both signal return and power return, so it is strongly recommended to route the signal ground and power ground separately with a star connection at the COM pin.
2) The RT pin provides a current reference for the internal oscillator and needs to be kept as clean as possible to avoid frequency jittering or duty-cycle mismatch between high-side and low-side. The components connected to this pin must keep away from the high frequency switching loop such as the gate driver loop and the VS node. The PCB traces connected to RT pin also need to be kept away from any switching node.

3) Connect CT capacitor directly to COM pin, don’t share the return with any other signal ground.

- **Layout examples**

![Layout examples](image)

**Figure 31:** Single layer board example

9. Appendix

**Symbols list**

- \( L_r \): primary resonant inductance. It is the primary leakage inductance of transformer when there is no external added resonant inductor.
- \( L_m \): transformer primary magnetic inductance. It is the measured transformer primary inductance minus the leakage inductance.
- \( C_r \): primary resonant capacitor and DC blocking capacitor
- \( f_{r1} \): the resonant frequency between \( L_r \) and \( C_r \)
- \( \text{Rac} \): Equivalent AC resistance for resonant tank AC analysis
- \( R_{\text{DSon}} \): MOSFET channel ON resistance
\( f_{\text{max}} \): converter maximum operating switching frequency
\( f_{\text{min}} \): converter minimum operating switching frequency
\( Q_g \): MOSFET total gate charge
\( Q_{gd} \): MOSFET gate to drain (Miller) charge
\( Q_{gs} \): MOSFET gate to source charge
\( I_{\text{QCC}} \): IRS2795(1,2) quiescent current
\( R_g \): MOSFET gate drive resistance external to IRS2795(1,2)
\( R_{up} \): IRS2795(1,2) gate driver pull up resistance
\( R_{down} \): IRS2795(1,2) gate driver pull down resistance
\( R_{gFET} \): MOSFET gate input resistance
\( P_{\text{ICmax}} \): IRS2795(1,2) maximum power dissipation
\( V_{\text{CC}} \): Supply voltage on IRS2795(1,2) Vcc pin
\( I_{\text{CC}} \): IRS2795(1,2) IC supply current

References
[1] IRS2795(1,2) datasheet