Application Note AN-1160

Design of Resonant Half-Bridge converter using IRS2795(1,2) Control IC

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1. Introduction and Device Overview

The IRS2795(1,2) is a self oscillating half-bridge driver IC for resonant half-bridge DC-DC converter applications for use up to 600V. It has a fixed 50% duty-cycle and very wide operating frequency range. The maximum switching frequency can go up to 500kHz. The frequency can be programmed externally through the RT and CT pins. The IC offers flexibility to program the minimum operating frequency, the maximum operating frequency and the frequency sweep at power up for the soft-start function.

The dead time is programmed by the CT capacitor. The programmable dead-time allows the user to optimize the system with the minimum body-diode conduction time for higher efficiency under full load, while keeping ZVS switching under no load condition.

The IC offers over current protection using the on-state resistance of the low-side MOSFET. The protection threshold is 2V for IRS27951 and it is 3V for IRS27952 IC.

The IC can be disabled by externally pulling the voltage at the CT/SD pin below its enable voltage threshold. The IC enters “sleep” mode and only consumes micro-power when disabled.

IRS2795(1,2) packing in a 8-pin package, it’s easy to use, and drastically reduces external component count for a high efficiency low cost power supply.

Figure 1 is the typical application schematic of IRS2795(1,2):

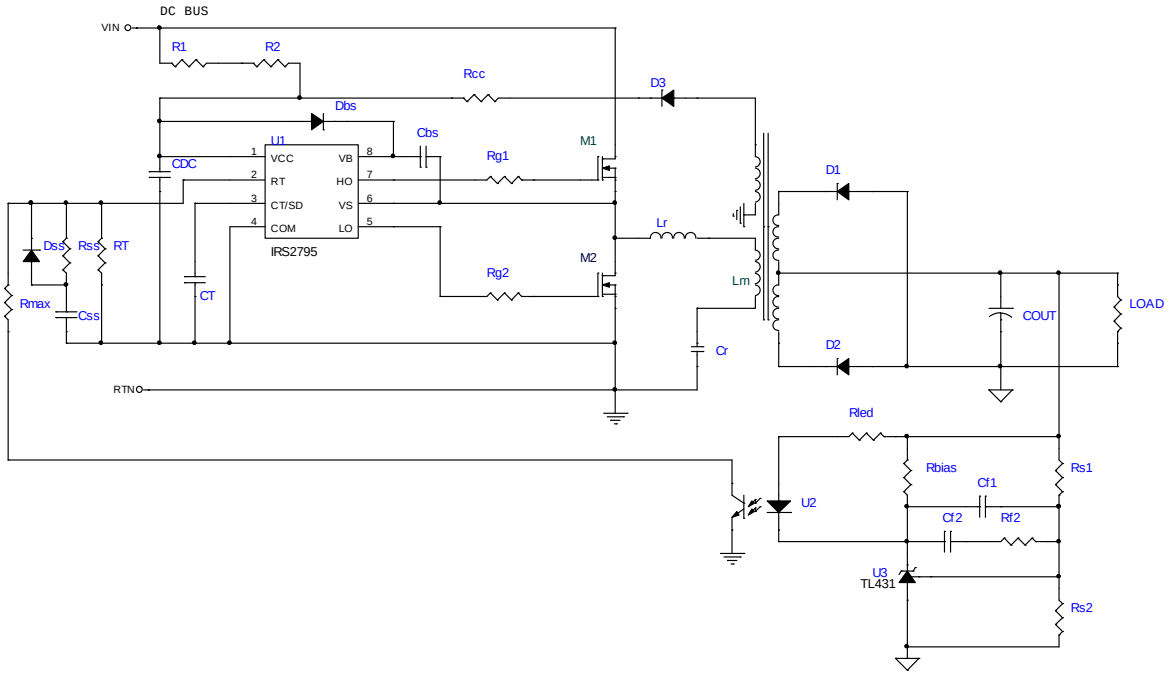


Figure 1: IRS2795(1,2) typical application circuit

The pinout of IRS2795(1,2) is shown below.

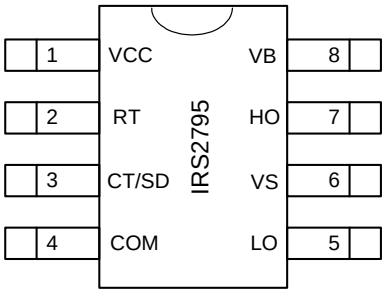
Lead Assignment	Pin#	Symbol	Description
	1	VCC	Supply voltage
	2	RT	Oscillator timing resistor
	3	CT/SD	Oscillator timing capacitor/Shutdown
	4	COM	Ground
	5	LO	Low-side gate drive
	6	VS	High-side gate drive return/ HV Current Sense
	7	HO	High-side gate drive
	8	VB	High-side floating supply voltage

Figure 2: IRS2795(1,2) IC pin assignment

2. LLC Resonant Half-Bridge Converter Operation

The increasing popularity of the LLC resonant converter in its half-bridge implementation is due to its high efficiency, low switching noise and ability to achieve high power density. This topology is also the most attractive topology for front-end DC bus conversion. It utilizes the magnetizing inductance of the transformer to construct a complex resonant tank with Buck Boost transfer characteristics in the soft-switching region. The typical power stage schematic for this topology is shown below.

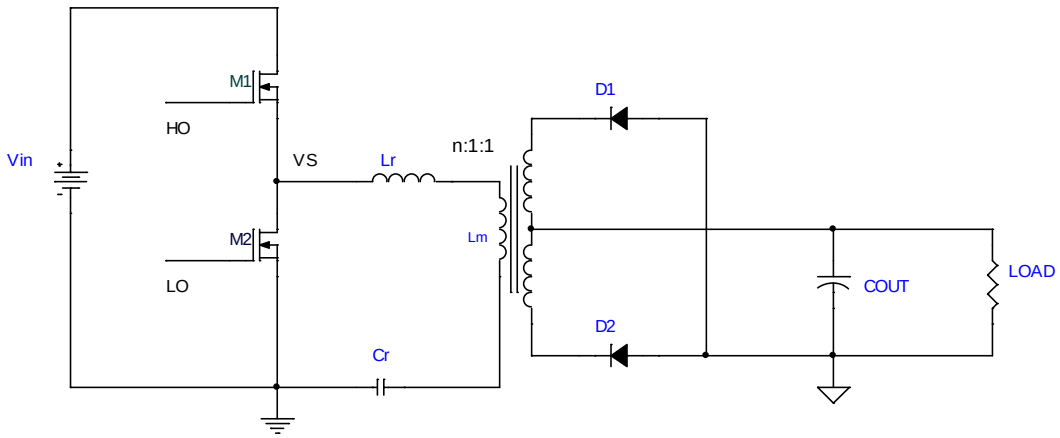


Figure 3: Typical schematic of a DC-DC half-bridge resonant converter

Devices M1 and M2 operate at 50% duty cycle and the output voltage is regulated by varying the switching frequency of the converter. The converter has two resonant frequencies – a lower resonant frequency (given by L_m, L_r, C_r and the load) and a fixed higher series resonant frequency F_{r1} (given by L_r and C_r only). The two bridge devices M1 and M2 can be soft-switched for the entire

load range by operating the converter under inductive load mode (ZVS region). It can be either above or below the resonant frequency F_{r1}.

The typical AC transfer characteristics[1] for a LLC tank resonant converter are shown in **Figure 4**. The group of curve indicates the gain under different load conditions.

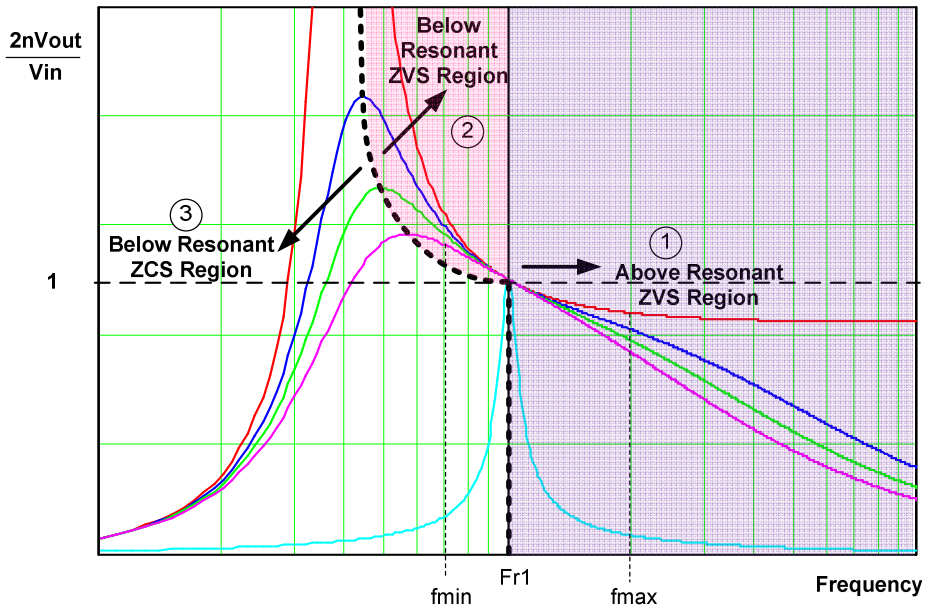


Figure 4: Typical frequency response of a LLC resonant converter

The characteristics of a LLC resonant converter can be divided into three regions based on the 3 different modes of operation.

The first region is for switching frequency above the resonant frequency F_{r1}.

$$F_{r1} = \frac{1}{2\pi\sqrt{L_r \cdot C_r}}$$

In region ① (the purple shaded area) the switching frequency is higher than resonant frequency F_{r1}. The converter operation is very similar to a series resonant converter. Here L_m never resonates with resonant capacitor C_r; it is clamped by the output voltage and acts as the load of the series resonant tank. This is the inductive load region and the converter is always under ZVS operation regardless of the load condition.

In the 2nd region, the switching frequency is higher than the lower resonant frequency but lower than F_{r1}. Region ② is in the pink shaded area in **Figure 4**. The lower resonant frequency varies with load, so the boundary of region ② and region ③ traces the peak of the family load vs. gain curves. In this complex region, the LLC resonant operation can be divided into two time intervals. In the first time interval, L_r resonates with C_r and L_m is clamped by output voltage. When the current in the resonant

[1] For this AC analysis, only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to output. The transformer, rectifier and filter are replaced by an equivalent AC resistance, *Rac*.

inductor L_r resonates back to the same level as the magnetizing current, L_r and C_r stop resonating. L_m now participates in the resonant operation and the second time interval begins. During this time interval, dominate resonant components change to C_r and L_m in series with L_r. The ZVS operation in region ② is guarantees by operating the converter to the right side of the load gain curve. For a switching frequency below resonant F_{r1}, it could falls in either region ② or region ③ depends on the load condition.

In the ZCS range ③ below f_{r1}, the LLC resonant converter operates in capacitive mode; M1 and M2 are under hard switching and have high switching losses. So ZCS operation should always be avoided.

The typical operating waveforms of the 3 modes are demonstrated in **Figure 5** to **Figure 7**.

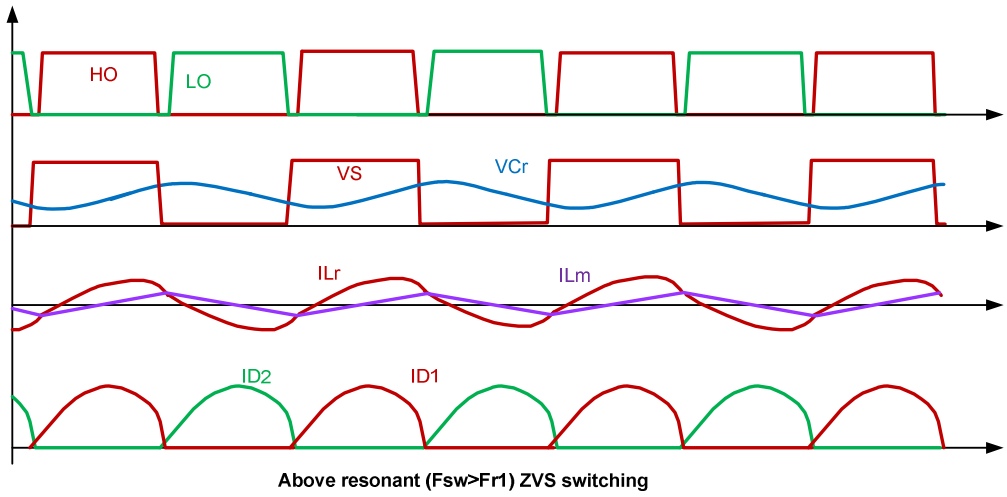


Figure 5: Typical waveform of above resonant ZVS switching

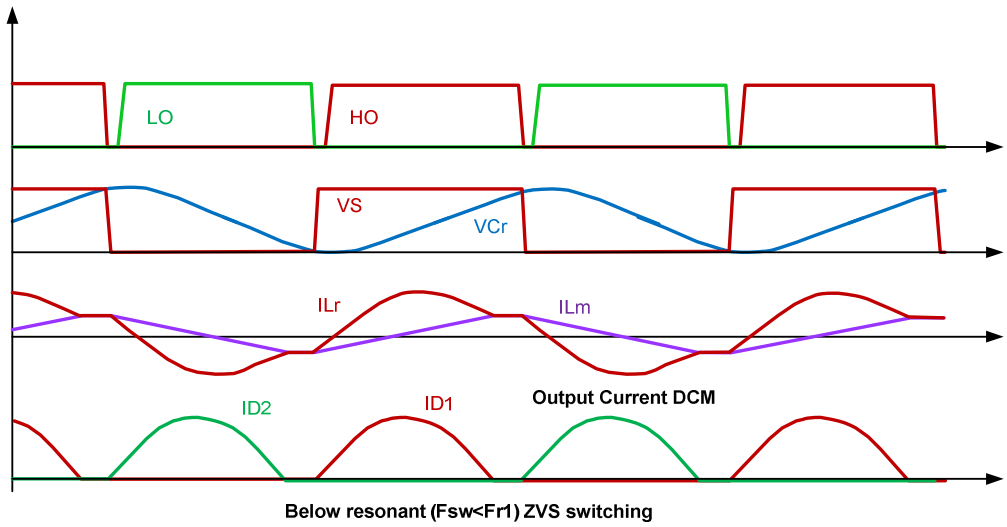


Figure 6: Typical waveform of below resonant ZVS switching

The waveforms indicate that the current in secondary rectifier diodes moves from continuous current mode (CCM) to discontinuous current mode (DCM) when the switching frequency varies from above resonant ZVS to below resonant ZVS due to load increasing. The ripple voltage on the resonant capacitor C_r also increases in the below resonant ZVS mode.

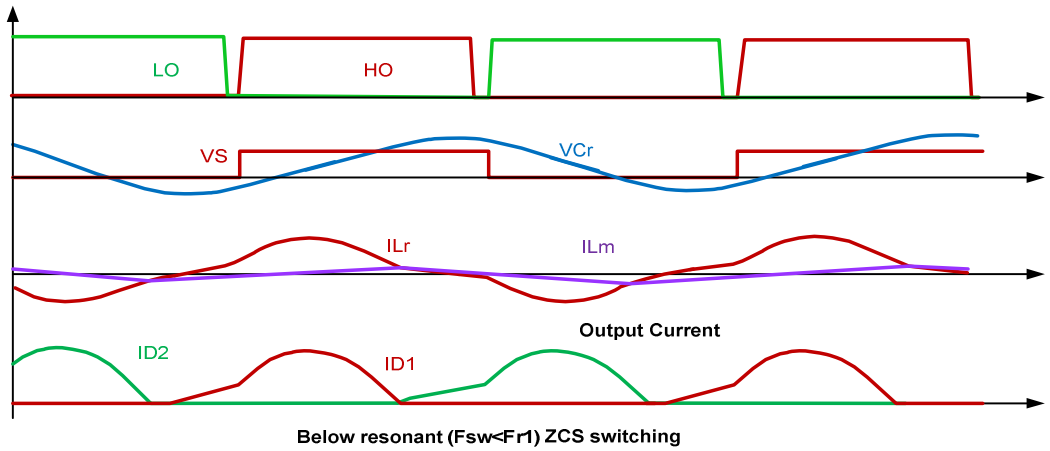


Figure 7: Typical waveform of below resonant ZCS switching

In ZCS mode, the two switching devices M1 and M2 are turned off under zero current condition. The turn-on of the two switches is hard switching (none ZVS). The turn-on switching loss is high especially under high voltage bus voltage. The resonant capacitor C_r also has high voltage stress. ZCS operation should always be avoided.

The typical voltage conversion ratio of a LLC resonant converter is shown in **Figure 8**.

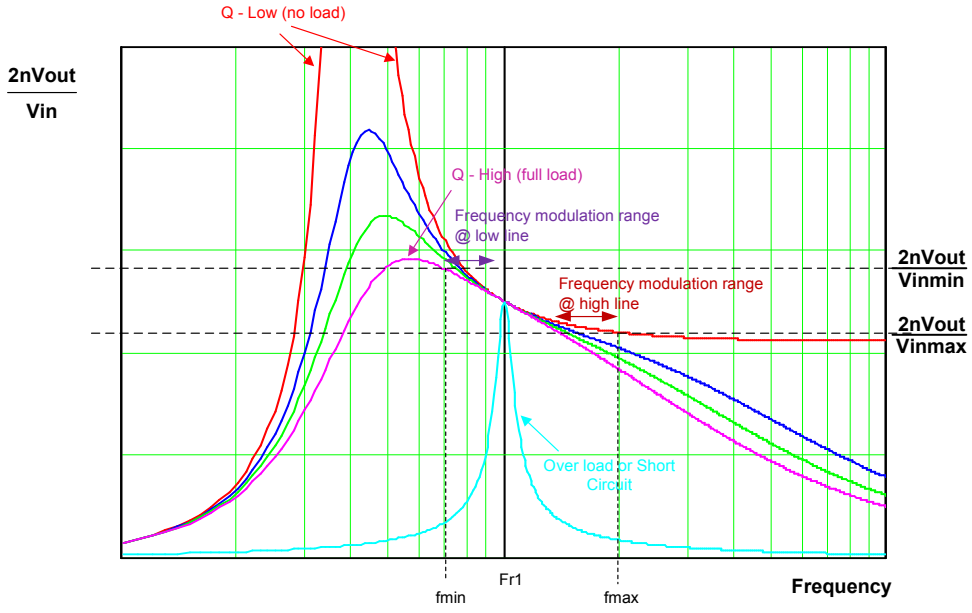


Figure 8: Typical voltage conversion ratio of a LLC resonant converter

With a fixed input voltage, the converter varies switching frequency to regulate the output voltage over load range – keeping the same conversion ratio over the family of curves with different Q.

Given a fixed load condition, the converter varies switching frequency along that load line to regulate output voltage over input voltage range – the conversion ratio increases when input voltage decreases.

To design the LLC resonant half-bridge converter, we use the First Harmonic Approximation (FHA) to get equivalent circuit. All the components are put to primary side to simply the analysis. The load equals to a resistor R_{ac} that is in parallel with transformer primary inductance L_m.

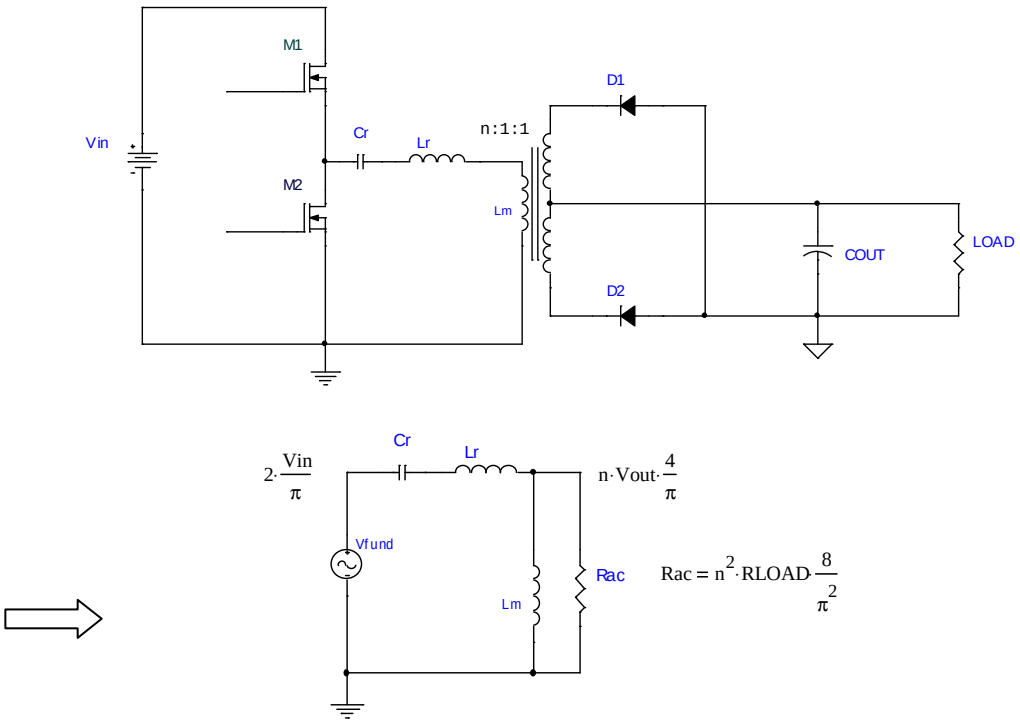


Figure 9: The FHA equivalent circuit

The input voltage of the resonant tank is a square wave with amplitude equals to the input DC voltage Vin. The fundamental component of the square waveform is:

$$\frac{2 \cdot Vin}{\pi} \sin(\varpi \cdot t)$$

The output voltage of the resonant tank is the voltage across L_m. It is very close to a square waveform with amplitude swinging from $-n \cdot Vout$ to $+n \cdot Vout$. So the fundamental component of the output square waveform is:

$$\frac{4 \cdot n \cdot Vout}{\pi} \sin(\varpi \cdot t)$$

The power dissipation on the equivalent AC resistor is equal to the power dissipation of R_{LOAD} resistor, thus it can be written as:

$$\frac{Vout^2}{R_{LOAD}} = \frac{\left(\frac{4 \cdot n \cdot Vout}{\sqrt{2}\pi}\right)^2}{Rac}$$

Rearrange the formula and get the equivalent AC resistor:

$$Rac = \frac{8 \cdot n^2}{\pi^2} R_{LOAD}$$

The transfer ratio of the equivalent circuit can be obtained as following:

$$M = \left| \frac{\frac{j \cdot \omega \cdot Lm \cdot Rac}{j \cdot \omega \cdot Lm + Rac}}{j \cdot \omega \cdot Lr + \frac{1}{j \cdot \omega \cdot Cr} + \frac{j \cdot \omega \cdot Lm \cdot Rac}{j \cdot \omega \cdot Lm + Rac}} \right|$$

Re-write the formula,

$$M = \left| \frac{1}{1 + \frac{Lr}{Lm} - \frac{1}{\omega^2 \cdot Lm \cdot Cr} + \frac{j\omega \cdot Lr}{Rac} - \frac{j}{\omega \cdot Cr \cdot Rac}} \right|$$

With the following definitions, M can be simplified.

$$F_{r1} = \frac{1}{2\pi\sqrt{L_r \cdot C_r}}, \qquad x = \frac{Fsw}{F_{r1}}, \qquad \varpi = 2\pi Fsw = 2\pi \cdot x \cdot F_{r1} = \frac{x}{\sqrt{L_r \cdot C_r}},$$

$$k = \frac{L_m}{L_r}, \qquad Rac = \frac{8 \cdot n^2 \cdot R_{LOAD}}{\pi^2}, \qquad Q = \frac{2\pi F_{r1} \cdot L_r}{Rac} = \frac{1}{2\pi F_{r1} \cdot C_r \cdot Rac}$$

$$M = \left| \frac{1}{1 + \frac{1}{k} \cdot \left(1 - \frac{1}{x^2}\right) + j \cdot Q \cdot \left(x - \frac{1}{x}\right)} \right|$$

Or,

$$M = \frac{1}{\sqrt{\left[1 + \frac{1}{k} \cdot \left(1 - \frac{1}{x^2}\right)\right]^2 + \left[Q \cdot \left(x - \frac{1}{x}\right)\right]^2}}$$

Per **Figure 9**, M is also equals to the output voltage to input voltage ratio:

$$M = \frac{n \cdot Vout \cdot \frac{4}{\pi}}{2 \cdot \frac{Vin}{\pi}} = \frac{Vout}{Vin} \cdot 2 \cdot n$$

So we have the conversion ratio of output voltage Vout to input voltage Vin:

$$\frac{Vout}{Vin} = \frac{M}{2 \cdot n}$$

3. Transformer and Resonant Circuit Design

This section provides the details of how to calculate the key components of a LLC converter, take a 24V output 240W power supply as an example.

The system input data

Parameter	Unit	Description	Value
Vin_{max}	V	The maximum DC bus voltage	430
Vin_{min}	V	The minimum DC bus voltage	350
Vin_{nom}	V	The nominal DC bus voltage	390
Vout	V	The DC output voltage	24
Iout	A	The output load current	10
F_{r1}	KHz	The resonant frequency	100
Fmax	KHz	The maximum switching frequency ①	150
Dmax		The maximum duty-cycle	0.5
Tss	ms	The soft start time	10
Fss	KHz	The soft start frequency	300
		Transformer	ETD49

①Note: Typically set Fmax < $2xF_{r1}$ as the parasitic capacitance in the system introduced a 3rd resonant frequency which could cause the output voltage to increase with switching frequency at no load if the maximum switching frequency is higher than the limit.

Step 1: Calculate the transformer turns ratio

$$n = \frac{Vin\max}{2 \cdot Vout},$$

$$n = \frac{430}{2 \cdot 24} = 8.96$$

The transformer turns ratio is calculated with the maximum input voltage to make sure the output is always under regulation, including the worst case - high-line voltage and no load condition.

Usually the transfer ratio of the power stage is higher than the theoretical calculated value. This is because of the parasitic capacitance in the system (the coupling capacitor between transformer windings and the junction capacitors of output diodes) affects the resonance, especially at zero load where the switching frequency is much higher than the resonant frequency. So it's recommended to choose the *n* to be slightly higher than the calculated value especially if the controller has no burst mode to keep regulation at high line and zero load condition.

$$n = 9$$

Step 2: Choose k value

k is the ratio between the transformer magnetic inductance and the resonant inductance. Smaller *k* value gives steeper Gain curve, especially at the below resonant ZVS region as shown in **Figure 10**. The output voltage is more sensitive to frequency variation with smaller *k* factor.

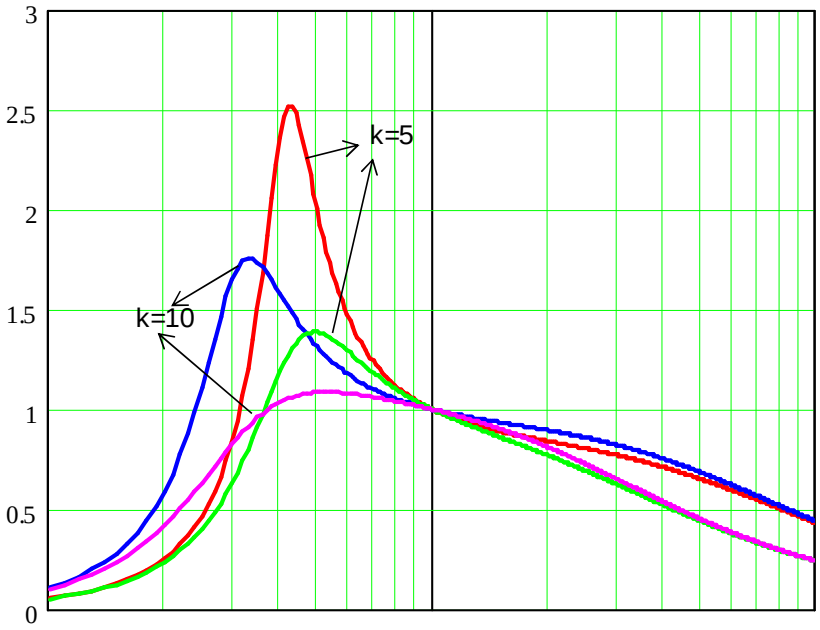


Figure 10: k factor

A higher *k* value results in higher magnetic inductance and thus lower magnetizing current in the transformer primary winding – that means lower circulating power losses. However, higher magnetic inductance could also cause non-ZVS switching at high line and zero load condition where the circulating current is too small to fully charge / discharge the VS node during dead-time.

The recommend range of k is from 3 to 10. Here $k = 5$ is chosen.

Step 3: Calculate Qmax to stay in ZVS operation at the maximum load under the minimum input voltage

The input impedance of the equivalent resonant circuit (Figure 9) is given by:

$$Zin = j\cdot\omega\cdot Lr + \frac{1}{j\cdot\omega\cdot Cr} + \frac{j\cdot\omega\cdot Lm\cdot Rac}{j\cdot\omega\cdot Lm + Rac}$$

$$Zin = Q\cdot Rac\left|\frac{k^2\cdot x^2\cdot Q}{1+k^2\cdot x^2\cdot Q^2} + j\left(x - \frac{1}{x} + \frac{x\cdot k}{1+k^2\cdot x^2\cdot Q^2}\right)\right|$$

To keep the converter working in soft switching mode, the operating point should always in the ZVS region as shown in **Figure 4**. The ZVS ZCS boundary line is defined by the phase angle of Zin Φ(Zin)= 0 (the boundary condition between capacitive and inductive load), i.e. the imaginary part of Zin is zero. With this condition we can calculate the maximum Q which allows the converter to stay in ZVS. The maximum Q happens at the minimum input voltage and the maximum load.

$$Qmax = \frac{1}{k}\cdot\sqrt{\frac{1+k\cdot\left(1-\frac{1}{Mmax^2}\right)}{Mmax^2-1}} = \frac{1}{k}\cdot\sqrt{\frac{1+k\cdot\left[1-\frac{1}{\left(2\cdot n\cdot\frac{Vout}{Vinmin}\right)^2}\right]}{\left(2\cdot n\cdot\frac{Vout}{Vinmin}\right)^2-1}}$$

Where *Mmax* is the maximum conversion ratio at the minimum input voltage,

$$Q\max = 0.456$$

Step 4: Calculate the minimum switching frequency

The minimum switching frequency happens at the maximum load and minimum input voltage with the previous calculated maximum Qmax. As Qmax is defined by Im(Zin)=0,

$$\left(x - \frac{1}{x} + \frac{x\cdot k}{1+k^2\cdot x^2\cdot Qmax^2}\right) = 0$$

The Fmin can be calculated with:

$$xmin = \frac{1}{\sqrt{1+k\cdot\left(1-\frac{1}{Mmax^2}\right)}} = \frac{1}{\sqrt{1+k\cdot\left[1-\frac{1}{\left(\frac{2n\cdot Vout}{Vinmin}\right)^2}\right]}}$$

$$x\min = 0.607$$

$$F\min = x\min\cdot F_{r1} = 60.7KHz$$

Step 5: Calculate L_r, C_r and L_m

As Qmax happens at the maximum load, so the resonant components L_r, C_r and L_m can be calculated per the Qmax value that had obtained in step 3:

$$R_{LOAD} = \frac{Vout}{Iout} = \frac{24V}{10A} = 2.4\Omega$$

$$Rac = \frac{8 \cdot n^2 \cdot R_{LOAD}}{\pi^2} = \frac{8 \times 9^2 \times 2.4}{\pi^2} = 157.57\Omega$$

$$L_r = \frac{Q\max \cdot Rac}{2 \cdot \pi \cdot F_{r1}} = \frac{0.456 \times 157.57}{2 \cdot \pi \cdot 100K} = 114uH$$

$$C_r = \frac{1}{2 \cdot \pi \cdot F_{r1} \cdot Q\max \cdot Rac} = \frac{1}{2 \cdot \pi \cdot 100K \times 0.456 \times 157.57} = 22.2nF$$

Choose the nearest standard capacitor value for C_r, $C_r = 22nF$

Recalculate F_{r1} to keep the same Qmax with the selected C_r capacitor.

$$F_{r1} = \frac{1}{2 \cdot \pi \cdot C_r \cdot Q\max \cdot Rac} = 100.7Khz$$

Recalculate L_r with the selected C_r and F_{r1}.

$$L_r = \frac{Q\max \cdot Rac}{2 \cdot \pi \cdot F_{r1}} = 113uH$$

The actual L_r value should be lower than the calculated value to stay in ZVS region.

Now calculate L_m value based on L_r and the *k* factor that preset in step 2:

$$L_m = L_r \cdot k = 113 \times 5 = 565uH$$

Please note that L_m is the magnetizing inductance of the transformer. The total primary inductance value L_p is the sum of L_m and L_r.

$$L_p = L_m + L_r = 678uH$$

To simplify the power stage, the resonant inductor can be integrated into the power transformer by using slotted bobbin, also called two-section or two-chamber bobbin. By separate the primary winding and the secondary winding in the two chambers, the coupling between primary and secondary is much worse than the single section bobbin. Thus the leakage inductance is high and can be used as resonant inductor. The component count is lower and the copper loss is also smaller. **Figure 11** is the picture of a two-section bobbin.

Figure 11: 2-section Transformer

When measure the inductance of a transformer, the primary inductance L_p is measured with all secondary windings opened. And the leakage inductance is measured with all the secondary windings shorted.

Step 6: Calculate transformer primary and secondary turns

The standard half-bridge equation for the transformer turns number calculation is used here:

$$Np = \frac{Vin\min \cdot D\max}{2 \cdot \Delta B \cdot Ae \cdot F\min}$$

With $\Delta B = 0.2T$, $Ae = 2.11cm^2$ (ETD49), $F\min = 60KHz$, $Vin\min = 350V$, $D\max = 0.5$

$$Np = \frac{350 \times 0.5}{2 \times 0.2 \times 2.11 \times 60} \times 10 = 35$$

$$Ns = \frac{Np}{n} = \frac{35}{9} = 3.89$$

The number of turns must be an integer and should be higher than the calculated value, so choose

$$Ns = 4$$

Then recalculate Np:

$$Np = Ns \cdot n = 4 \times 9 = 36$$

Step 7: Calculate transformer primary and secondary current

Most LLC converters design the minimum switching frequency to be below the resonant frequency Fr1, in order to maintain output voltage regulation at low line and full load. When the switching frequency is lower than the resonant frequency Fr1, the current waveform is shown as in **Figure 12**.

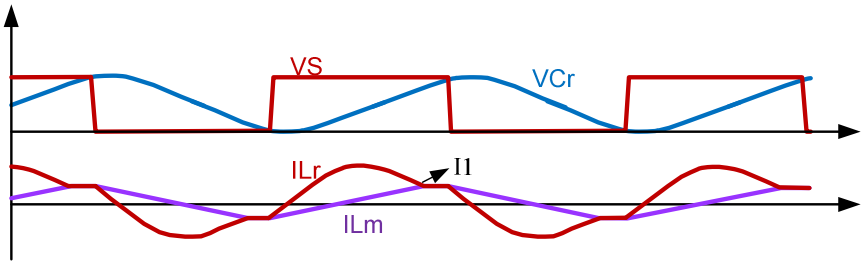


Figure 12: Transformer primary current at full load and minimum input voltage

I1 is the current where the resonant current in L_r meets the magnetizing current in L_m. This is also the point where C_r and L_r finish resonance for the first half-period of F_{r1}. At this point, there is no more energy delivered to the load and the output diodes are off. The C_r starts to resonate with L_r + L_m until the switching MOSFETs change states. I1 can be calculated as:

$$I1 = \frac{n \cdot Vout}{2 \cdot Lm \cdot 2 \cdot Fr1} = 0.95A$$

The peak and RMS value of primary current can be estimated as:

$$Ipri(pk) = \sqrt{\left(\frac{Iout \cdot \pi}{2 \cdot n}\right)^2 + I1^2} = 1.99A$$

$$IpriRMS = \frac{Ipri(pk)}{\sqrt{2}} = 1.4A$$

The RMS current is calculated by assuming pure sinusoid current waveform. So the actual primary RMS current is higher than the calculated value.

The current in each secondary winding is very close to half-sinusoid, thus the peak and RMS current can be estimated by:

$$Ispk = \frac{Iout \cdot \pi}{2} = 15.7A$$

$$Isrms = \frac{Iout \cdot \pi}{4} = 7.85A$$

The wire gauge of primary and secondary windings should be selected properly according to the calculated RMS current.

Step 8: Calculate resonant capacitor voltage

The C_r waveform is shown as in **Figure 13**:

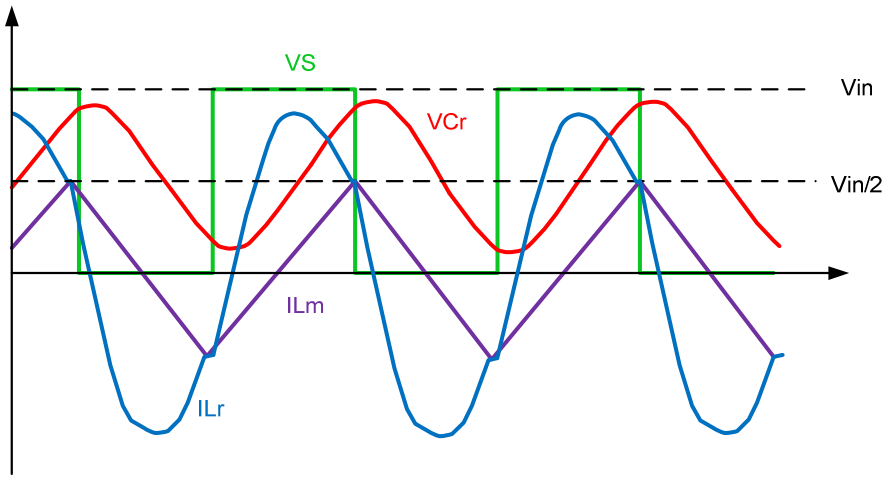


Figure 13: Typical resonant tank voltage and current waveforms

IL_m is the magnetizing current of transformer primary, not including the current which is delivered to the secondary load through an ideal transformer in parallel with L_m. The difference between IL_r and IL_m is the output current.

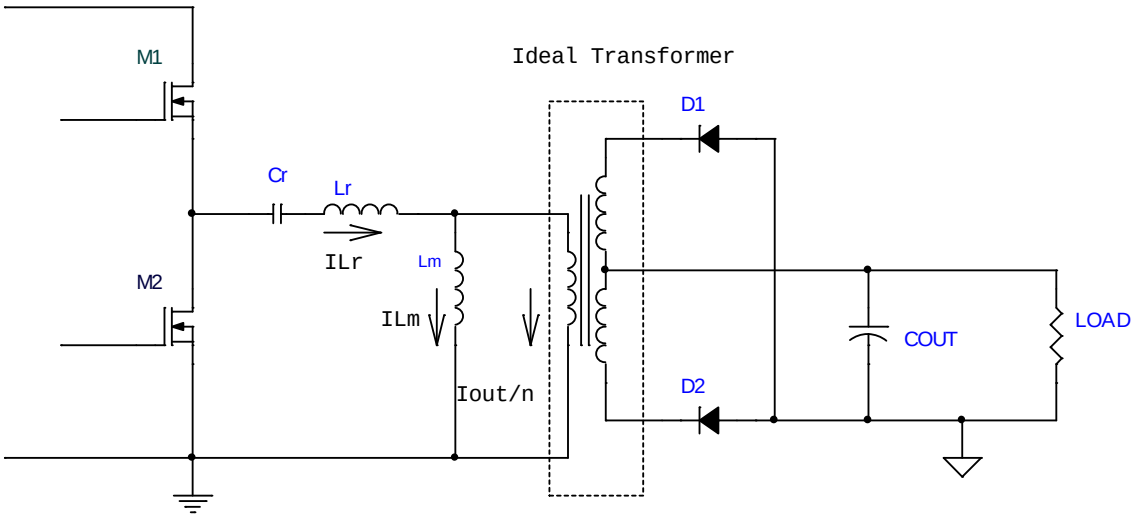


Figure 14: L_m and ideal transformer

The VC_r voltage reaches its peak when L_r current is crossing zero and it is at the mid of input voltage when L_r current reached its peak. The C_r voltage is at the maximum value when VS node is zero and it is at the minimum value when VS node is equals to Vin. So VC_{rmin} and VC_{rmax} can be calculated as:

$$VC_{r\max} = n \cdot Vout + Ipri(pk) \times \sqrt{\frac{L_r}{C_r}}$$

$$VC_{r\min} = Vin - n \cdot Vout - Ipri(pk) \times \sqrt{\frac{L_r}{C_r}}$$

The peak to peak voltage ripple of VC_r is VC_{rmax}-VC_{rmin}.

$$VC_{rpk\_pk} = 2n \cdot Vout + 2 \cdot Ipri(pk) \times \sqrt{\frac{L_r}{C_r}} - Vin$$

It can be seen that the maximum peak-to-peak voltage happens at the maximum load and the minimum DC input Vinmin, the switching frequency is at the minimum Fmin.

In this example:

$$Vcrpk\_pk = 2 \times 9 \times 24V + 2 \times 1.99A \times \sqrt{\frac{113uH}{22nF}} - 350V = 368V$$

The resonant capacitor C_r can be selected according to the capacitance value, together with its voltage and current rating. Polypropylene film capacitor is preferred to use for lower power loss. Please note the polypropylene film capacitor is rated under DC voltage or 50Hz AC voltage and has voltage derating at high frequency and high ambient temperature. The ability of withstanding high frequency voltage is limited by thermal (power dissipation) and peak current capability. Usually the derating starts at 85~90C ambient and is not a concern. But a capacitor with higher voltage rating

should be chosen if the ambient temperature is higher than 85C. Below is an example of EPCOS MKP capacitor B32621 (630Vdc/400Vac).

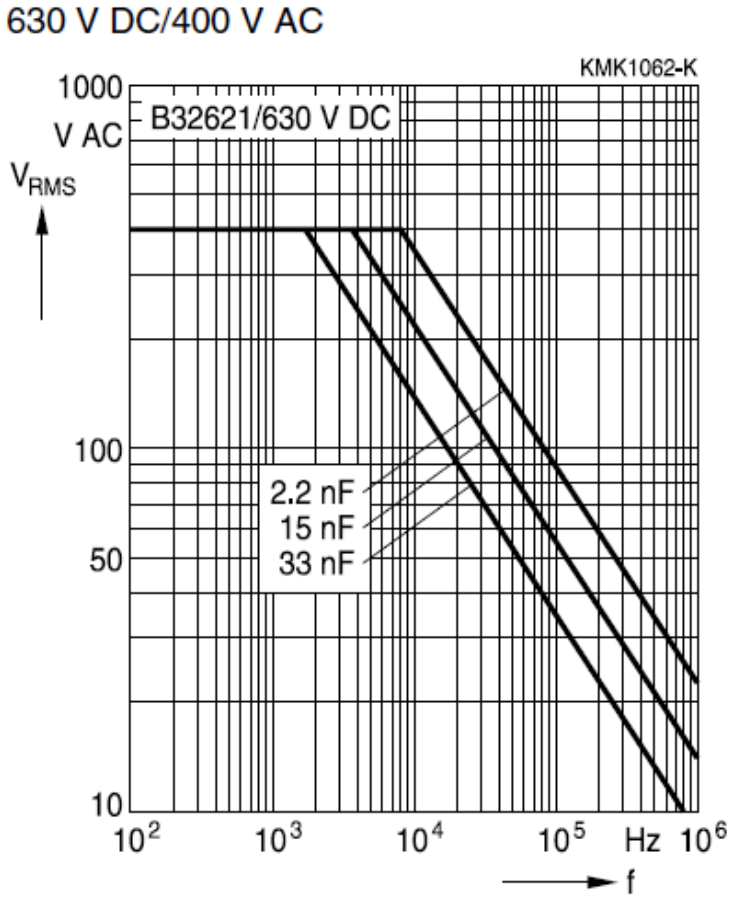


Figure 15: Vrms vs. frequency curve of MKP capacitor B32621 @ Ta<=90℃

4. IRS2795 Passive Components Design

Step 9: Calculate the minimum dead-time to keep ZVS switching at zero load at the maximum input voltage

For resonant half-bridge converter, the switching frequency goes to the maximum under no load at the maximum input voltage. Theoretically when the switching frequency is above the resonant frequency Fr1, the operation is ZVS switching. However, above resonance is only one of the necessary conditions for ZVS. The other condition is the equivalent parasitic capacitor of the half-bridge midpoint (junction capacitor of VS node) to be fully (dis-)charged within the dead-time period. **Figure 16** demonstrates if the dead-time is not sufficient, the turn-on of the MOSFET has hard-switching even though the converter is working under the below resonant ZVS mode.

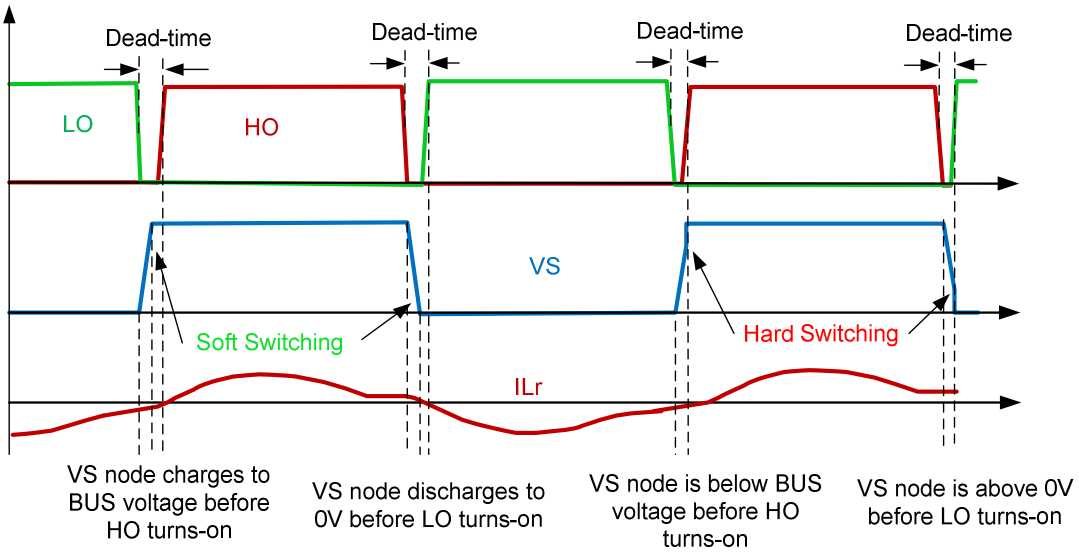


Figure 16: ZVS and none-ZVS waveform of region 2 operation

To keep the converter always working under ZVS condition, it is necessary to calculate the minimum time that required to fully (dis-)charging the VS equivalent capacitor during the two switches interleaving period (dead-time).

As the equivalent capacitor is (dis-)charged by the circulating current in the transformer primary winding, so the worst case happens at the maximum input voltage and zero load condition where the transformer current is at minimum. At zero load, there is no current transfer to the secondary side and the current in the tank is just the magnetizing current of transformer. In each half-cycle, it is a linear straight line as shown in **Figure 17**.

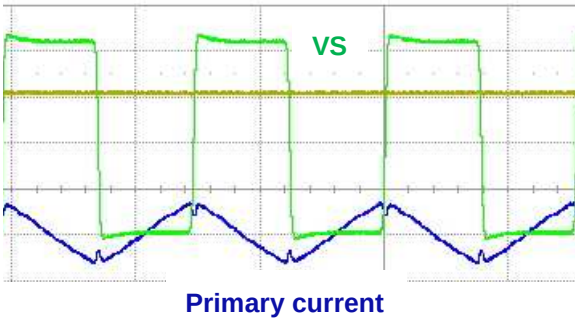


Figure 17: Transformer primary current at zero load

So the primary current under this condition can be calculated as:

$$I'pri(pk) = \frac{n \cdot Vout}{4F \max \cdot (Lr + Lm)}$$

$$I'pri(pk) = 0.53A$$

The total equivalent junction capacitor C_{HB} of VS node is shown in **Figure 18**.

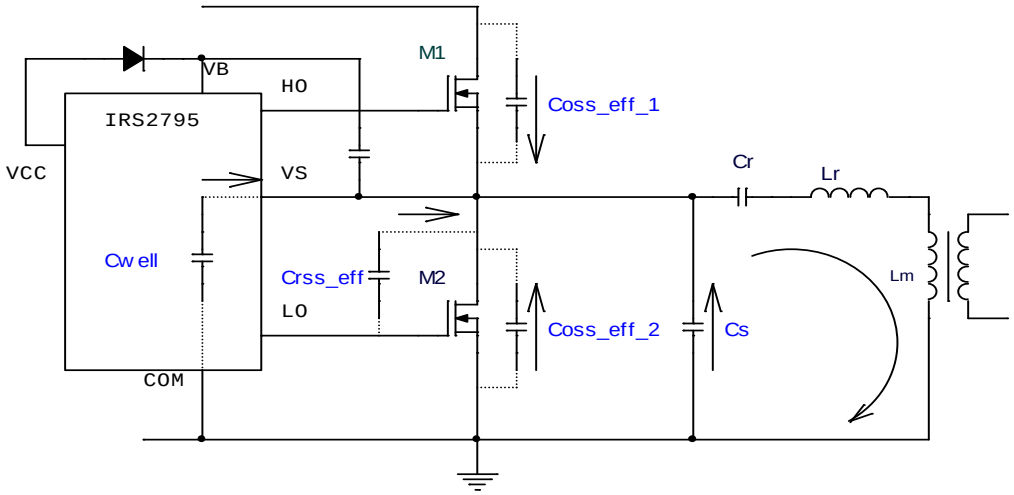


Figure 18: VS Equivalent junction capacitor

$$C_{HB} = 2 \cdot Coss\_eff + Crss\_eff + C_{Well} + Cs$$

It includes:

The *effective Coss* of the two MOSFETs (both high-side and low-side);

The *Coss_eff* as defined in the MOSFET datasheet is the effective capacitance of MOSFET that gives the same charging time as a fixed capacitor while V_{DS} is rising from 0 to 80% of V_{DS}. So the *Coss_eff* of a 500V MOSFET is defined under 0 to 400V V_{DS} which fits to this application.

The *effective Crss* of the low-side MOSFET;

The *Crss* of MOSFET is typically defined at VDS=25V. The *Crss* capacitance value reduces as VDS voltage increasing. So the *effective Crss* can be chose as ½ or 1/3 of *Crss*.

The stray capacitance *Cwell* of IRS2795(1,2);

The stray capacitance of IRS2795(1,2) is the high-side well capacitance of the 600V driver. The value of the stray capacitor is around 5pF.

The snubber capacitor Cs (if any) that is connected to the VS node.

For example, the *Coss_eff* of MOSFET STF13NM50N is 110pF, Crss is 5pF, and there is no snubber capacitor to the VS node, the (dis-)charging time of VS node can be calculated as:

$$Coss\_eff = 110\,pF\ ,\ Crss\_eff = 2.5\,pF\ ,\ C_{Well} = 5\,pF\ ,\ Cs = 0\,pF$$

$$Tch = \frac{C_{HB} \cdot Vin\max}{I'pri(pk)}$$

$$Tch = 185ns$$

The dead-time calculation should also include the gate driver falling time. The MOSFET turn-off timing diagram is shown in **Figure 19**, which using LO and M2 as an example. In the first time interval t1, gate voltage discharges to a plateau voltage V'm, and both VDS voltage and I_D current

stay unchanged in t1. As long as MOSFET gate voltage reaches the miller plateau V'm, miller cap Cgd is discharged and VDS voltage starts increasing. Due to the nonlinearity of Coss capacitor, VDS voltage increase slowly at the beginning, then the slope becomes steeper at higher VDS voltage. The miller plateau is the flat portion of gate driver curve. It varies with drain current. MOSFET turns off at a relative low current level in LLC application, the miller plateau is very close to the gate turn off threshold Vgs(th).

The timing that is interested for the dead time calculation is t1, as the charging time of the VS node (i.e. VDS of M2) starting from t2 is already included in the *Tch* calculation. In t1, VDS voltage is 0V, and MOSFET gate equals to a constant capacitor load to the IC. So the discharge time t1 can be calculated based on the RC time constant of the gate drive loop.

$$t_1 = -RC_{geq} \ln \frac{V'm}{V_G}$$

Where, $R = R_{down\_eff} + R_g + R_{gFET}$

$C_{geq} = \frac{(Qg - Qgd - Qgs)}{Vgs - Vm}$, Please refer to **Figure 21.**

$V'm \approx Vgs(th)$

$V_G = Vcc$, IRS2795(1,2) gate output voltage is clamped to Vcc voltage

R_{down_eff}: IRS2795(1,2) gate driver effective pull down resistance (6Ω)

R_g :is the external MOSFET gate drive resistor

$R_{gFET:}$ MOSFET gate input resistance

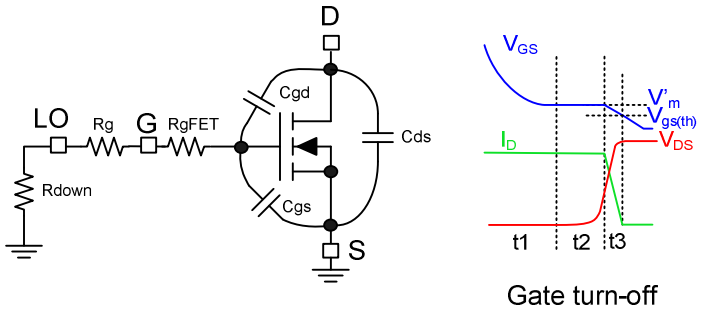


Figure 19: MOSFET turn-off equivalent circuit and timing diagram

STF13NM50 gate equivalent capacitor is 2.32nF, MOSFET internal gate resistor is 5Ω, Vgs(th) is 3V. Thus if Vcc=15V, Rg=10Ω, gate discharge time t1 is:

$$t_1 = 78.4ns$$

The dead-time should be longer than the sum of *Tch* and t1. For experience, it is recommended to add 50ns to the calculated value. The minimum dead-time T_{DT} is then given by:

$$T_{DT} = Tch + t_1 + 50ns = 313ns$$

For most of the design, it's not recommended to have a dead-time that is longer than 1us, as longer dead-time leads to higher body-diode power losses at full load. So if the calculated dead-time is too long, go back to step 2 and choose a smaller *k* value.

Once the system parameters are defined, the passive components around the IRS2795(1,2) as shown in **Figure 20** can be calculated.

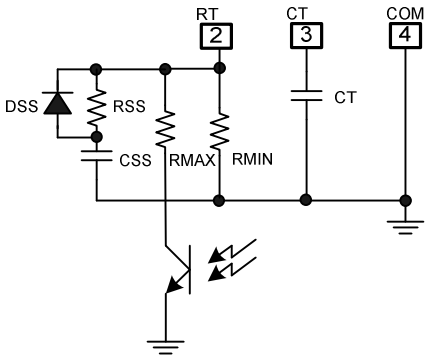


Figure 20: IRS2795(1,2) two-pin Oscillator

$$C_T = \frac{T_{DT} \cdot 10^{-3} - 40 \cdot 10^{-12}}{0.85} = \frac{313 \cdot 10^{-12} - 40 \cdot 10^{-12}}{0.85} = 321pF$$

C_T capacitor should be equal or bigger than the calculated value for ZVS operation. Choose a standard capacitor value for C_T.

$$C_T = 390\,pF$$

Calculate the actual dead-time per the selected C_T value:

$$t_{DT} = (0.85C_T + 40\,pF) \cdot \frac{2V}{2mA} = 371.5ns$$

Calculate R_T per the minimum switching frequency Fmin and C_T:

$$R_T = \frac{1}{2 \cdot F\,\min \cdot t_{DT} \cdot 10^{-3}} - 1k\Omega$$

R_T resistor should be smaller than the calculated value to keep ZVS operation.

Calculate Rmax per the maximum switching frequency Fmax and C_T, R_T:

$$\mathrm{Re}\,q = \frac{1}{2 \cdot F\,\max \cdot t_{DT} \cdot 10^{-3}} - 1k\Omega, \qquad R\max = \frac{R_T \cdot \mathrm{Re}\,q}{R_T - \mathrm{Re}\,q}$$

Calculate Rss with the desired soft-start frequency:

$$Rsseq = \frac{1}{2 \cdot Fss \cdot t_{DT} \cdot 10^{-3}} - 1k\Omega, \qquad Rss = \frac{RT \cdot Rsseq}{RT - Rsseq}$$

Calculate Css based on the desired soft-start time:

$$Css = \frac{Tss}{3 \cdot Rss}$$

In sleep mode or fault mode, RT pin is discharged to 0V. A diode Dss is put in parallel with Rss to fast discharge Css when IC is shutdown or in fault mode. This is to make sure the system still has soft start when IRS2795(1,2) restarts quickly. Dss can be any general purpose low voltage (10V) and low current (100mA) diode.

The bootstrap capacitor C_{BS} is used to hold V_{BS} supply voltage for the high-side driver. The value of C_{BS} is recommended to be 100nF to 220nF. Bigger C_{BS} capacitor causes higher charging current

during startup and should be avoid. IRS2795(1,2) doesn't have integrated bootstrap MOSFET. A 600V/1A fast recovery diode is required for bootstrap.

5. IRS2795 Power Loss Calculation

5.1 Low voltage static loss that caused by quiescent current

$$Pd1 = Vcc \times Iqcc$$

where Iqcc is 2.5mA maximum per IRS2795(1,2) datasheet.

5.2 The gate driver power losses

The gate driver losses of IRS2795(1,2) are the losses when driving the two external MOSFETs M1 and M2. In ZVS mode, MOSFET V_{DS} voltage is 0V prior to the gate turns on, so the "Miller" charge Qgd should be subtracted from the total gate charge. Further, at ZVS operation, the MOSFET is as a constant capacitor load to the driver. The equivalent capacitor value equals to the Cgs+Cgd at VDS=0V condition, which can be obtained from the gate charge curve in a MOSFET data sheet. It is indeed the slope factor of the gate charge curve where VGS is above the miller plateau voltage Vm, as shown in **Figure 21**.

$$C_{geq} = \frac{(Qg - Qgd - Qgs)}{Vgs - Vm}$$

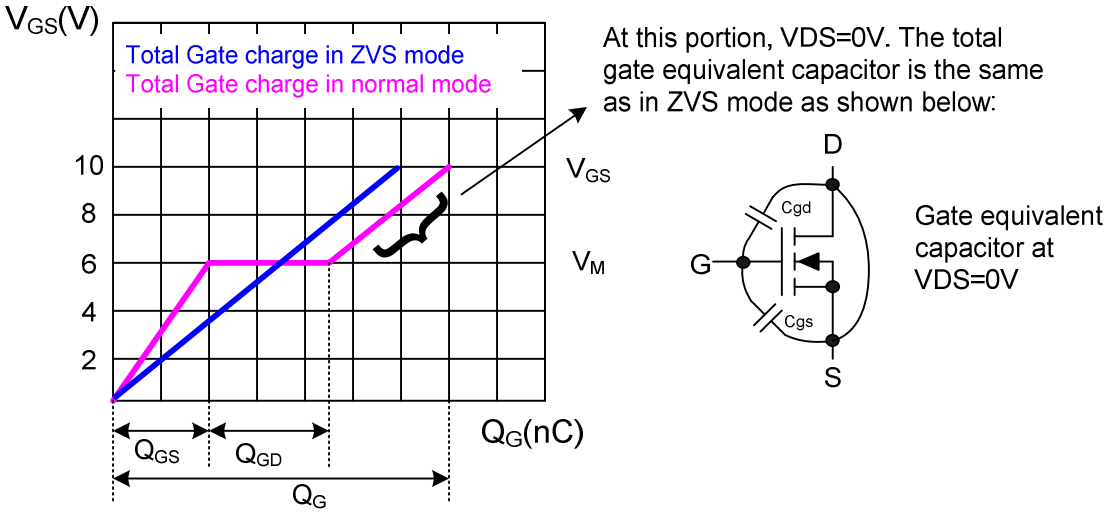


Figure 21: MOSFET gate charge curve and equivalent gate capacitance at ZVS mode

Typically the Qg, Qgd and Qgs value are specified under 10V V_{GS} voltage, Vm is the flat portion voltage of the gate charge curve. For example, STF13NM50 Qg=30nC, Qgd=15nC, Qgs=5nC, Vm=5.7V, its gate equivalent capacitor in ZVS is 2.32nF.

The total gate charge in ZVS mode is proportional to the gate voltage:

$$Qgz = Cgeq \cdot V_G$$

IRS2795(1,2) gate output voltage is clamped to Vcc voltage. So the total gate driver losses of both high-side and low-side can be calculated by:

$$Pdr = Pdr1 + Pdr2 = 2 \cdot Cgeq \cdot Vcc^2 \cdot Fsw$$

The total gate driver losses are dissipated in driver IC IRS2795(1,2) and the external gate driver resistor including the MOSFET internal gate resistor. The power loss in IRS2795(1,2) is proportional to the resistor divider value:

$$Pd2 = \left(\frac{Rup\_eff}{Rup\_eff + Rg + R_{g\ FET}} + \frac{Rdown\_eff}{Rdown\_eff + Rg + R_{gFET}}\right) \times \frac{Pdr}{2}$$

Where,

R_g :is the external MOSFET gate drive resistor

R_{up_eff}: IRS2795(1,2) gate driver effective pull up resistance (40Ω)

R_{down_eff}: IRS2795(1,2) gate driver effective pull down resistance (6Ω)

$R_{gFET:}$ MOSFET gate input resistance

The gate driver pull-up and pull-down resistance used for power loss calculation are given below: $Rup = 40\Omega, Rdown = 6\Omega$. They are bigger than datasheet specification (with is defined under 20mA current) as they are the equivalent pull-up and pull-down resistance under high gate current.

5.3 The CMOS switching losses

The switching loss in low voltage logic circuit is proportional to the switching frequency and supply voltage Vcc:

$$Pd3 = Vcc \times Fsw \times Qcmos$$

For IRS2795(1,2),

$$Qcmos = 6nC \sim 10nC$$

5.4 The high voltage switching losses

The switching losses in high voltage level-shift circuit:

$$Pd4 = (Vcc + Vin) \times Fsw \times Qp$$

Vin is the input bus voltage. Qp is the charge absorbed by the level shifter. For IRS2795(1,2), Qp is 2nC under 300V to 430V bus voltage.

5.5 An example of power loss calculation

The total power loss in IRS2795(1,2) is the sum of Pd1 to Pd4.

$$Pd\_total = Pd1 + Pd2 + Pd3 + Pd4$$

An example of power loss calculation with Vcc=15V, maximum switching frequency =150KHz, MOSFETs =STF13NM50N, input bus voltage = 400V, external gate resistor = 10ohm:

$$Pd1 = 37.5mW$$

$$Pdr = 157mW, Pd2 = 79.5mW$$

$$Pd3 = 18mW$$

$$Pd4 = 124.5mW$$

$$Pd\_total = 259.5mW$$

It can be seen that the high voltage switching loss Pd4 and gate driver loss Pd2 are the main source of total power losses. Pd4 is proportional to switching frequency and HV bus voltage. For 400V DC BUS voltage, IRS2795(1,2) can directly drives big MOSFETs (Cgeq ≤ 4.7nF) up to 250KHz switching frequency. It is necessary to clamp the Vcc supply voltage to 15V or lower to reduce gate driver losses when the frequency goes to 300KHz while driving big MOSFETs. For 300KHz to 500KHz switching frequency and 400V applications, it is recommended to use external driver.

IC operation current Icc can be obtained by the total low-voltage power loss and Vcc voltage:

$$Icc = (Pd1 + Pdr + Pd3)/Vcc$$

6. MOSFET Selection Guide

The power MOSFET should be selected per the breakdown voltage and R_{DSON} value. In addition, the body diode reverse recovery characteristic also plays important role to the selection. The converter usually has a few switching cycles that is under hard switching at the beginning of startup. This is because the resonant capacitor and output capacitors are fully discharged. In this case, longer reverse recovery time could cause shoot through between the two MOSFETs. Thus a MOSFET with fast reverse recovery diode is preferred.

As the resonant half-bridge has ZVS switching, the turn-on loss is negligible. If not switching under very high frequency (≤150Khz), the major power loss in MOSFET comes from the conduction loss. The maximum conduction loss can be calculated as:

$$Pcon = Iqrms^2 \times Rdson_{@Tj}$$

Where $Iqrms = \frac{Ipri(pk)}{2}$, and $Rdson_{@Tj}$ is the MOSFET on-state resistance at the system maximum allowable junction temperature.

The calculation of the turn-off loss of MOSFET is complicated due to none linearity of Coss under different VDS voltage. Thus we use the estimated formula:

$$Poff = \frac{C_{HB} \times Vin^2 \times Fsw}{24}$$

The total power loss in each MOSFET equals to $Pcon + Poff$.

IRS2795(1,2) uses the Rdson of low side MOSFET for current sensing and over current protection. The product family provides two choices on different over current protection level: the OCP threshold of IRS27951 is 2V and IRS27952 is 3V. Typically the IRS27951 is good for oversized MOSFET where a lower Rdson for better efficiency and the IRS27952 is good for cost effective MOSFET where the Rdson is bigger. A quick estimation for OCP threshold is to use 2.5 to 3 times of the maximum drain current times the Rdson of MOSFET.

At startup, the MOSFET current could be a few times higher than the normal working current. To prevent false triggering of over current protection when using large Rdson MOSFET, it is recommended to extend the soft-start time to tens of milliseconds.

7. Operating Waveforms and Efficiency of the Reference Design

The specification of the reference design:

Parameter	Description	Value
Vin_{max}	The maximum DC bus voltage	430V
Vin_{min}	The minimum DC bus voltage	350V
Vin_{nom}	The nominal DC bus voltage	390V
Vout 1	The DC output voltage	24V
Iout 1	The output load current	6A
Vout 2	The DC output voltage	12V
Iout 2	The output load current	6A
F_{r1}	The resonant frequency	100KHz
Fmax	The maximum switching frequency	150KHz
Dmax	The maximum duty-cycle	0.5
Tss	The soft start time	30ms
Fss	The soft start frequency	300KHz
	Transformer	ETD49

Design analysis result:

Resonant tank components	Cr=22nF, Lr=125uH, Lm=500uH, k=4
Transformer	Np=36, N24V=4, N12V=2, n=9
IRS27951 components	CT=390pF, RT=18k, Rmax=14k, Rss=3.9k, Css=3.3uF

7.1 Schematic

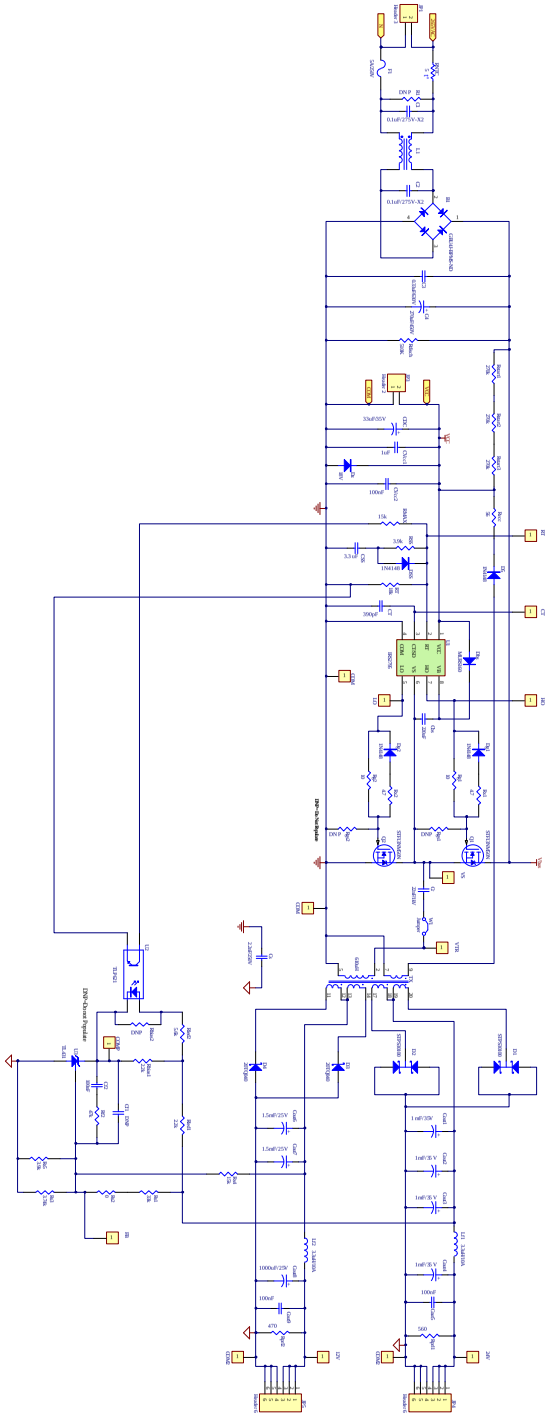


Figure 22 – IRS27951 Reference Design Schematic

The reference board has input rectifier and filter, so it can take either DC or AC input. The DC input range is 350V~430V, the AC input voltage range is 250Vac~300Vac.

The dummy loads at 24V and 12V output are for cross-regulation purpose.

7.2 BOM

Designator	Description	Quantity	Value/Rating	Vendor	Part#
B1	Single Phase Bridge Rectifier	1	600V/4A	DIGIKEY	GBU4J-BPMS-ND
C1, C2	X2 Safety Capacitor	2	100nF/275VAC	DIGIKEY	P10524-ND
C3	Metal Poly Capacitor	1	0.33uF/630V	DIGIKEY	P12245-ND
C4	Electrolytic Bulk Capacitor TS-HC	1	270uF/450V	DIGIKEY	EET-HC2W271LA
Cbs	1206 General Purpose Ceramic SMD	1	220nF/50V	DIGIKEY	490-1776-1-ND
Cf2, Cout5, Cout9, CVcc2	1206 General Purpose Ceramic SMD	4	100nF/50V	DIGIKEY	490-1775-1-ND
CDC	Electrolytic Capacitor FM Radial	1	33uF/35V	DIGIKEY	P13475-ND
Cf1	Not Used				
Cout1, Cout2, Cout3, Cout4	Aluminium Electrolytic Capacitor 105℃	4	1000uF/35V	DIGIKEY	565-1581-ND
Cout6, Cout7	Aluminium Electrolytic Capacitor 105℃	2	1500uF/25V	DIGIKEY	565-1557-ND
Cout8	Aluminium Electrolytic Capacitor 105℃	1	1000uF/ 25V	DIGIKEY	565-1555-ND
Cr	Polypropylene Capacitor High Ripple	1	22nF/1kV	DIGIKEY	495-3552-ND
Cs	250VAC Y1 Safety Ceramic Disc Capacitor	1	2.2nF/250V	DIGIKEY	445-2411-ND
CSS	1206 General Purpose Ceramic SMD	1	3.3uF/16V	DIGIKEY	445-4038-1-ND
CVcc1	1206 General Purpose Ceramic SMD	1	1uF/25V	DIGIKEY	445-1592-1-ND
CT	1206 General Purpose Ceramic SMD ±5%	1	390pF/50V	DIGIKEY	478-1487-1-ND
D1, D2	TO220AB Power Schottky Rectifier	2	100V/30A	DIGIKEY	STPS30100CT
D3, D4	TO220AC Power Schottky Rectifier	2	40V/20A	DIGIKEY	20TQ040PBF-ND
D5, Dg1, Dg2, DSS	Fast Recovery Diode DO-35	4	75V/0.3A	DIGIKEY	1N4148DICT-ND
Dbs	Fast Recttifier diode SMB	1	600V/1A	DIGIKEY	MURS160-FDICT-ND
Dz	Zener Diode SMD	1	18V/0.5W	DIGIKEY	FLZ18VCCT-ND
F1	FUSE IEC FA LBC 5x20	1	250V/5A	DIGIKEY	F2395-ND
JP1	CONN HEADER 3POS 0.156 VERT TIN	1		DIGIKEY	WM4621-ND
JP3	CONN HEADER 2POS 0.1 VERT TIN	1		DIGIKEY	WM4200-ND
JP4, JP5	CONN HEADER 6POS 0.156 VERT TIN	2		DIGIKEY	WM4624-ND
L1	EMI Common Mode Choke	1	16mH/2.6A	DIGIKEY	237-1233-ND
Lf1, Lf2	PCV Series Drum Core Inductor 10mm	2	4.7uH/12A	COILCRAFT	PCV-0-472-10L
Q1, Q2	TO-220FP N-Channel Power MOSFET	2	500V/12A	DIGIKEY	STF13NM50N
R1, Rbias2, Rgs1, Rgs2	Not Used				
Rbias1, Rled1	1206 SMD Film RED 1/4W 1%	2	2.2k	DIGIKEY	RHM2.20kFCT-ND
Rdisch	Metal Film Power Resistor 2W 5%	1	510k	DIGIKEY	BC510KW-2CT-ND
Rf2	1206 SMD Film RED 1/4W 1%	1	47k	DIGIKEY	RHM47.0kFCT-ND
Rg1, Rg2	1206 SMD Film RED 1/4W 5%	2	10	DIGIKEY	RHM10ERCT-ND
Rled2	1206 SMD Film RED 1/4W 1%	1	5.6k	DIGIKEY	RHM5.60kFCT-ND
RMAX	1206 SMD Film RED 1/4W 1%	1	15k	DIGIKEY	RHM15.0kFCT-ND
RNTC	Inrush Current Limiter	1	5	DIGIKEY	495-2093-ND
Rprl1	Metal Film Power Resistor 2W 5%	1	560	DIGIKEY	PPC560W-2CT-ND
Rprl2	Metal Film Power Resistor 2W 5%	1	470	DIGIKEY	PPC470W-2CT-ND
Rs1	1206 SMD Film RED 1/4W 1%	1	33k	DIGIKEY	RHM33.0KFCT-ND
Rs2	1206 SMD Film RED 1/4W 1%	1	0	DIGIKEY	P0.0ECT-ND
Rs3	1206 SMD Film RED 1/4W 1%	1	3.74k	DIGIKEY	RHM3.74KFCT-ND
Rs4	1206 SMD Film RED 1/4W 1%	1	15k	DIGIKEY	RHM15.0KFCT-ND
Rs5, RSS	1206 SMD Film RED 1/4W 1%	2	3.9k	DIGIKEY	RHM3.90KFCT-ND
Rstart1, Rstart2, Rstart3	1206 SMD Film RED 1/4W 1%	3	270k	DIGIKEY	RHM270KFCT-ND
RT	1206 SMD Film RED 1/4W 1%	1	18k	DIGIKEY	RHM18.0KFCT-ND
Rvcc	1206 SMD Film RED 1/4W 5%	1	56	DIGIKEY	RHM56ERCT-ND
Rx1, Rx2	1206 SMD Film RED 1/4W 5%	2	4.7	DIGIKEY	RHM4.7ERCT-ND
TX	Resonant Power Transformer	1	ETD49	PRECISION INC	019-4974-00R
U1	IRS27951 Control IC	1		IR	IRS27951S
U2	Photocoupler TRANS-OUT 4-DIP	1	TLP621	DIGIKEY	TLP621FT-ND
U3	Programmable Voltage Regulator SOT23-3	1	TL431	DIGIKEY	296-17328-1-ND
W1	Jumper for Primary Current Sensing Loop	1			AWG22, multi strands

7.3 Typical Operating Waveforms

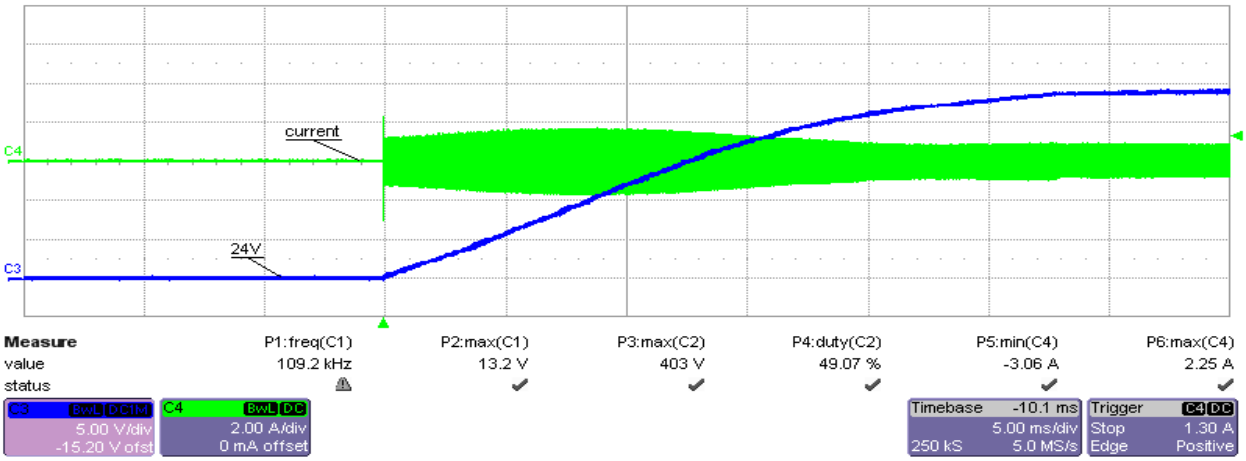


Figure 23 – 400Vdc input, 0W load startup

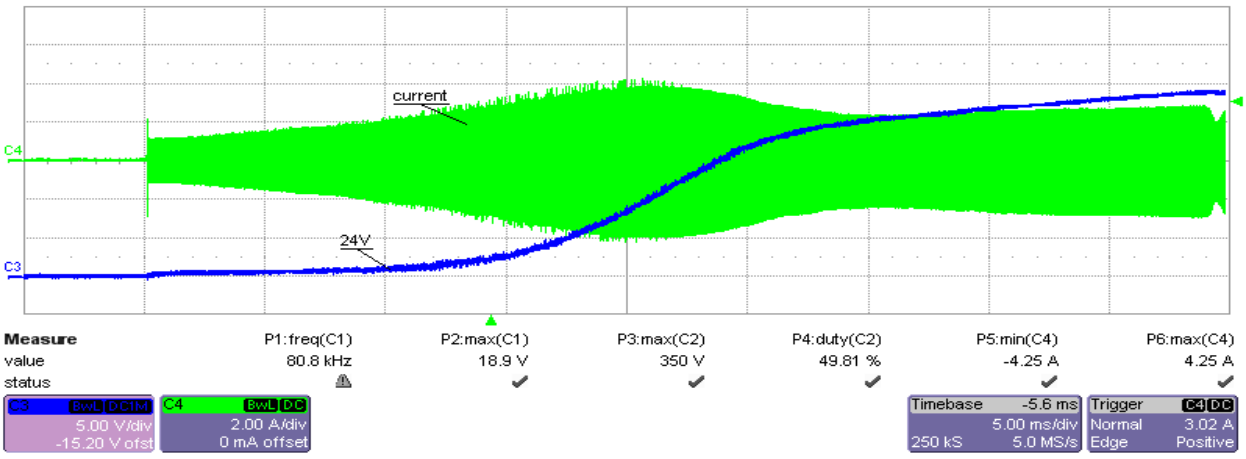


Figure 24 - 400Vdc input, 220W load startup

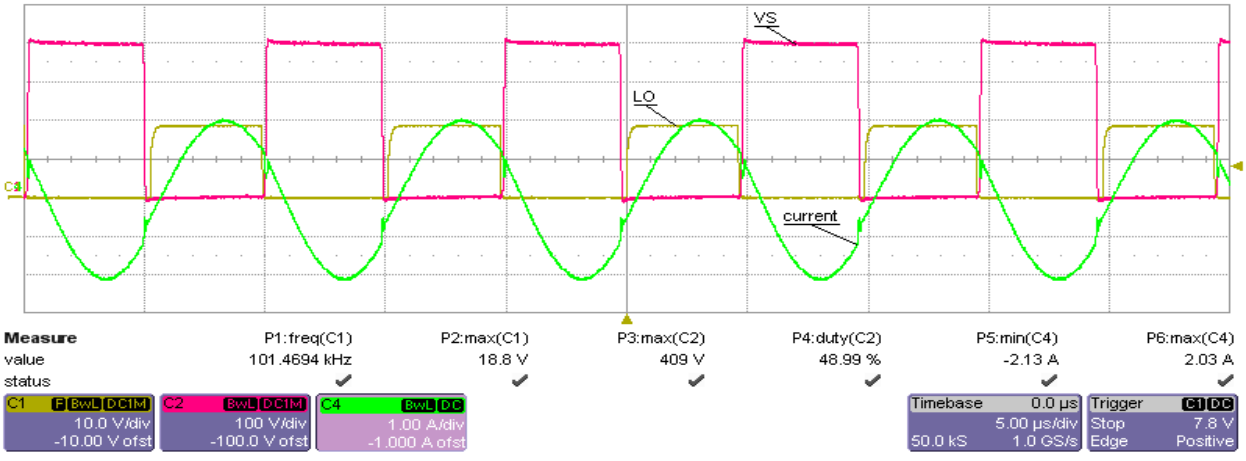


Figure 25 - 400Vdc input, 220W load operation

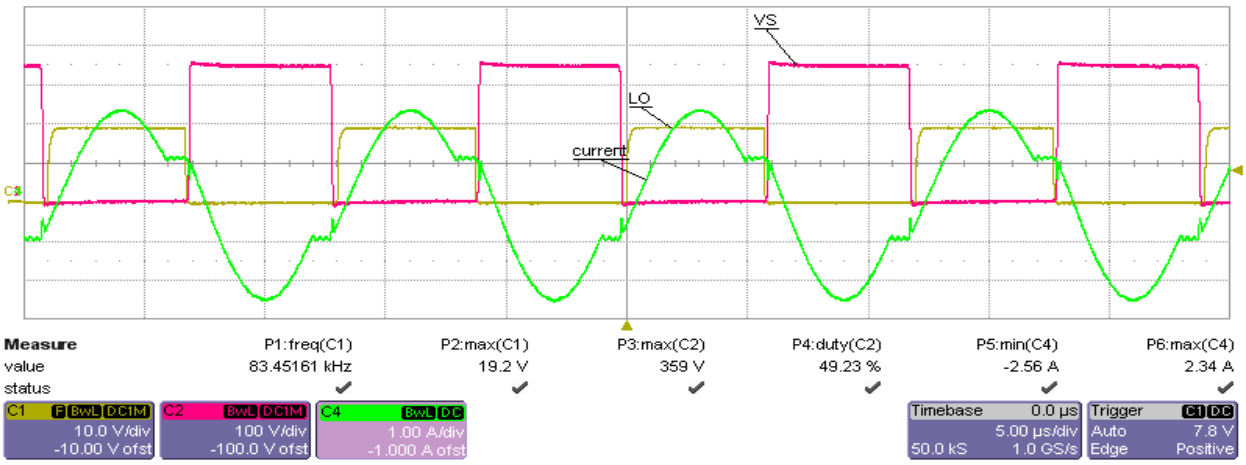


Figure 26 – 350Vdc input, 220W load operation

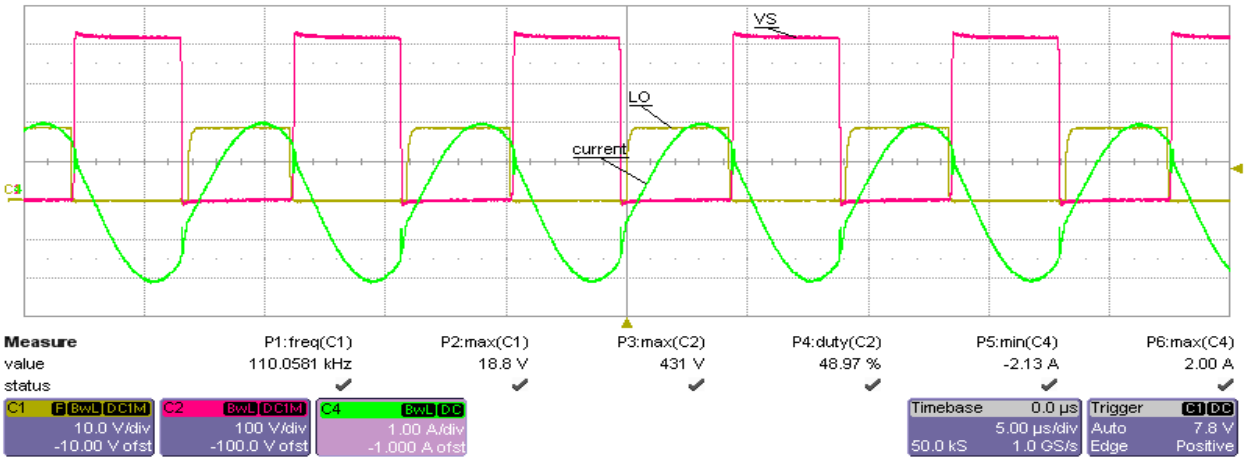


Figure 27 – 420Vdc input, 220W load operation

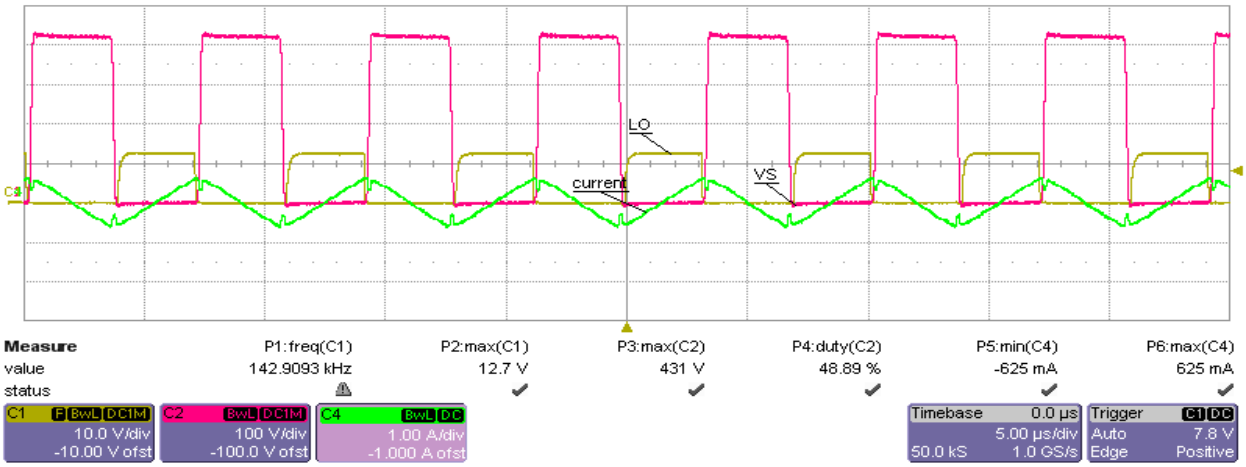


Figure 28 – 420Vdc input, 0W load operation

7.4 Short circuit protection

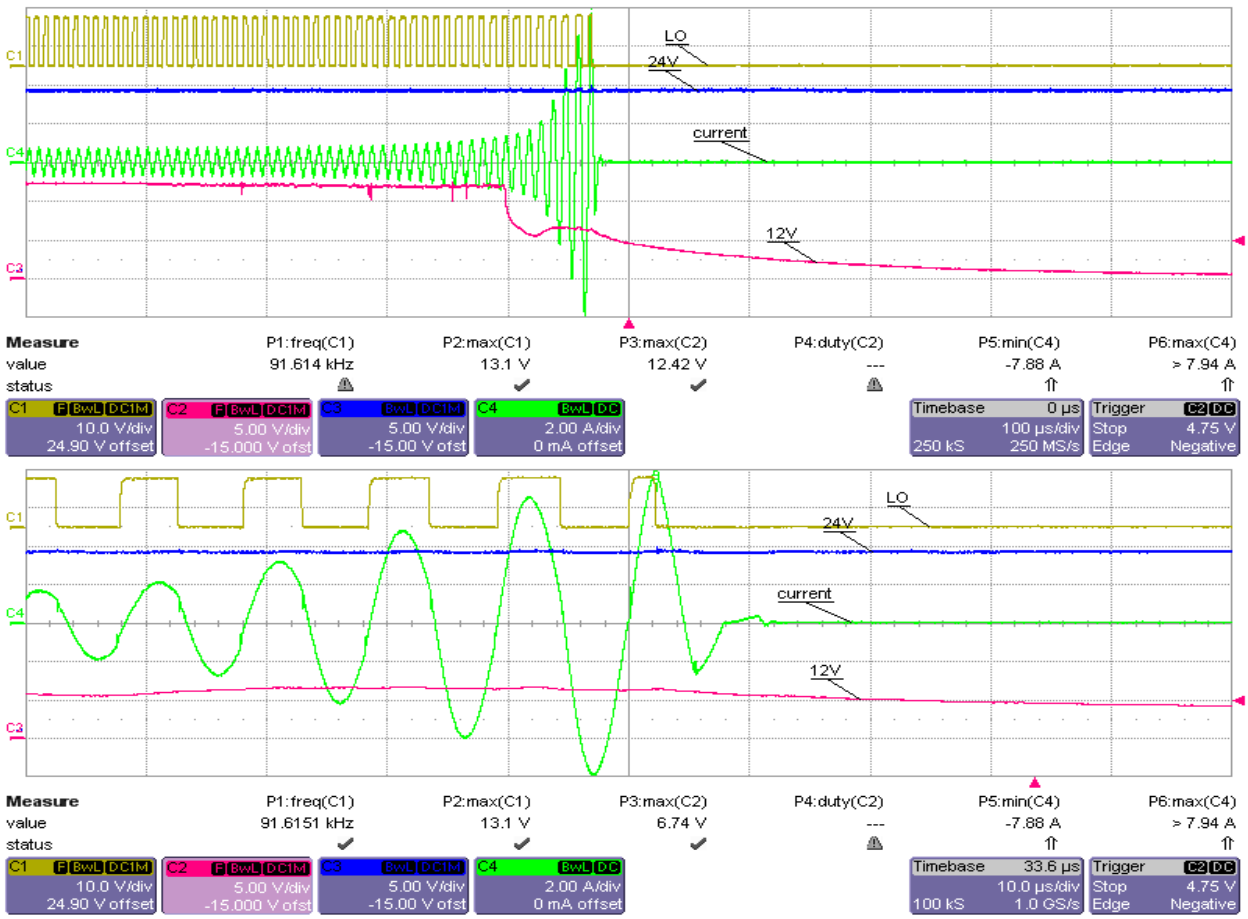


Figure 29 –260Vac input, short 12V, IC latched shut down

7.5 Efficiency

The average efficiency of the board at 25%, 50%, 75% and 100% load is 92% at 270Vac input:

					270Vac	400Vdc
24Vout	24V Iout(A)	12Vout	12V Iout(A)	Pout(W)	Efficiency	Efficiency
24.176	1.5	11.97	1.5	54.2	90.8%	91.0%
24.2	3	11.92	3	108.4	92.6%	92.6%
24.22	4.5	11.9	4.5	162.5	92.4%	92.9%
24.24	6	11.86	6	216.6	92.2%	92.7%
23.517	6	12.26	0	141.1	92.8%	
24.814	0	11.63	6	69.8	89.5%	

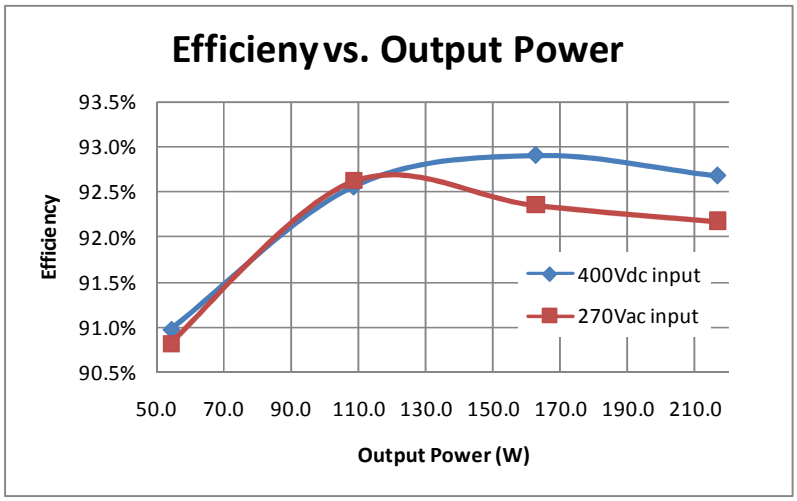


Figure 30 – Efficiency Plot

8. Layout guidelines and example

- **Ground Plane:**

In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

- **Gate Drive Loops:**

Current loops behave like antennas and are able to receive and transmit EM noise. In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. For the low-side driver, the return of the drive loop must be directly connected to the COM pin of the IC and separate with signal ground (power ground and signal ground have star connection at COM pin).

- **Supply Capacitor:**

It is recommended to place a bypass capacitor (CVCC) between the VCC and COM pins. A 1µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

- **CBS Capacitor:**

The CBS capacitor should be placed as close as possible to the VB and VS pins.

- **Routing and Placement:**

1) The 8-pin IC has only one COM pin for both signal return and power return, so it is strongly recommended to route the signal ground and power ground separately with a star connection at the COM pin.

2) The RT pin provides a current reference for the internal oscillator and needs to be kept as clean as possible to avoid frequency jittering or duty-cycle mismatch between high-side and low-side. The components connected to this pin must keep away from the high frequency switching loop such as the gate driver loop and the VS node. The PCB traces connected to RT pin also need to be kept away from any switching node. The PCB traces connected to RT pin also need to be kept away from any switching node.

3) Connect CT capacitor directly to COM pin, don't share the return with any other signal ground.

- **Layout examples**

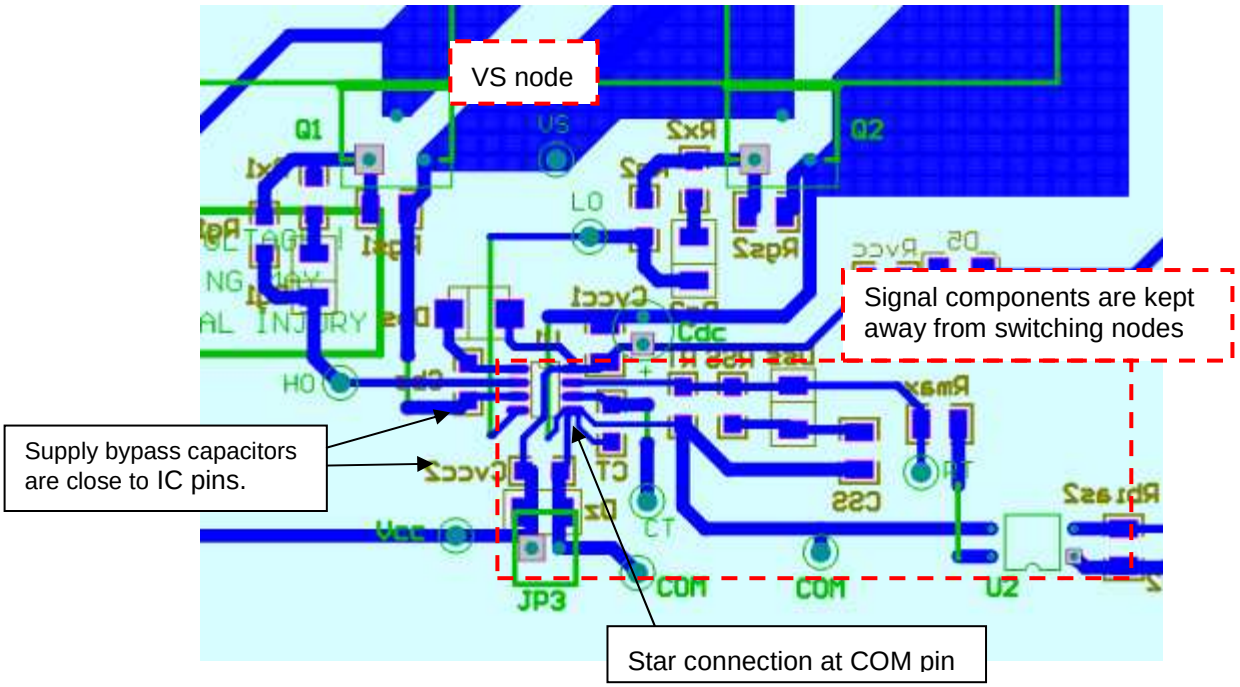


Figure 31: Single layer board example

9. Appendix

Symbols list

L_r: primary resonant inductance. It is the primary leakage inductance of transformer when there is no external added resonant inductor.

L_m: transformer primary magnetic inductance. It is the measured transformer primary inductance minus the leakage inductance.

C_r: primary resonant capacitor and DC blocking capacitor

f_{r1}: the resonant frequency between L_r and C_r

Rac: Equivalent AC resistance for resonant tank AC analysis

R_{DSon}: MOSFET channel ON resistance

f_{max}: converter maximum operating switching frequency
f_{min}: converter minimum operating switching frequency
Q_g: MOSFET total gate charge
Q_{gd}: MOSFET gate to drain (Miller) charge
Q_{gs}: MOSFET gate to source charge
I_{QCC}: IRS2795(1,2) quiescent current
R_g: MOSFET gate drive resistance external to IRS2795(1,2)
R_{up}: IRS2795(1,2) gate driver pull up resistance
R_{down}: IRS2795(1,2) gate driver pull down resistance
$R_{gFET:}$ MOSFET gate input resistance
P_{ICmax}: IRS2795(1,2) maximum power dissipation
V_{CC}: Supply voltage on IRS2795(1,2) Vcc pin
I_{CC}: IRS2795(1,2) IC supply current

References

[1] IRS2795(1,2) datasheet