Introduction

Compact fluorescent lamps (CFLs) are now replacing incandescent bulbs because of longer life time and energy saving. Most CFLs seen in the market are electronic ballast integrated CFLs. Due to the cost, these electronic ballasts don't include PFC circuit which typically requires additional control IC, inductor and switch, resulting in low power factor and high THD.

This application note describes a CFL ballast using valley fill passive PFC circuit and IR2520D ballast control IC. This ballast design achieves high power factor (>0.9), low THD (<30%) and regulated lamp current crest factor without typical active PFC circuit.
Functional Description

Valley Fill Passive PFC Circuit

Figure 1 shows the valley fill circuitry to achieve high power factor and low THD in simple and low cost.

![50% Valley Fill Passive PFC Circuit](image)

Fig. 1: 50% Valley Fill Passive PFC Circuit

The capacitors CVF1 and CVF2 are charged to \( \frac{1}{2} \) of the AC peak voltage in series via the diode DVF2 and resistor RVF on each half cycle of the rectified AC input. RVF is for reducing the peaks in the current waveform as the capacitors charge. They supply output current after the BUS voltage follows the sinusoidal waveform down to \( V_{\text{peak}}/2 \). At this time the caps are essentially in parallel an supply load current until the rectified AC input again exceeds \( V_{\text{peak}}/2 \) on the next half cycle. This valley fill passive PFC circuit presents good power factor (>0.9) and low THD (<30%), the major drawback is the 50% DC BUS ripple which result in a very high lamp current crest factor. (Fig.2)

The capacitor CX is for filtering the half-bridge inverter switching spikes which appears at DC BUS. Especially at the light load condition or at the peak of AC input, a big spike occurs at every switching cycle when switching frequency decreases towards resonance causing load voltage and current to increase as seen in Figure 3. Table 1 shows bigger CX cap value gives better filtering, but also decreases PF value.

![Half-Bridge Inverter Switching Waveforms](image)

Fig. 3: Half-Bridge Inverter Switching Waveforms

<table>
<thead>
<tr>
<th>CX value</th>
<th>Power Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.047uF</td>
<td>0.960</td>
</tr>
<tr>
<td>0.1uF</td>
<td>0.952</td>
</tr>
<tr>
<td>0.22uF</td>
<td>0.939</td>
</tr>
<tr>
<td>0.33uF</td>
<td>0.923</td>
</tr>
<tr>
<td>0.47uF</td>
<td>0.900</td>
</tr>
</tbody>
</table>

Table 1: PF Value vs. CX Value
Lamp Current Crest Factor Control Circuit

If the ballast operating frequency is fixed, 50% DC BUS ripple caused by valley fill circuit generates very high lamp current crest factor because higher DC BUS voltage gives higher lamp current in the resonant output stage. Since high lamp current crest factor shortens lamp life, a compensation circuit is required to decrease lamp current crest factor. Figure 4 shows the crest factor control circuit by modulating half-bridge inverter switching frequency when IR2520D is used for controlling the ballast.

Since IR2520D has VCO with externally programmable minimum frequency, half-bridge inverter switching frequency is determined by the voltage on VCO pin and the value of resistor connected to FMIN pin. (Please refer to the IR2520D datasheet for detail.) When DC BUS reaches a certain voltage, the voltage on the base of QFMIN connected to the voltage divider, which consists of RBUS1 and RBUS2, exceeds the QFMIN conduction threshold and then QFMIN turns on. At this case, the resistance between FMIN pin and ground becomes parallel RFMIN1 and series RFMIN2 and RFMIN3, which is lower than RFMIN1. Since lower resistance on FMIN pin gives higher switching frequency, the inverter switching frequency at near peak of the DC BUS is higher than at near valley of the DC BUS. As a result, crest factor value which is given by \( \frac{I_{LAMP(pk)}}{I_{LAMP(avg)}} \) will be decreased.

![Waveforms without crest factor control circuit](image1)

![Waveforms without crest factor control circuit](image2)

CF =1.95, half-Bridge (Upper), I LAMP (Mid), V LAMP (Lower)

Fig. 5: Waveforms without crest factor control circuit

CF =1.71, Half-Bridge (Upper), I LAMP (Mid), V LAMP (Lower)

Fig. 6: Waveforms without crest factor control circuit
The purpose of RFMIN3 is emitter degeneration for improving linearity. Without RFMIN3, QFMIN turns on quickly when the voltage on base of QFMIN reaches threshold. This causes lamp current shape distortion because of rapid operating frequency increase.

Electronic Ballast Design

Figure 11 shows the complete CFL ballast design. This ballast includes AC input stage with EMI filter, valley fill PFC stage, ballast control stage using IR2520D adaptive ballast control IC and lamp current crest factor control circuit, half-bridge inverter and resonant output stage.
Measurements

Table 2 shows measurement results. Following are the measurement conditions:
1. AC input: 200VAC to 260VAC
2. Lamp Type: 23W Spiral
3. Bill of Material

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Pin (W)</th>
<th>I in (mA)</th>
<th>PF</th>
<th>THD (%)</th>
<th>Lamp CF</th>
</tr>
</thead>
<tbody>
<tr>
<td>200VAC</td>
<td>19.7</td>
<td>97.3</td>
<td>0.965</td>
<td>25.8</td>
<td>1.62</td>
</tr>
<tr>
<td>220VAC</td>
<td>20.1</td>
<td>88.1</td>
<td>0.961</td>
<td>27.5</td>
<td>1.71</td>
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<tr>
<td>240VAC</td>
<td>21.4</td>
<td>85.4</td>
<td>0.959</td>
<td>28.5</td>
<td>1.78</td>
</tr>
<tr>
<td>260VAC</td>
<td>21.5</td>
<td>83.5</td>
<td>0.957</td>
<td>28.9</td>
<td>1.84</td>
</tr>
</tbody>
</table>

Table 2: Major Electrical Parameters

Conclusion

This application note suggests a CFL ballast circuit that achieves good power factor and low THD in cost effective way. The design includes low cost PFC stage and control stage using IR2520D 8-pin ballast control IC. Because of the simplicity of the ballast control method, total number of components used in this ballast is minimized, however, the design satisfies all of the necessary ballast features.