

# Application Note AN-1154

## Discrete Power Quad Flat No-Lead (PQFN) Inspection Application Note

### Table of Contents

	Page
Introduction.....	2
Inspection techniques.....	2
Visual inspection .....	2
X-ray inspection.....	2
Examples of well-mounted devices .....	3
Photographs .....	3
X-rays .....	3
Rejection criteria.....	4
Types of faults .....	4
Misalignment .....	4
Spatial and planar tilt.....	6
Loose components .....	6
Solder application.....	7
Solder balls and bridges.....	7
Solder voids.....	7
Poorly formed joints.....	8

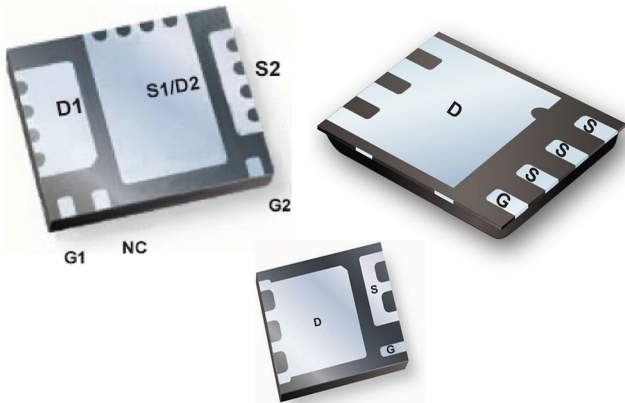
**NOTE:** For recommended substrate/PCB layouts and stencil designs, refer to [AN-1136](#).

The Discrete PQFN package family comprises efficient devices with a wide range of input voltages, all of which are lead-free as indicated by the PbF suffix after the part number (for example, [IRFH5300PbF](#)). There are various sizes and outlines. This application note explains the methods available for inspecting the quality of solder joints between device and PCB. It describes the types of problems that may arise in assembly.

## Introduction

This application note contains guidance on suitable inspection techniques for Power Quad Flat No-Lead (PQFN) devices. It considers the quality of solder joints between the device pads and printed circuit board (PCB). It also describes post-reflow alignments: how devices move and align themselves within pad tolerances once the solder has melted. Some devices move more than others, while some have excellent self-alignment, all arising from their device outlines.

PQFN devices vary but, typically, there are three electrical connections (gate, source and drain) but more mechanical joints (one gate pad, one or more source pads, and one or more drain pads). Figure 1 shows some examples.



*Figure 1 Bottom views of various PQFN packages (5x6 C, 5x6 B, 3x3 A)*

For information about the SupIRBuck™ PQFN, refer to [AN-1132](#) and [AN-1133](#).

## Inspection techniques

The design of PQFN devices demands different inspection methods from typical surface-mounted devices. As PQFN devices are bottom-terminated components (BTC), their pads are located on the underside and are difficult to see after mounting on a board. The PCB layouts and stencil designs recommended by International Rectifier in [AN-1136](#) provide the best possible access but the value of visual inspection is still limited. Only X-ray inspection provides a reliable indication of joint quality.

### Visual inspection

This is the simplest method to implement, requiring no additional equipment and being easy to automate. Although its use for PQFN devices is limited by their construction, viewing devices from the side can verify that proper solder joints have formed.

Visual inspection does not always detect poor electrical connections but it can confirm that devices are physically well-mounted. If the perimeter of a device does not have properly filled joints, the device may still be adequately mounted on the underside pad connection. This can occur when insufficient solder is applied to pool after reflow on the perimeter pads.

Inspection should focus on the joints underneath the device, rather than the connections visible on the sides of the device. These connections are sawn copper, exposed after separating devices from the sheets in which they are manufactured, and, unlike pads, are not plated to improve solderability. As any oxidation on the copper will impair solderability, there may be no solder fillets up the sides of a device even when the pad connections are well made.

### X-ray inspection

This is the only reliable way to verify that good electrical connections have been made. It reveals solder voids, planar tilts and poor joints caused by insufficient solder.

It is possible to implement sophisticated workflows that incorporate automated and even three-dimensional X-ray inspection. However, good results can be achieved by taking two-dimensional X-rays manually at the start of a manufacturing run and then at regular intervals during the run. If an automated system is used, the algorithms by which joint formation is evaluated must be suitable for leadless packages with proportionally large pads.

## Examples of well-mounted devices

### Photographs

The images in this section were taken at various stages of assembly: after solder placement on the PCB, after device mounting with a split-beam machine and after reflow. The split-beam machine has a placement accuracy of 0.005–0.006" but was set to skew devices by specific amounts to assess their limitations and behavior with recommended footprint/stencil designs.

Figure 2 shows properly filled solder joints running from the PCB pads towards the underside of the device pads.

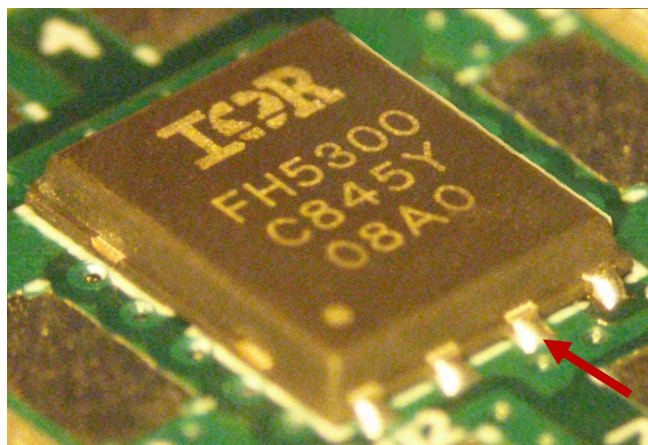


Figure 2(a) 5x6 B (IRFH5300PbF)

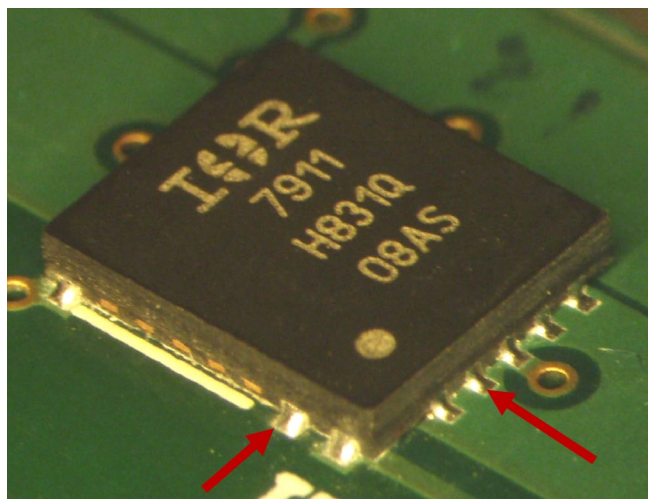


Figure 2(b) 5x6 C (IRFH7911PbF)

### X-rays

Figure 3 shows the solder joints between pads on the PCB and PQFN devices. Note the completely filled dark areas and the minimal voids.

The outlines of the device and its pads are highlighted in blue and green respectively. Their clearly defined shapes indicate proper solder flow and good electrical connections.

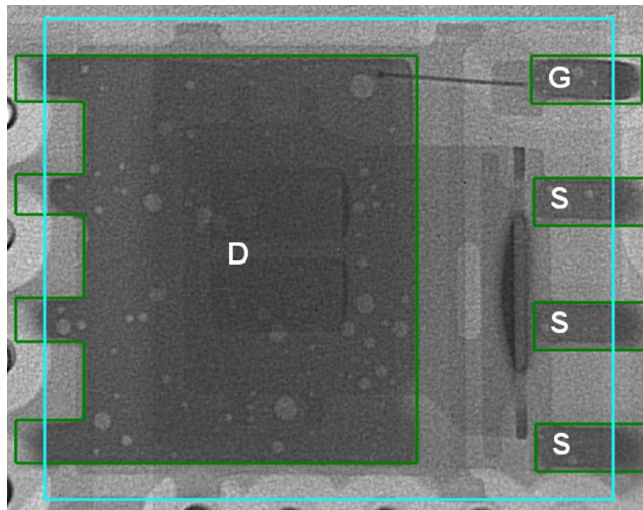


Figure 3(a) 5x6 B (IRFH5300PbF)

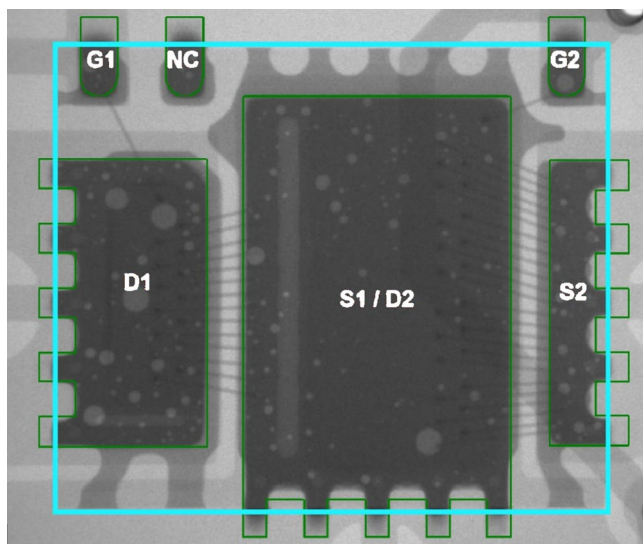


Figure 3(b) 5x6 C (IRFH7911PbF)



## Rejection criteria

The remaining sections of this application note explain the types of problems that can arise when board-mounting PQFN devices. In each case, criteria are given on which to base the decision whether to accept or reject a device. The table below summarizes these criteria and gives the number of the page on which you will find more information.

Observation	Reject any device that has:	Page
Misaligned device	Been turned through 180°	4
Twisted or tilted device	A gate or source pad with less than 75% solder coverage A drain pad with less than 50% solder coverage Been tilted by more than 3° relative to the PCB	5
Solder balling and bridging	A solder ball causing an electrical short A solder bridge linking electrically isolated points of the circuit (for example, between gate and drain pads not two drain pads)	7
Solder voiding	A solder joint with less than 75% coverage of the pad on the PCB	7
Poorly formed joints	A solder joint with less than 75% coverage of the pad on the PCB A missing or open solder joint	7

Note: Some of the problems shown in this document were deliberately created for illustrative purposes. They do not commonly arise in practice.

## Types of faults

### Misalignment

Although alignment is a vital factor to consider when using PQFN devices, the large pad areas on these devices can help to control post-reflow movement.

Figures 4 and 5 show the alignment of a device with a PCB footprint. The green lines in Figure 5 are PCB pads and match the silver blocks in Figure 4, while the blue lines are the device pads. As the green and blue lines overlap, the device and PCB footprint are exactly aligned. Even if the device is not placed optimally, adhesion forces pull it to align with the pad edge.

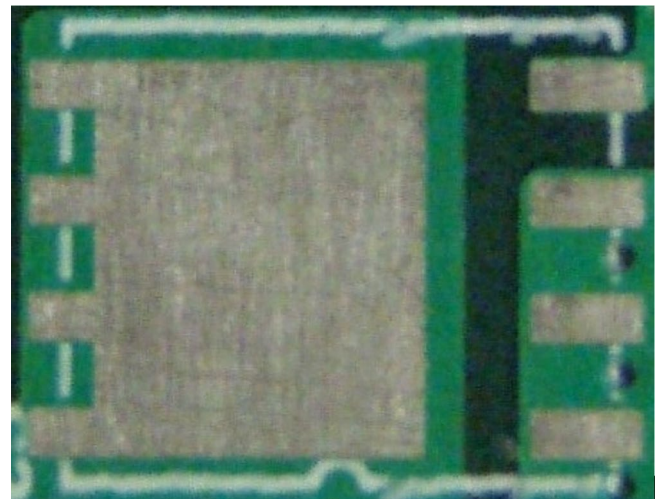


Figure 4 View of PCB footprint from Dutcard (silver)

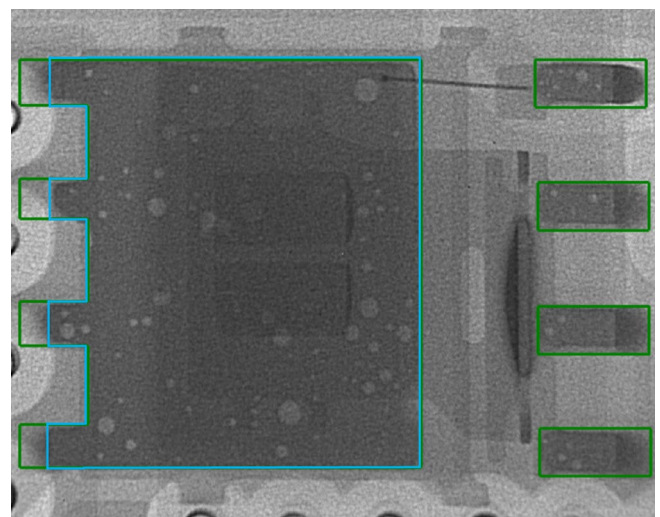


Figure 5 Alignment of device pad with PCB footprint

As the largest devices, the 5x6mm outlines have the largest pad areas. The C outline has three large pads that help to retain the device in position, providing a high degree of confidence in reliable, repeatable, accurate and problem-free placement. The B and E outlines have only one large pad area, causing these devices to align to one edge of the Drain pad.

Figures 6(a) and 7(a) show incorrectly placed devices, one to the right of the PCB pads and one to the top of the PCB pads. The former realigned itself during reflow, while the latter did not (Figures 9(b) and 10(b)).

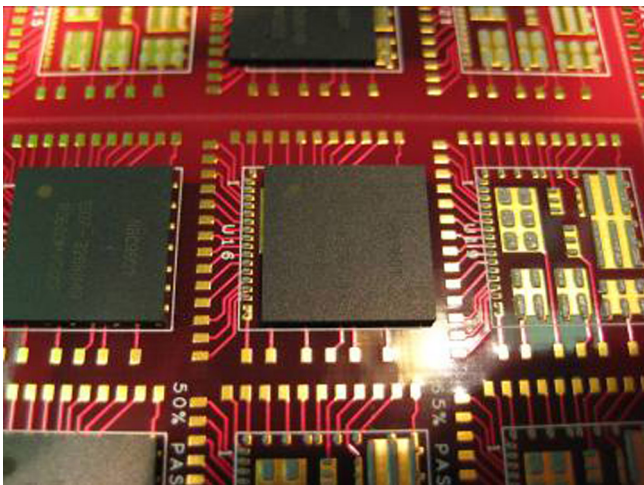


Figure 6(a) X-axis misalignment after placing

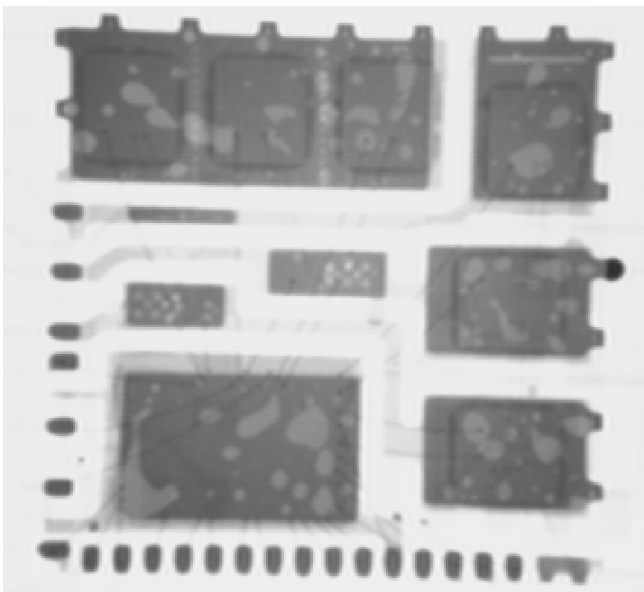


Figure 6(b) X-ray showing successful realignment

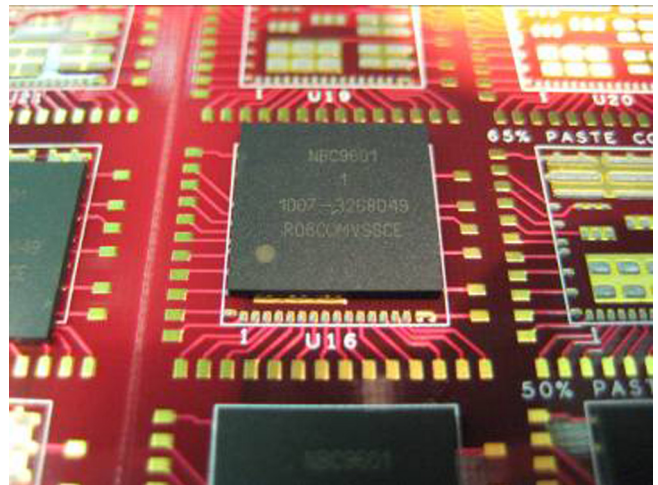


Figure 7(a) Y-axis misalignment after placing

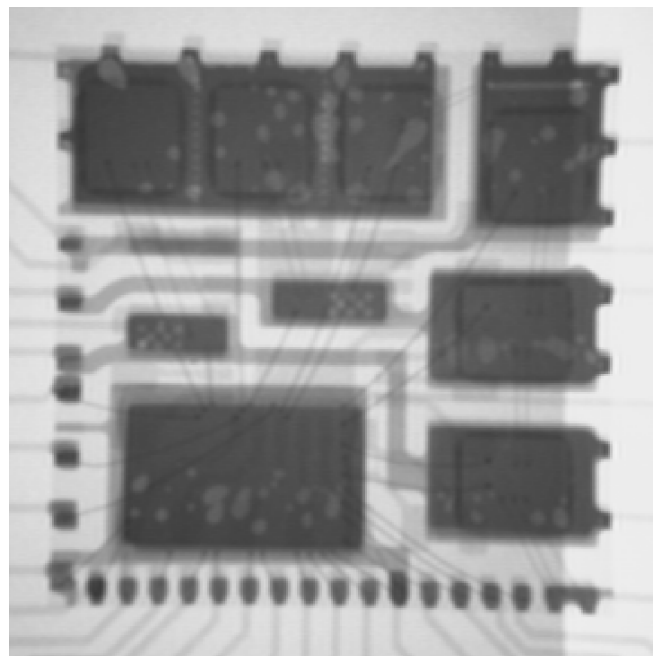


Figure 7(b) X-ray showing failure to realign

Such alignment features must be taken into consideration when designing PCB layouts and stencils. Using the designs recommended in Appendix A of [AN-1136](#) will avoid problems.



### Spatial and planar tilt

Spatial, or three-dimensional, tilt describes devices that are not parallel to the PCB because there is more solder under one edge than another.

Planar, or two-dimensional, tilt describes devices that are twisted when viewed from above, rather than being aligned with the edges of the PCB pad.

Figure 8(a) shows a device with planar tilt. The device did not realign itself during reflow (Figure 8(b)).

None of the samples in International Rectifier's tests showed spatial or planar tilt.

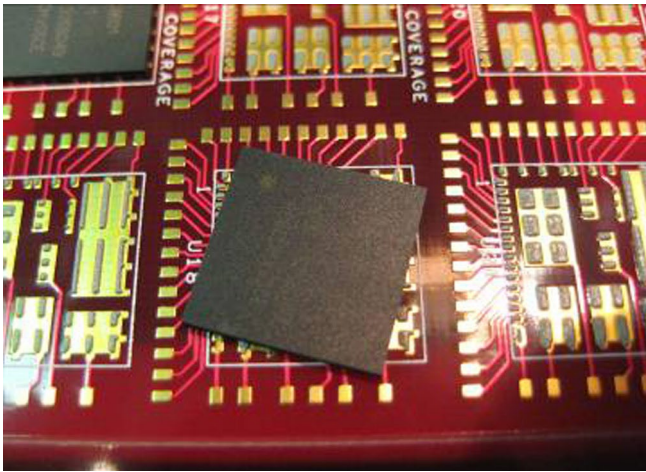


Figure 8(a) Planar tilt after placing

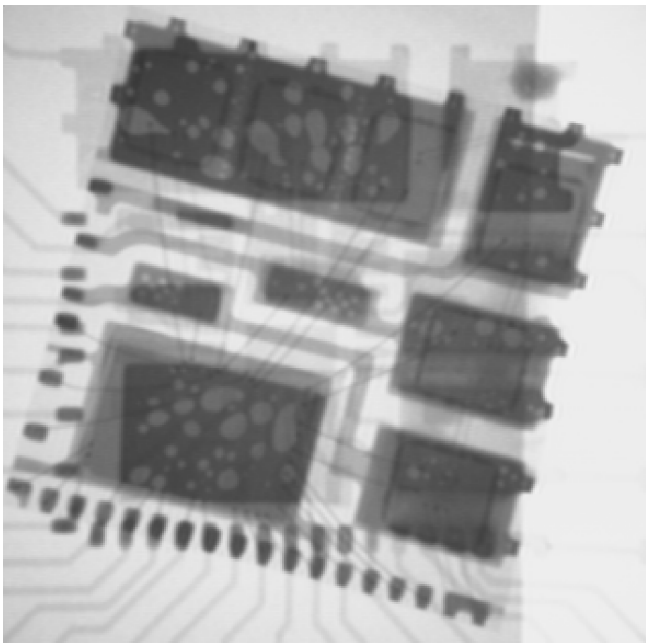


Figure 8(b) X-ray showing failure to realign

### Loose components

Components dropped during pick and place operations can be trapped under devices. Both visual and X-ray inspection can reveal such problems (Figures 9(a) and 9(b)).



Figure 9(a) Device place over a loose capacitor

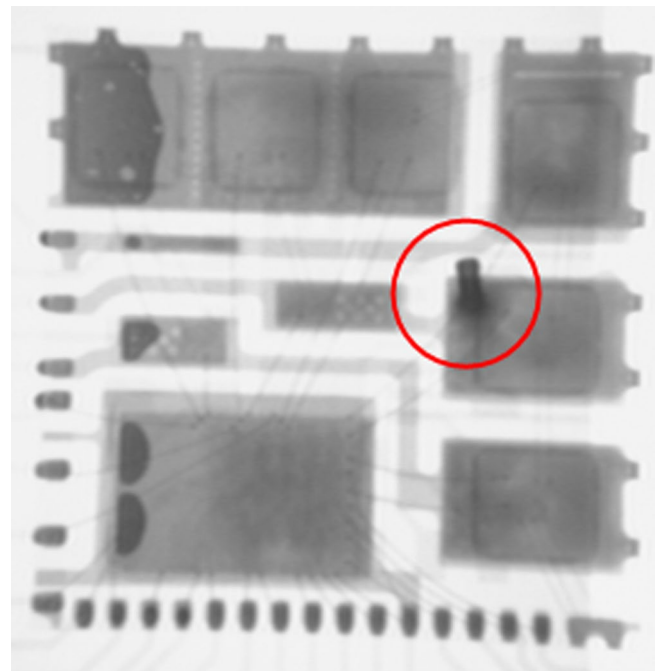


Figure 9(b) X-ray showing a loose capacitor

### Solder application

Correct stencil design is essential for proper solder connections. A design that puts down too little solder will cause poor solder joints and more voids (or open circuits, in extreme cases). A design that puts down too much solder will cause solder balls and bridges (or short circuits, in extreme cases). The recommended stencil designs gave good results under test.

Manual solder application requires care to ensure that solder is applied neatly and in sufficient quantity to prevent voids. When using the recommended PCB layouts, the direction of application (horizontal or vertical) is unimportant because even the smallest areas are large enough for solder to be properly deposited. Although the central S1/D2 pad on the 5x6 C outline has small legs, the recommended stencil design takes this into account and allows solder to be applied in either direction.

### Solder balls and bridges

Balls of excess solder and bridges of solder between the legs on devices can cause electrical shorts. Figure 10 shows these faults, both of which arise from applying too much solder.

There were no problems with solder balls and bridges in International Rectifier's tests and no short circuits were seen in any of the samples. Even where bridges formed initially, the leg spacing and large pads pulled the melted solder away and it adhered to the PCB pads adequately.

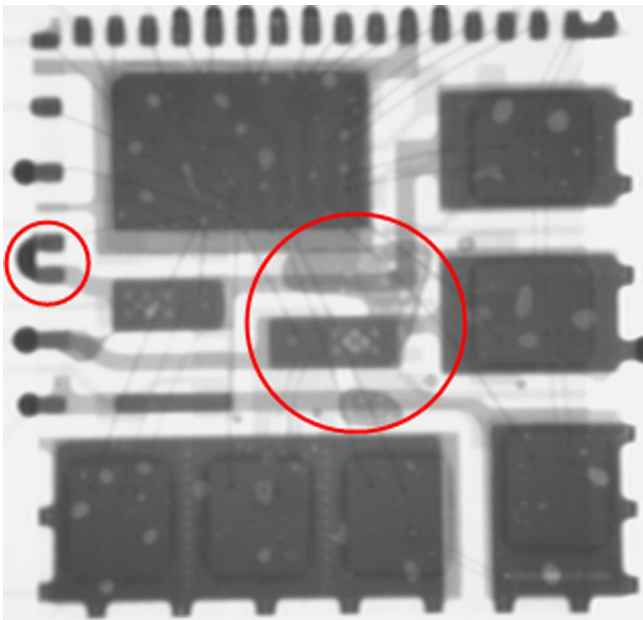


Figure 10 X-ray showing a solder bridge (left) and solder balls (centre)

### Solder voids

Solder voids inevitably occur when mounting devices but should be minimized. The IPC-A-610 standard requires the total void area to be less than 25%. Applying the correct amount of solder usually results in fewer voids but there are other factors: solder alloy, solder particle size, flux type and content variations (excess flux will increase the percentage of void area).

Figure 11 shows a device with voids in the solder joints exceeding 25%. This image was taken during void analysis for stencils of different thicknesses.

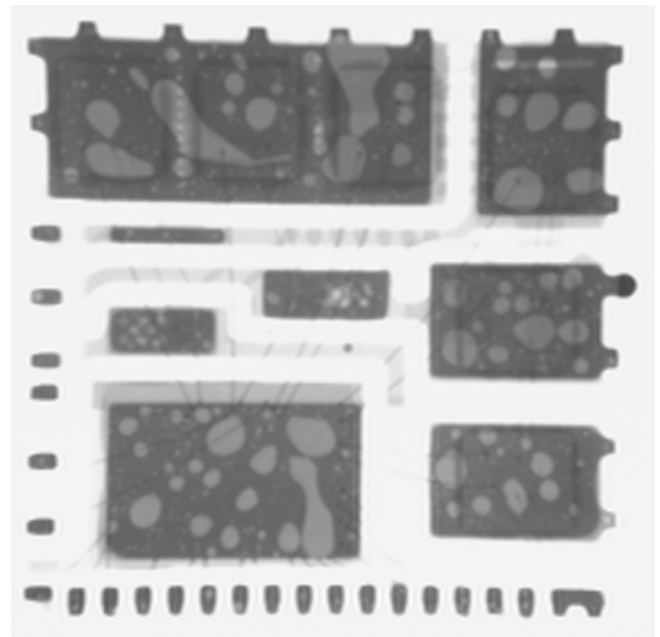


Figure 11 X-ray showing extensive voids

### Poorly formed joints

Poor joints differ from solder voids in that when the solder melted and flowed across the pad, there was not enough to reach the edges of the pad. Although the bare pad is still considered as a voided area, it doesn't have the characteristic circular appearance.

Figure 12 shows poor joints created deliberately during testing by removing half of the solder usually applied.

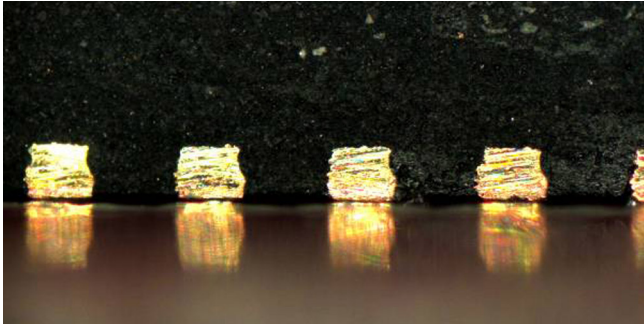


Figure 12 Insufficient solder on joints

Figure 13 shows open circuits on some pins, created deliberately during testing to demonstrate that X-ray inspection could detect such faults.

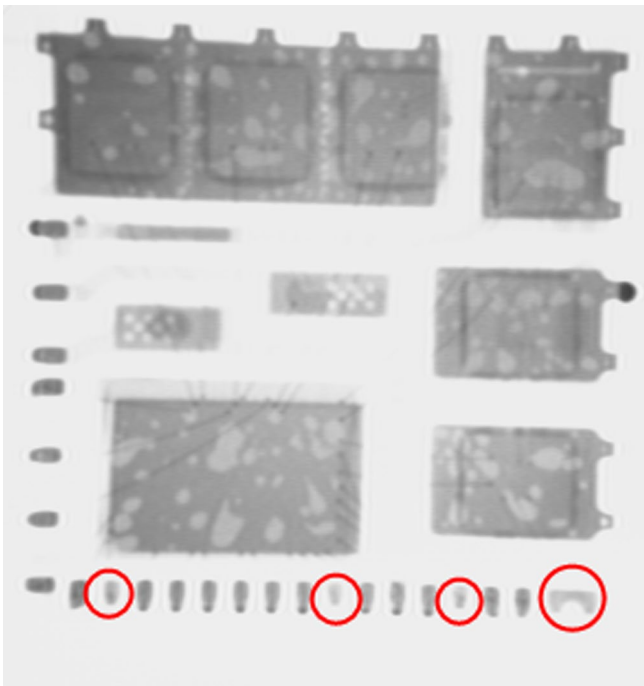


Figure 13 Open circuits on pins 2, 9, 13, 16 and 17

Figure 14 shows a voided area on the S2 pad of a device. As all five legs are internally connected to the leadframe, the fact that legs 4 and 5 are not fully connected externally may seem unimportant. However, it is unacceptable because there could be problems if a poorly connected leg was selected, for example, in an application that calls for sensing.

In conclusion, completely formed joints are sometimes essential. The typical circular voids are acceptable but only within standard limits.

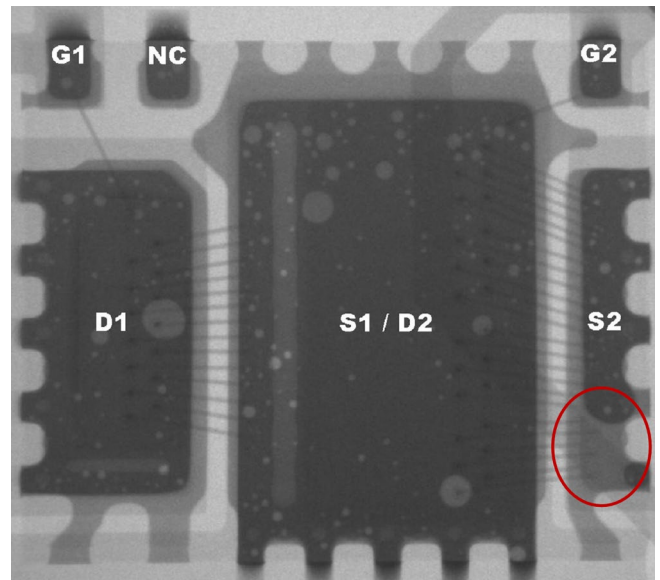


Figure 14 Insufficient solder applied, voided area impedes proper connection