Application Note AN-1152

Dual 5x6 Power QFN Technology Inspection and Footprint / Stencil Recommendation Application Note

By Behnia Barzegarian

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The Dual Power QFN is an efficient, single output power module with two Mosfets in a synchronous buck configuration, within a small Dual 5x6 Power QFN package. This package is offered only as Lead-Free (PbF), identified by a PbF suffix after the part number (for example, IRFH7911PbF). Per JEDEC JESD30E guidelines, the descriptive nomenclature is HV-PQFN/5x6, which stands for heat-spreader, very thin, plastic QFN 5 x 6 package. The main text of this application note contains guidance regarding the footprint and stencil design. Appendix A contains the device outline, footprint design, and stencil design for the Dual 5x6 PQFN package. To simplify board mounting and improve reliability, International Rectifier manufactures Power QFN devices to exacting standards. These high standards have evolved through evaluating many different materials and designs. Although such evaluations have yielded good results, the recommendations in this application note may need to be adjusted to suit specific production environments.

Introduction

Power QFN (PQFN) is a surface mount semiconductor technology designed primarily for board-mounted power applications. This includes the HEXFET Power MOSFET Silicon technology with the advanced PQFN packaging. This contributes both thermally and electrically, so that the package design has higher power capabilities than other comparable sized packages. See Figure 1 and 2 for package design. The gate pads were optimally designed to minimize gate tract lengths & allow for direct connections to the IC. The NC pad was intended to be a test pin, but was not implemented.

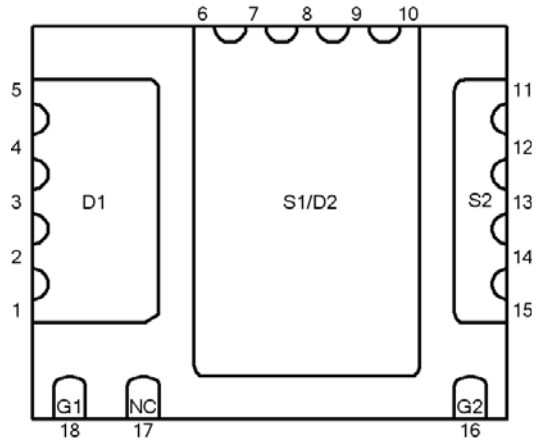

Figure 1 Dual 5x6 PQFN Bottom Contact Pads

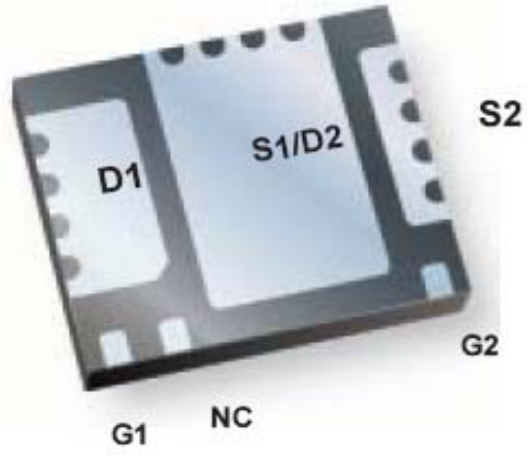

Figure 2 Bottom View of Dual 5x6 PQFN device

This design requires a different approach for inspection methods from typical surface - mounted devices (SMDs) like SO-8, for example. Verifying acceptable solder joint connections between the device pads and the pcb was achieved with x-ray microscopy (x-rays). The PCB layout was done so that a visual inspection could be administered as well. From a top view, the PQFN package design has the pads located on the underside of the device with no access to the pads via protruding legs like an SO-8 typically does. For this reason, the PCB Layout/ Footprint was designed to allow access to probe the pads once the device was mounted. This approach also allows for an additional, on-the-spot inspection that can be completed instantly upon mounting without any additional equipment except for the actual visual inspection. This is valuable because most of the verification will come from this type of fast and low-cost method rather than doing time-consuming x-rays. Optical inspection does not necessarily detect a poor solder connection. It *can* indicate an acceptable device mounting via a properly filled solder joint between the pcb and device pad. If the outside perimeter of the device does not show properly filled joints, the part may still be adequately mounted on the underside pad connection. This would occur if enough solder was not applied; then after reflow, did not pool on the external perimeter pcb pads for visual affirmation.

This application note reviews the quality of the solder joint between the pcb and device pads. Also, an important note often missed is post-reflow alignments. This is how the device moves and aligns itself within the pad tolerances once the solder has melted. This study included various placement skews from ideal to various degrees of erroneous placements. The included table shows a matrix of options and the results. For this study, x-rays and standard photos (via a microscope) were taken at each step: solder placement on pcb board, then after the devices were mounted via a split-beam machine (pre-reflow), and finally after the devices were reflowed (post-reflow). The split-beam machine allows for placement accuracy to within 5-6 mils. However, in this study, they were *accurately* skewed to define the limitations and behavior of the device using this footprint / stencil design.

Inspection Techniques

Two inspection techniques will be noted- visual inspection and x-ray inspection. The visual inspection will verify that a proper solder joint has formed. However, as noted above, an inadequate solder joint connection may not be an indicator of an inadequate solder connection underneath the pads. That would be verified with

the other inspection method, x-rays. This allows a defined picture of the solder connection to be seen between PCB pad and device pad. It provides information regarding solder voids, planar tilts, and if an adequate amount of solder was applied to cause poorly formed joints. Below are several acceptable examples.

Properly Mounted Device Examples

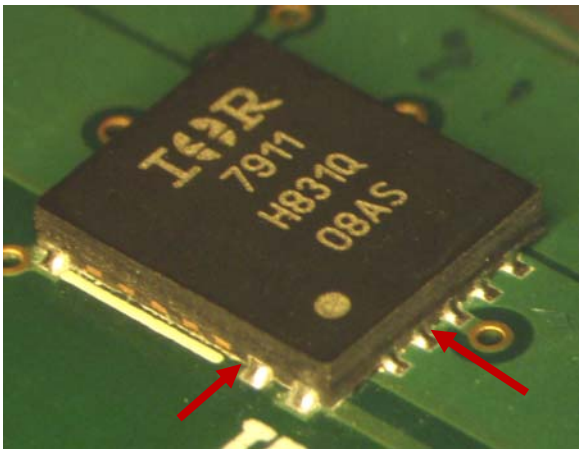

Figure 3 Standard Photo of Mounted Device

Pay particular attention to the proper solder joint from the PCB pad towards the underside of the device pad.

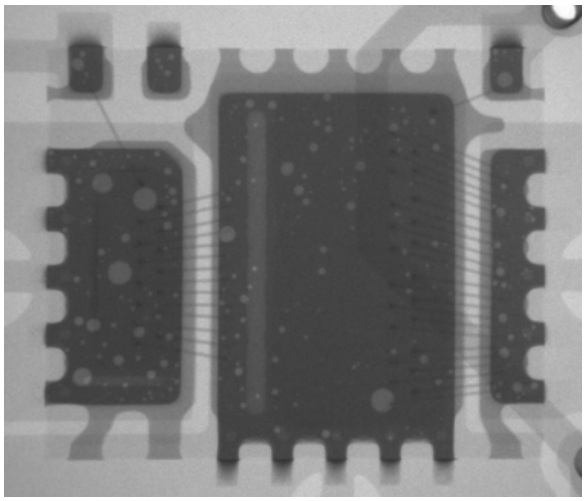

Fig. 4 Ideal X-Ray of properly mounted Device

Notice completely-filled dark areas and minimum void areas. These are the solder-connected areas between PCB and device pad. A clear definition of the area's shape indicates proper solder flow and connection. Next figure shows the area outlines for further clarification.

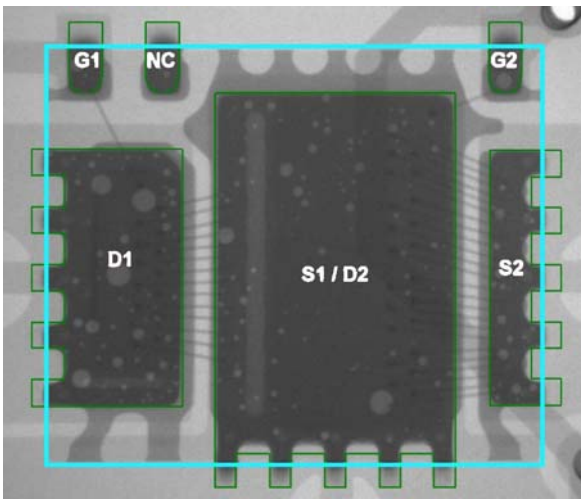

Figure 5 Details of Outlined areas

The blue line is the device outline. The green lines are the footprint design for the Drain 1 pad, Source 1 / Drain 2 pad, Source 2 pad, Gate 1, Gate2, and No Connect (NC) pad. The dark areas are the device pads (on the underside).

Mounting Skews and Results

Post-reflow, the alignments of 10 devices were exact carbon copies to dut#1 (note A1* below). The other devices, were slightly to the left by .020mm, which is <.8mil (noteA2* below). See Figure 8 and 9 on the following page.

dut#	solder applied	skew type	alignment
1	normal	Ideal	Good
2	normal	50% D below	A1*, like #1
3	poor	50% D below	A1*, like #1
4	poor	Ideal	A1*, like #1
5	normal	75% D below	A1*, like #1
6	normal	100% D below	A2*, .8mil off
7	normal	1 D pad below	A1*, like #1
8	normal	D Left edge align	A2*, .8mil off
9	normal	50% DS right	A1*, like #1
10	normal	Ideal	A2*, .8mil off
11	normal	S Right edge align	A1*, like #1
12	normal	50% G below	A2*, .8mil off
13	normal	Ideal	A1*, like #1
14	normal	hand mount	A2*, .8mil off
15	normal	hand mount	A1*, like #1

Table 1 Various Mounting Skews and Results

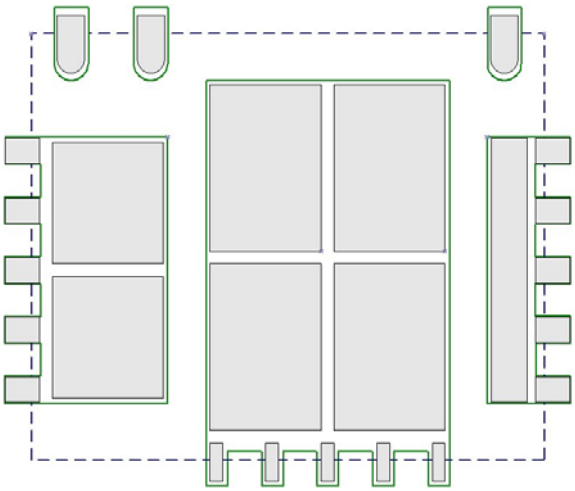

Figure 6 Drawing of Ideal Mounting, pre-reflow

Device is placed so that it is evenly spaced on the footprint (green lines) and stencil design (shaded grey areas). Device outline is the dotted line. Post-reflow result is seen in Figure 8.

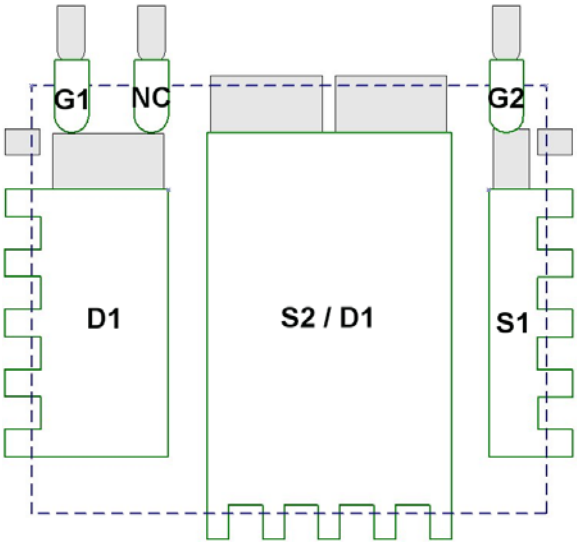

Figure 7 Drawing of skewed mounting (extreme), pre-reflow

In this example, the device is shifted one complete D1 leg down (dut#7). This is an extreme example of erroneous mounting just to evaluate alignment behavior. For this study, even more extreme placements were attempted with the same self-aligning positive results.

X-ray results of Fig 6 and 7 after reflow are the same as Figure 4 from above (or same as Figure 8). Only 1 picture is necessary because both device placements produced exactly the same alignments (as noted in Table 1 above).

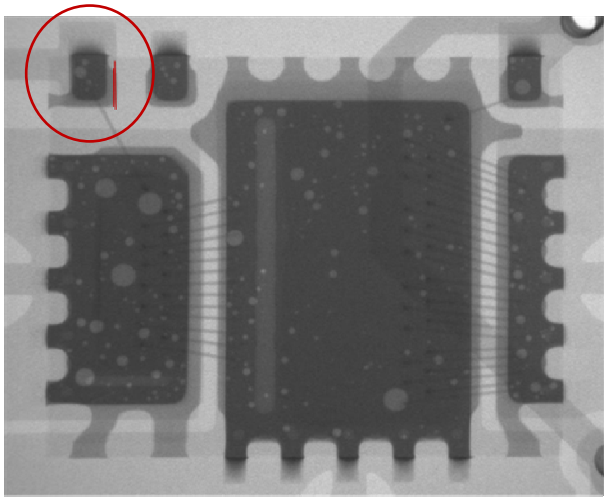

Figure 8 Ideal mounting (dut#13). Gate1 has .025mm (<1mil) spacing from pad edge (in red)

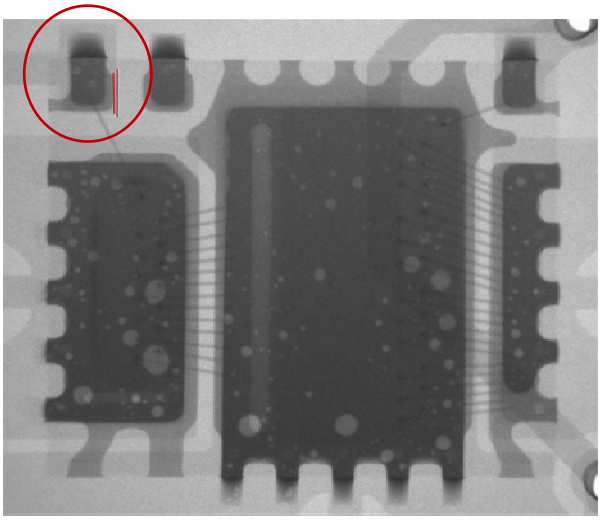

Figure 9 Skewed Mounting (dut #12). Gate1 has .045mm spacing from pad edge (in red).

Even with this extreme skew test, the part only had a placement difference by .020mm to the left, which is less than .8mil. This is virtually difficult to notice except with close examination & specifically looking for some difference. Even though the pre-reflow placement between the two are so different, the post-reflow placements are near identical and the slight differences do not have any affecting impact. This is the self-alignment feature of this device with the provided footprint design noted in Appendix A.

Observations for all of these devices showed clear definition of all the pads. However, the external perimeter of pcb pad extensions need more solder coverage, so that the solder flows

outside the device outline and becomes visible on the pcb board. This allows for confirmation of a good solder joint for the mounted device. The stencil design has been updated accordingly to accommodate for this need.

Description of Possible Concerns

Solder application via the stencil

Stencil design is crucial for proper solder connections. An insufficient design will not provide enough solder to allow for complete solder joints or increases solder voids. An overdesign will provide too much solder that can cause solder balling and shorting. The stencil provided has been tested and produced desirable results. Manual application should be done with care to ensure enough solder is applied neatly and to prevent voids. Depending on the direction of solder application, the deposited amount to the legs will be different. If solder is applied vertically (reference to Figure 10), then the correct amount of solder gets deposited for the S1/D2 legs, but the D1 and S2 legs will not be as clean. If the solder is applied horizontally, the D1 and S2 legs will have expected solder deposited, but the S1/D2 legs will appear to have very minimal solder. This is because the S1/D2 legs have small openings, making it more difficult for solder to completely fill the stencil openings. Though this may appear undesirable, the large S1/D2 pad has ample solder for coverage. Once melted, there is enough solder to adhere to the copper pad and spread to the legs. More solder will allow for an easier visual inspection, but samples have shown that the large pad itself provides enough solder to still pass a visual inspection. If possible, apply solder in the horizontal direction.

The two other large pads, D1 (on the left) and S2 (on the right), have smaller areas, plus the legs are larger. Thus, proper solder application is important here as well. To remedy any issues, the stencil design calls for these legs to be 100% (so footprint legs equals stencil legs, see Figure 6).

The gate pads are large enough and the stencil only has one rectangle. Thus, the solder melts uni-directional and there are no issues with solder coverage.

The end result is that the stencil design has been enhanced to remedy these issues so that ample solder will be deposited for any applied direction. This note is only mentioned to forewarn that slight imperfections will be seen during pre-reflow wet solder application and that it is of no concern because post-reflow x-rays show excellent solder definition and connectivity.

Solder Voids

Voids are related to the previous section. They are a normal occurrence during mounting devices, but within limits. The standards, specified in IPC-A-610, dictate that the total void area must be < 25%. If the appropriate solder amount was administered, there will generally be fewer voids. However, type of solder should be taken into consideration because excess flux will increase the percentage of void area. These samples were evaluated using lead pastes (Sn63 Pb37) and were within the standard limits.

Poorly formed joints

This is different from solder voids in that it is not a matter of voids in the area or from flux, but rather there was not enough solder so that when the solder melted and distributed across the pad, it did not reach the pad edges leaving them empty. This is still considered a voided area, but doesn't have the same characteristic circular appearance.

If enough solder is not applied, it may impede proper connection contributing to either solder voids or poorly formed joints. See Figure 10 on next page. The S2 pad has all 5 legs internally connected to the leadframe, so this voided area may seem to be of no concern if legs 4 and 5 are not fully connected externally. This is not acceptable because if the application calls for sensing, there would be issues if that leg was selected. Thus, completely-formed joints are vital at all times, but the typical circular voids are acceptable, within standard limits.

Again, the stencil has been enhanced to accommodate for this issue by making the vertical length and legs of the stencil for these pads 100%.

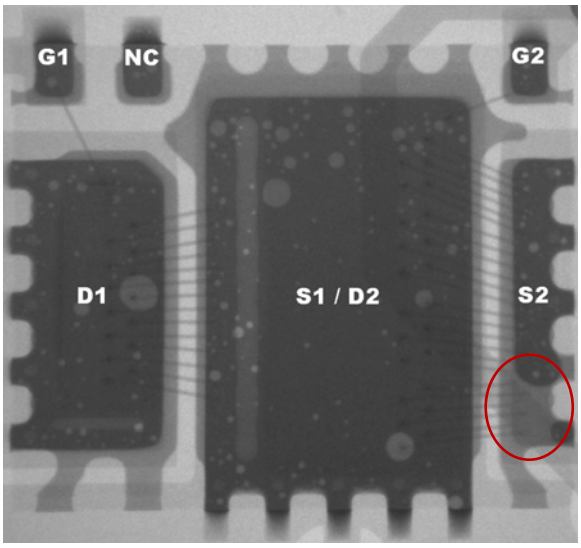

Figure 10 Not enough solder applied, voided area impedes proper connection.

Solder bridging between pads

This was not an issue when using these devices with the footprint / stencil provided. If too much solder is placed, the wet solder from two legs may combine to form one large lump. Once melted, the leg spacing and large pads would still pull the solder and adhere it to the PCB pads adequately. No shorting was seen in any of these samples.

Spatial and Planar Tilt

This was a small sample size, so issues that did not appear in the x-rays were still taken into consideration. None of the samples exhibit any spatial tilt. Spatial or 3D tilt looks at a side view of the device on the board and if it is virtually horizontal and evenly balanced vs tilted because there was more solder underneath one edge from another. These samples did not have tilt.

Another item to consider is Planar or 2D tilt, or where the device appears slightly twisted. Looking at a top view of the device, there is a slight tilt or twist instead of being vertically aligned to the pads. These samples did not show this for two reasons. One- the spacing on the PCB layout did not allow the device much room for tilting. Two- the various large device pads aligned and locked the device in the desired location (noted in the next paragraph).

One of the main items of concern was alignment. However, the various large pads help to lock the device to the same point repeatedly. Whether the device came from an extreme skew test, or from an ideal skew test, they both nearly aligned to the exact point. This was a very definite feature of this footprint / stencil design and can provide customer's with high confidence in a reliable, repeatable, accurate, and hassle-free placement. See figures below for details regarding the alignment considerations.

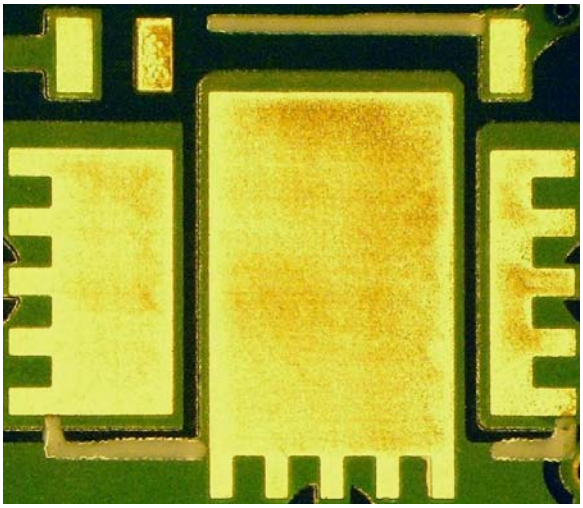

Figure 11 View of Actual Footprint layout from Dutcard (yellow)

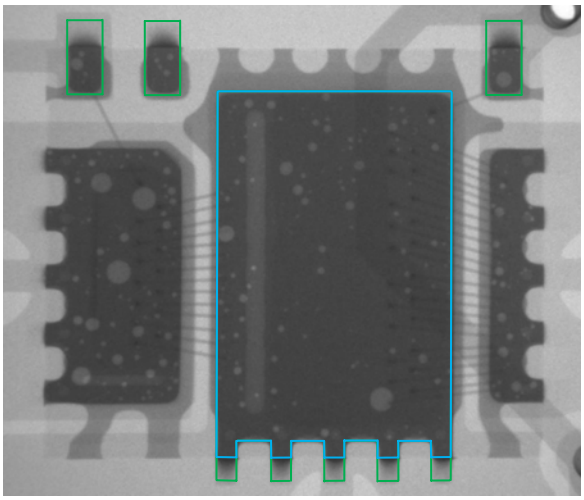

Figure 12 Alignment of Device's large pads to PCB pad edges

The green outlines are the PCB pads (footprint) and matches the yellow blocks in Figure 11. The blue lines are the pads from the device's bottom side. It can be seen that the device aligns exactly on the PCB footprint design as the green and blue lines are overlapping. Even if the part is not placed properly, the adhesion forces pull the drain to align to the Drain edge. For this

device, there are three large areas that cause this self-alignment to arrive at the same location with little variability.

Conclusions

The Footprint and Stencil design provided here in Appendix A are a recommendation and may need to be adjusted for your individual requirements. For the sample study conducted, these designs were found to be reliable for repeatable placement of the devices, helping the customer with hassle-free mounting.

Appendix A

This appendix contains the following information about the Dual 5x6 Power QFN Discrete device:

- Device Outline Drawing (per datasheet)
- Recommended PCB/ Footprint Layout
- Recommended Stencil Design

Device Outline

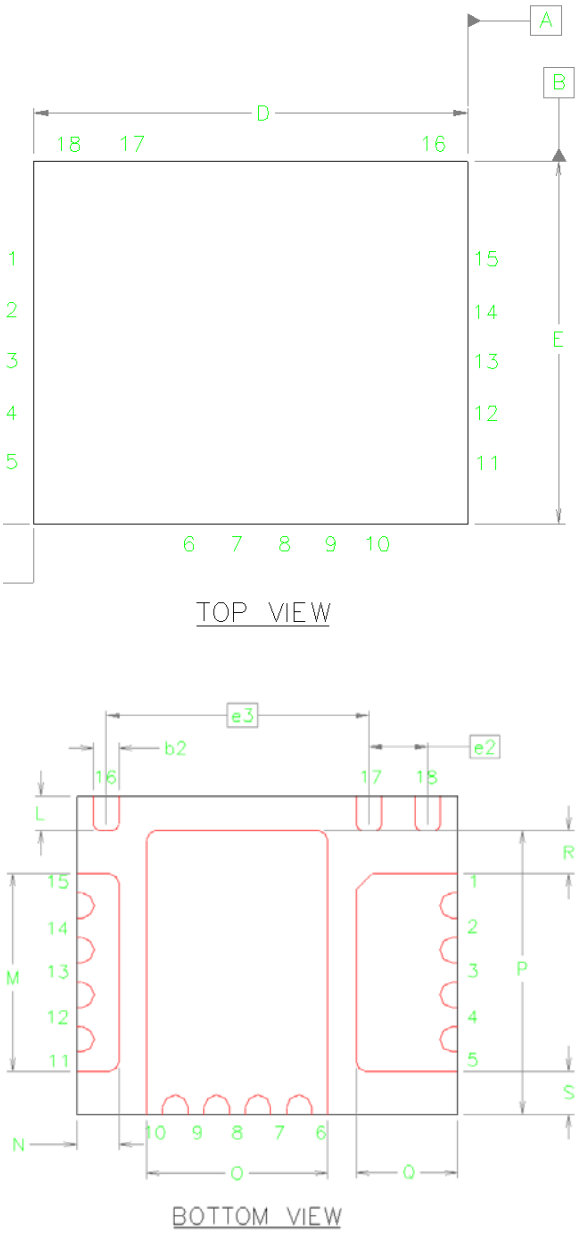

Figure A.1 Device Outline, Top and Bottom

Outline PQFN 5X6 C				
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0315	.0394	0.800	1.000
A1	.0000	.0020	0.000	0.050
b	.0098	.0138	0.250	0.350
b1	.0079	.0118	0.200	0.300
b2	.0138	.0177	0.350	0.450
c	.0080 REF.		0.203 REF.	
D	.2362 BASIC		6.000 BASIC	
E	.1969 BASIC		5.000 BASIC	
e	.0276 BASIC		0.700 BASIC	
e1	.0256 BASIC		0.650 BASIC	
e2	.0365 BASIC		0.926 BASIC	
e3	.1630 BASIC		4.140 BASIC	
L	.0197	.0236	0.500	0.600
M	.1201	.1240	3.050	3.150
N	.0243	.0282	.617	.717
Q	.1102	.1142	2.800	2.900
P	.1732	.1772	4.400	4.500
Q	.0607	.0647	1.543	1.643
R	.0266 REF.		0.675 REF.	
S	.0266 REF.		0.675 REF.	

Figure A.2 Device Outline Dimensions

Refer to relevant product datasheet for actual package outline drawing and dimensions.

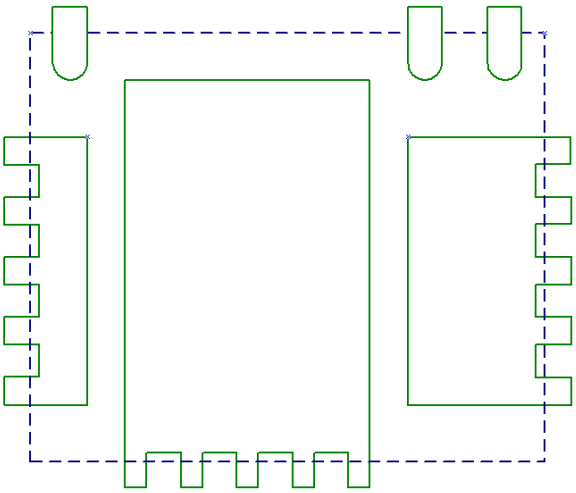

Figure A.3 Footprint Recommendation

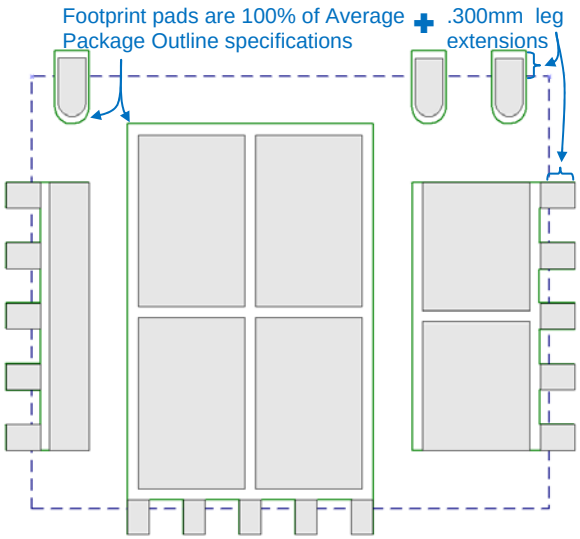

Figure A.4 Overall view of Footprint, Stencil and Device Outline

The footprint was designed to 100% package dimensions found in the above figures, plus extended each of the legs by .300 mm (shown in Figure A.4 above in blue). This would allow for verification of proper solder joint and for probing signals, if necessary.

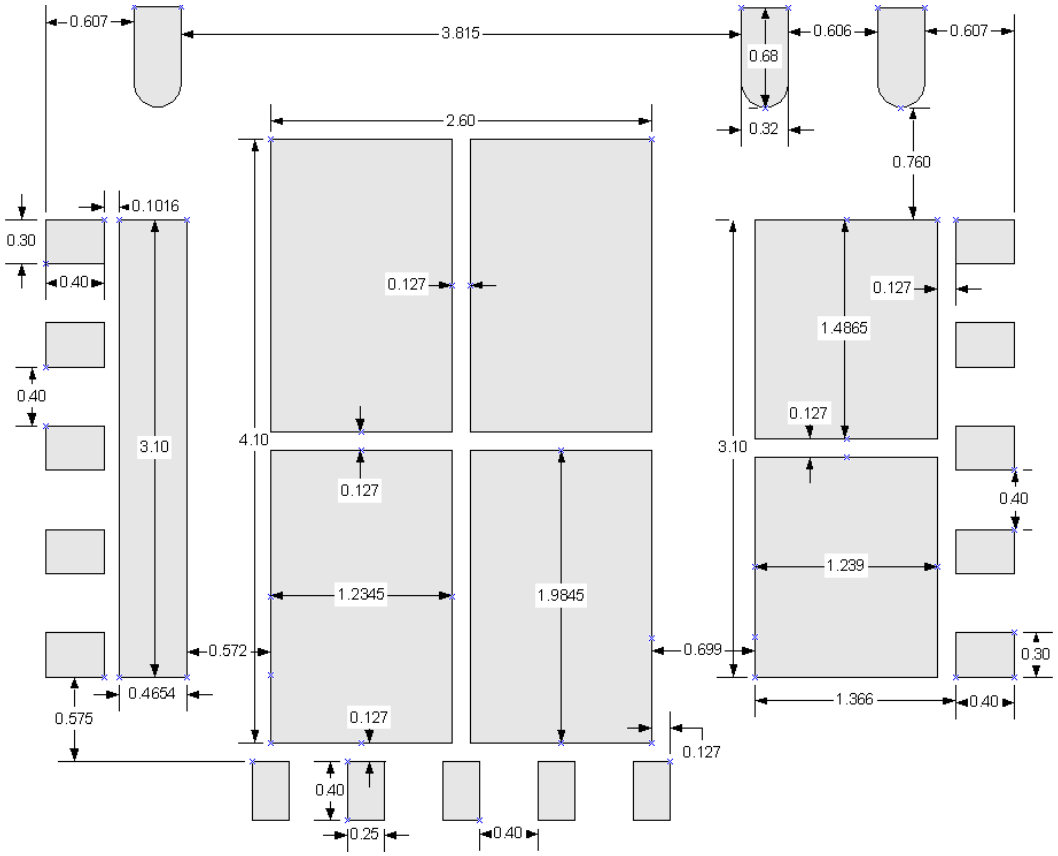

Figure A.5 Stencil design and dimensions

It is suggested that the stencil be applied at 5 mils thickness. Design was optimized to remove any concerns for insufficient solder to cause incomplete solder joints or excess solder voids, or concerns for direction of solder application. This design allows for solder to be applied in either direction.

Revision History

Date	Revision	Detail
7/14/09	-	Original Document posted online
8/26/09	1	Update figure A.4 & A.5 for stencil, include Revision History
12/19/09	2	Update figure 1

Table 2 Application Note revision history