International
IOR Rectifier

APPLICATION NOTE

Application Note AN-1150

Power Factor Correction using IR1152 Fixed Frequency CCM PFC IC

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Keywords: PFC, Power Factor Correction, THD.

1. Introduction

The IR1152 IC is a fixed 66kHz frequency PFC IC designed to operate in continuous conduction mode Boost converters with average current mode control. The IC is packed with an impressive array of advanced features such as programmable soft-start, micro-power startup current, user initiated micro-power Sleep mode for compliance with stand-by energy standards, ultra low bias currents for sensing pins. The fixed internal oscillator ensures stable operation at 66kHz switching frequency with very low gate jitter thus eliminating audible noise in PFC magnetics. In addition, the IC offers input-line sensed brown-out protection (BOP), “dual & dedicated” overvoltage protection, cycle-by-cycle peak current limit, open loop protection (OLP) and VCC under voltage lock-out (UVLO). All these features are offered in a compact 8-pin package making IR1152 the most feature-intensive IC for PFC applications. This application note provides an overview of IR1152 and demonstrates the design of a universal input 350W AC-DC Boost PFC Converter. Design & layout tips are also included.

2. IR1152 – Detailed Description

2.1 Overview of IR1152

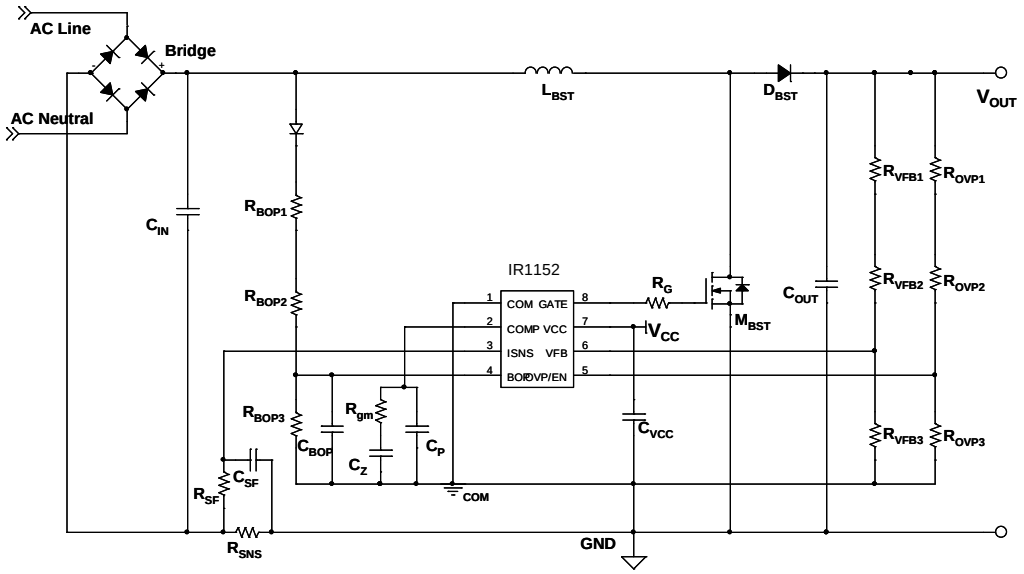

Fig.1: Typical application diagram of IR1152 based PFC converter

Fig.1 shows the system application diagram of the IR1152 based PFC converter. Only 3 pin functionalities - VFB, COMP & ISNS – are actually needed to obtain the necessary diagnostic signals to achieve power factor correction and maintain output voltage regulation. The functions of the abovementioned 3 pins are as follows:

- VFB – provides DC bus voltage sensing for voltage regulation
- COMP – used for compensating the voltage feedback loop to set the correct transient response characteristics
- ISNS – provides sensing of the inductor current, which is used to determine the PFC switch duty cycle

Essentially, there are 2 control loops in the PFC algorithm:

- a slow, outer voltage loop whose function is to simply maintain output voltage regulation
- a fast inner current loop whose function is to determine the instantaneous duty cycle every switching cycle

The current shaping function i.e. power factor correction is achieved primarily by the current loop. The voltage loop is responsible only for controlling the magnitude of the input current in order to maintain DC bus voltage regulation.

2.2 Key Features of IR1152

❖ *Fixed 66kHz Frequency Internal Oscillator*

IR1152 features a fixed frequency internal oscillator running at 66kHz. The gate drive pulse is completely free of jitter and this greatly enables elimination of audible noise in PFC magnetics due to magnetostriction. Also internalization of the oscillator greatly improves noise immunity of the IC.

❖ *Programmable soft-start*

IR1152 facilitates programmability of system soft-start time thus allowing the designer enough freedom to choose the converter start-up times appropriate for the application. The soft start time is the time required for the V_{COMP} voltage to charge through its entire dynamic range i.e. 0V through $V_{COMP,EFF}$. As a result, the soft-start time is dependent upon the component values selected for compensation of the voltage loop on the COMP pin – primarily the C_Z capacitor (described in detail in *Soft-Start Design* section of PFC Converter Design portion of this document). As VCOMP voltage rises gradually, the IC allows a higher and higher RMS current into the PFC converter. This controlled increase of the input current contributes to reducing system component stress during start-up. It is clarified that, during soft-start, the IC is capable of full duty cycle modulation (from 0% to MAX DUTY), based on the instantaneous ISNS signal from system current sensing. Furthermore, the internal logic of the IC is designed to ensure that the soft-start capacitor is discharged when the IC enters the Sleep or Stand-by modes in order to facilitate soft-start upon restart.

❖ *User initiated micro-power sleep mode*

The IR1152 has an ENABLE function embedded in the OVP/EN pin. When this pin voltage is actively pulled below V_{SLEEP} threshold, the IC is pushed into the

Sleep mode where the current consumption is less than 75uA even when V_{CC} is above $V_{CC,ON}$ threshold. The system designer can use an external logic level signal to access the ENABLE feature since V_{SLEEP} threshold is so low. The IR1152 internal logic ensures that V_{COMP} is discharged before the IC enters Sleep mode in order to enable soft-start upon resumption of operation.

❖ *Protection features*

The IR1152 features a comprehensive array of protection features to safeguard the system. These are explained below.

1. "Dual & Dedicated" Overvoltage protection (OVP)

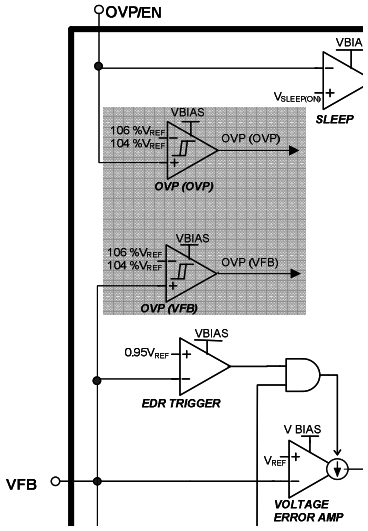

Fig.2: IR1152 Overvoltage Protection Scheme (dual & dedicated)

There are 2 overvoltage comparators in IR1152 – the OVP(OVP) and OVP(VFB) comparators. Both are identical in operation and also in terms of the overvoltage trigger and release thresholds. The OVP(OVP) tracks the OVP/EN pin while the OVP(VFB) tracks the VFB pin for output voltage information.

An overvoltage fault is triggered when either one or both of the pin voltage exceeds the V_{OVP} threshold of 106%V_{REF}. The IC gate drive is immediately disabled and held in that state. The overvoltage fault is removed and gate drive re-enabled only when both pin voltages are below the $V_{OVP,RST}$ threshold of 103% V_{REF}. The tandem operation of the 2 comparators lends 2 important aspects to the overvoltage protection feature in IR1152 that is not afforded by any competitor, 8-pin PFC ICs:

- Dedicated OVP protection- The OVP pin is a dedicated pin for overvoltage protection that safeguards the system even if there is a break in the VFB feedback loop due to resistor divider failure etc.
- Dual OVP Protection- Each comparator acts as a watchdog for the other. Under abnormal failure situations such as pin-to-pin shorts, if for any reason

one of the comparator misbehaves, the other comparator still provides overvoltage protection.

Since the VFB pin which programs the DC bus regulation voltage through the voltage error amplifier also features an overvoltage comparator with 106%V_{REF} threshold, this effectively fixes the system maximum overvoltage protection level at 106% of the nominal regulation voltage level. Though a lower level of overvoltage protection can be set through the dedicated OVP pin, care must be taken to avoid setting the protection threshold too low. A lower overvoltage protection threshold could cause the OVP reset threshold lower than 100% of the nominal output voltage, which may trigger multi OVP protections during startup. Thus it is recommended to set the overvoltage protection threshold to the default 106%$V_{REF.}$ In another word, the voltage divider that connected to OVP pin should use the same value as the VFB voltage divider.

2. Open-Loop protection (OLP)

The open-loop protection ensures that the IC is restrained in the Stand-by mode if the VFB pin voltage has not exceeded or has dropped below V_{OLP} threshold of 19%V_{REF}. In the Stand-by mode, all internal circuitry of the IC are biased, the gate drive is disabled and current consumption is a few milliamps. During start-up, if for some reason the voltage feedback loop is open then IC will remain in Stand-by and not start thus avoiding a potentially catastrophic failure.

3. Brown-Out protection (BOP)

IR1152 provides brown-out protection based on direct sensing of AC input line. Information about the rectified AC input voltage is communicated to the BOP pin after scaling it down using a resistor divider network and filtering using a capacitor on BOP pin. During start-up, the IC is held in Stand-by mode when BOP pin voltage is less than $V_{BOP(EN)}$ threshold of 1.56V. When the pin voltage exceeds this threshold, the IC enters normal operation (assuming no OLP condition exists). Subsequently, if the pin voltage falls below V_{BOP} threshold of 0.76V during normal operation, then a brown-out fault is detected and IC is pushed into Stand-by mode. For the IC to exit Stand-by, the pin voltage has to exceed $V_{BOP(EN)}$ threshold again. In the Stand-by mode, all internal circuitry of the IC are biased, the gate drive is disabled and current consumption is a few milliamps.

4. Cycle-by-cycle peak current limit protection (IPK LIMIT)

The cycle-by-cycle peak current limit is encountered when V_{ISNS} pin voltage exceeds $V_{ISNS(PK)}$ threshold of -0.75V (in magnitude). When this condition is encountered, the IC gate drive is immediately disabled and held in that state until the ISNS pin voltage falls below $V_{ISNS(PK)}$. Even though the IR1152 operates based on average current mode control, the input to the peak current limit

comparator is decoupled from the averaging circuit thus enabling instantaneous cycle-by-cycle protection for peak current limitation.

5. V_{CC} UVLO

In the event that the voltage at the V_{CC} pin should drop below that of the VCC UVLO turn-off threshold, $V_{CC(UVLO)}$ the IC is pushed into the UVLO mode, the gate drive is terminated, and the turn on threshold, $V_{CC,\ ON}$ must again be exceeded in order to re start the process. In the UVLO mode, the current consumption is less than 75uA.

3. PFC Converter Design Procedure

3.1 PFC Converter Specifications

AC Input Voltage Range	85-264VAC
Input Line Frequency	47-63Hz
Nominal DC Output Voltage	385V
Maximum Output Power	350W
Power Factor	0.99 @ 115VAC/350W 0.99 @ 230VAC/350W
Minimum Output Holdup Time	25ms @ $V_{OUT,MIN}$=285V
Maximum Soft Start Time	60msec

Table 1: Design Specifications for PFC Converter

3.2 Power Circuit Design

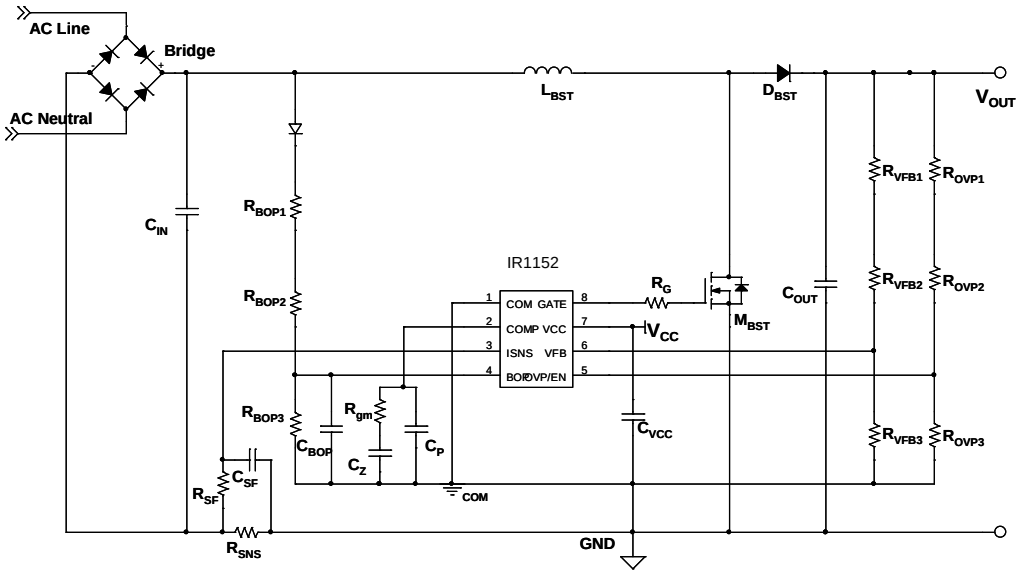

Fig.3: IR1152 based PFC Boost Converter

❖ *Peak Input Current*

It is necessary to determine the maximum input currents (RMS & peak) from the specifications in Table 1 before proceeding with detailed design of the PFC boost converter. The maximum input current is typically encountered at highest load & lowest input line situation (350W, 85VAC). Assuming a nominal efficiency of 92% at this situation, the maximum input power can be calculated:

$$P_{IN(MAX)} = \frac{P_{O(MAX)}}{\eta_{MIN}} = \frac{350W}{0.92} = 380W$$

From this, the maximum RMS AC line current is then calculated:

$$I_{IN(RMS)MAX} = \frac{P_{O(MAX)}}{\eta_{MIN}(V_{IN(RMS)MIN})PF}$$

$$I_{IN(RMS)MAX} = \frac{350W}{0.92(85V)0.998} = 4.5A$$

The selection of the semiconductor components (bridge rectifier, boost switch & boost diode) is based on $I_{IN(RMS)MAX}$ =4.5A.

Assuming a pure sinusoidal input, the maximum peak AC line current can then be calculated:

$$I_{IN(PK)MAX} = \frac{\sqrt{2}(P_{IN(MAX)})}{V_{IN(RMS)MIN}}$$

$$I_{IN(PK)MAX} = \frac{1.414(380W)}{85V} = 6.3A$$

❖ *Boost Inductance (L_{BST})*

IR1152 IC is an average current mode controller. An on-chip RC filter is sized to effectively filter the boost inductor current ripple to generate a clean average current signal for the IC. The averaging function in the IC can accommodate a maximum limit of 40% inductor current ripple factor at maximum input current. The boost inductance has to be sized so that the inductor ripple current factor is not more than 40% at maximum input current condition (at peak of AC sinusoid). This is because:

- Higher ripple current factors will interfere with the Average Current Mode operation of One Cycle Control algorithm in IR1152 leading to duty cycle instabilities and pulse skipping which results in current distortion and sometimes even audible noise
- power devices are stressed more with higher ripple currents as the peak inductor current ($I_{L(PK)MAX}$) also increases proportionately

In this calculation, an inductor current ripple factor of 35% is selected (typical ripple factor is ~20% for most PFC designs). The ripple current at peak of AC sinusoid at maximum input current is:

$$\Delta I_L = 0.35 \times I_{IN(PK)MAX}$$
$$\Delta I_L = 0.35 \times 6.3A = 2.2A$$

And, peak inductor current is:

$$I_{L(PK)MAX} = I_{IN(PK)MAX} + \frac{\Delta I_L}{2}$$
$$I_{L(PK)MAX} = 6.3A + \frac{2.2A}{2}$$
$$I_{L(PK)MAX} = 7.4A$$

In order to determine the boost inductance, the power switch duty cycle at peak of AC sinusoid (at lowest input line of 85VAC) is required.

$$V_{IN(PK)MIN} = \sqrt{2} \times V_{IN(RMS)MIN} = 120V$$

Based on the boost converter voltage conversion ratio,

$$D = \frac{V_O - V_{IN(PK)MIN}}{V_O}$$
$$D = \frac{385V - 120V}{385V} = 0.69$$

The boost inductance is then given by:

$$L_{BST} = \frac{V_{IN(PEAK)MIN} \times D}{f_{SW} \times \Delta I_L} = \frac{120V \times 0.69}{66kHz \times 2.2A}$$
$$L_{BST} = 570\mu H$$

A convenient value of 600µH is selected for L_{BST} for this converter which will result in an inductor ripple current factor between 30-35%.

❖ *High Frequency Input Capacitor (C_{IN})*

The purpose of the high-frequency capacitor is to supply the high-frequency component of the inductor current (the ripple component) via the shortest possible loop. This has the advantage of acting like an EMI filter, since it minimizes the high-frequency current requirement from the AC line. Typically a high-frequency, film type capacitor with low ESL and high-voltage rating (630V) is used.

High-frequency input capacitor design is essentially a trade-off between:

- sizing it big enough to minimize the noise injected back into the AC line
- sizing it small enough to avoid line current zero-crossing distortion (flattening)

The high-frequency input capacitor is determined as follows:

$$C_{IN} = k_{\Delta I_L} \frac{I_{IN(RMS)MAX}}{2\pi \times f_{SW} \times r \times V_{IN(RMS)MIN}}$$

$$C_{IN} = 0.35 \frac{4.5A}{2\pi \times 66kHz \times 0.09 \times 85V}$$

$$C_{IN} = 0.496\mu F$$

where:

$k_{\Delta IL}$ = inductor current ripple factor, of 35% as mentioned earlier

r = maximum high frequency input voltage ripple factor ($\Delta V_{IN}/V_{IN}$), assumed 9%

A standard 0.470µF, 630V capacitor is selected for C_{IN} for this converter.

❖ Output Capacitor (C_{OUT})

Output Capacitor design is based on hold-up time requirement

For 25ms hold-up time and minimum output voltage of 285V the output capacitance is first calculated:

$$C_{OUT(MIN)} = \frac{2 \cdot P_O \cdot \Delta t}{V_O{}^2 - V_{O(MIN)}{}^2}$$

$$C_{OUT(MIN)} = \frac{2 \cdot 350W \cdot 25ms}{(385V)^2 - (285V)^2}$$

$$C_{OUT(MIN)} = 261\mu F$$

Minimum capacitor value must be de-rated for capacitor tolerance (20%) to guarantee minimum hold-up time.

$$C_{OUT} = \frac{C_{OUT(MIN)}}{1 - \Delta C_{TOL}} = \frac{261\mu F}{1 - 0.2} = 326\mu F$$

A standard 330µF, 450V capacitor is selected for C_{OUT} for this converter.

3.3 IR1152 Control Circuit Design

3.3.1 Current Sense Resistor Design (ISNS pin)

In IR1152, there are two levels of current limitation:

- a “soft” current limit, which limits the duty-cycle and causes the DC bus voltage to fold-back i.e. droop
- a cycle-by-cycle “peak” current limit feature which immediately terminates gate drive pulse once the ISNS pin voltage exceeds $V_{ISNS,PEAK}$

❖ “Soft” Current Limit

In IR1152 the COMP pin voltage is directly proportional to the RMS input current into the PFC converter i.e. V_{COMP} is higher at higher RMS current. Clearly its magnitude is highest at maximum load P_{MAX} & minimum AC input voltage, $V_{IN,MIN}$. The dynamic range of V_{COMP} in the IC is defined by $V_{COMP,EFF}$ parameter in the IR1152 datasheet. Once V_{COMP} signal saturated (reaches $V_{COMP,EFF}$), any system requirement causing an additional increase in current will cause the IC to respond by limiting the duty cycle and thereby causing the output voltage to droop. This is called “soft” current limit protection. The selection of R_{SNS} must ensure that “soft” current limit is not encountered at any of the allowable line and load conditions.

❖ R_{SNS} Design

The design of R_{SNS} is performed at the system condition when the inductor current is highest at lowest input line ($V_{IN,MIN}$) and highest load (P_{MAX}). Further, the inductor current is highest at the peak of the AC sinusoid. The duty cycle required at peak of AC sinusoid at $V_{IN,MIN}$=85VAC in order to regulate V_{OUT}=385V is:

$$D_{PEAK} = \frac{V_{OUT} - \sqrt{2}V_{IN(RMS)MIN}}{V_{OUT}}$$

$$D_{PEAK} = \frac{385V - \sqrt{2}.85V}{385V} = 0.69$$

R_{SNS} design should guarantee that

i. PFC algorithm can deliver this duty cycle at peak of AC sinusoid at $V_{IN,MIN}$ & P_{MAX} condition
ii. soft current limit is encountered whenever there is a further increase in demand for current while operating at $V_{IN,MIN}$ & P_{MAX} condition

To do this, the V_{ISNS} is calculated below.

$$V_{ISNS(MAX)} = \frac{V_{COMP(EFF)(MIN)} \cdot (1 - D)}{g_{DC}}$$

$$V_{ISNS(MAX)} = \frac{4.7V \cdot (1 - 0.69)}{3.1} = 0.47V$$

Note: if the calculated $V_{ISNS(MAX)}$ is higher than the cycle-by-cycle peak overcurrent limit specification of the IC, the $V_{ISNS(PK)}$ value should be used to determine R_{SNS}. In this example, $V_{ISNS(MAX)}$ is lower than 0.68V $V_{ISNS(PK)(MIN)}$ thus 0.47V is used for R_{SNS} calculation.

Peak Current Limit Protection ISNS Voltage Threshold (IPK LIMIT)	$V_{ISNS(PK)}$	-0.82	-0.75	-0.68	V	Bias on ISNS pin

Next the peak inductor current at maximum peak AC line current, derated with an overload factor (K_{OVL}=10%), is calculated.

$$I_{IN(PK)OVL} = I_{L(PK)\max} \cdot (1 + K_{OVL})$$

$$I_{IN(PK)OVL} = 7.4 \times 1.1 = 8.2A$$

From this maximum current level and the required voltage on the current sense pin, we now calculate the maximum resistor value that can be used for the PFC converter.

$$R_{SNS,MAX} = \frac{V_{SNS(\max)}}{I_{IN(PK)OVL}} = \frac{0.47V}{8.2A}$$

$$R_{SNS,MAX} = 0.057\Omega$$

It is noted that even though IR1152 operates in average current mode it is still safer to use the peak inductor current for current sense resistor design to guarantee avoiding premature fold-back.

Power dissipation in the resistor is now calculated based on worst case RMS input current at minimum input voltage:

$$P_{R_S} = I_{IN(RMS)MAX}^{\ 2} \cdot R_S$$

$$P_{R_S} = 4.5^2 (0.057\Omega) = 1.2W$$

A standard 50mΩ resistor can be selected for R_{SNS} for the PFC converter.

❖ Peak Current Limit

The cycle-by-cycle peak current limit is encountered when V_{ISNS} pin voltage exceeds $V_{ISNS,PEAK}$. For the PFC converter, this limit is encountered whenever the inductor current exceeds the following:

$$I_{PK\_LMT} = \frac{|-.75V|}{0.05\Omega} = 15A$$

It is clarified that even though the IR1152 operates based on average current mode control, the input to the peak current limit comparator is decoupled from the averaging circuit thus enabling instantaneous cycle-by-cycle protection for peak overcurrent.

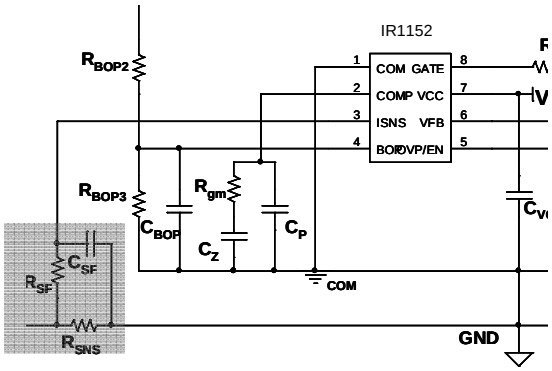

Fig 4: Current Sense Resistor and Filtering

The current sense signal is communicated to the ISNS pin of the IC using a current limiting series resistor, R_{SF}. An external RC filtering for ISNS pin can be realized (though not necessary for IR1152) by adding a filter capacitor, C_{SF} between the ISNS pin and COM as shown in Fig.4. A corner frequency around 1-1.5MHz will offer a safe compromise in terms of filtering, while maintaining the integrity of the current sense signal for cycle-by-cycle peak overcurrent protection.

$$f_{PSF} = \frac{1}{2\pi \cdot R_{SF} \cdot C_{SF}}$$

With R_{SF}=100Ω, we can use C_{SF}=1000pF to obtain a cross-over frequency of 1.6MHz. The input impedance of the current sense amplifier is approximately 25KΩ. The R_{SF} resistor will form a divider with this 25KΩ resistor. For R_{SF}=100Ω it is noted that the accuracy of the current sense voltage signal communicated to the IC is more than 99.5%.

3.3.2 Output Regulation Voltage Divider (VFB pin)

The output regulation voltage of the PFC converter is set by voltage divider on VFB pin - R_{FB1}, R_{FB2}, and R_{FB3}. The total impedance of this divider network must be high enough to reduce power dissipation, but low enough to keep the feedback voltage error (due to finite bias currents into the voltage error amplifier which is less than 0.2uA) negligible. Around 2MΩ is an acceptable value for the total resistor divider impedance.

A standard 1MΩ, 1% tolerance resistor is selected for R_{FB1} & R_{FB2} for this converter. Then, R_{FB3} is determined based on error amplifier V_{REF} (Typ)=5V and V_{OUT}=385V converter specification.

$$R_{FB3} = \frac{V_{REF}(R_{FB1} + R_{FB2})}{(V_{out} - V_{REF})}$$

$$R_{FB3} = \frac{5.0V(2000k)}{(385\text{V} - 5.0\text{V})} = 26.3k\Omega$$

A standard resistor, R_{FB3} = 26.1kΩ, 1% tolerance, is selected for this converter.

The new regulation V_{OUT} value based on actual resistor values is then calculated.

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2} + R_{FB3}) \cdot V_{REF}}{R_{FB3}}$$

$$V_{OUT} = \frac{(2000k + 26.1k) \cdot 5.0V}{26.1k} = 388.1V$$

Power dissipation of divider resistors is given by the following.

$$P_{R_{FB1}} = P_{R_{FB2}} = \frac{(V_{out} - V_{REF})^2}{2(R_{FB1} + R_{FB2})}$$

$$P_{R_{FB1}} = P_{R_{FB2}} = \frac{(388.1V - 5V)^2}{4 \times 1000k} = 37mW$$

VFB is a multi-function pin with the following functionalities:

- The VFB pin is an input to the open-loop comparator that references a V_{OLP} threshold of 19% of V_{REF}. The IC is restrained in the Stand-by Mode whenever VFB pin is less than V_{OLP}.
- The VFB pin is also non-inverting input to the overvoltage comparator. This comparator is designated the OVP(VFB) comparator in the IC Block diagram in the datasheet. The typical overvoltage set-point is V_{OVP}=106%V_{REF} and the re-enable set-point is $V_{OVP(RST)}$=103%V_{REF}.

  $$V_{OVP} = 1.06 \cdot V_{REF} = 5.30V$$

  $$V_{OVP(RST)} = 1.03 \cdot V_{REF} = 5.15V$$

  Using the resister divider determined earlier, it is a straightforward calculation to obtain the overvoltage trigger/re-enable set-points.

  $$V_{OVP} = 1.06 \cdot V_{Out}$$

  $$V_{OVP} = 1.06 \times 388.1 = 412V$$

  $$V_{OVP\ (RST)} = 1.03 \cdot V_{Out}$$

  $$V_{OVP\ (RST)} = 1.03 \times 388.1 = 400\,V$$

3.3.3 Dedicated Overvoltage Protection Divider (OVP/EN pin)

In addition to the overvoltage comparator on VFB pin, IR1152 features a 2nd overvoltage comparator (designated the OVP(OVP) in the IC block diagram) which is connected to the OVP/EN pin. The OVP(OVP) comparator is identical in design to the OVP(VFB) comparator and also references the same trigger and re-enable thresholds of 106% and 103% of V_{REF} respectively. The VFB pin resistor divider calculated earlier is applicable for the OVP/EN pin also. Hence, for this converter, 1Mohm, 1% tolerance resistor is selected for R_{OVP1} & R_{OVP2} and 26.1kΩ, 1% tolerance resistor is selected for R_{OVP3}. The trigger and re-enable set-points calculated earlier are likewise applicable here too.

3.3.4 Brown-Out Protection R/C Circuit (BOP pin)

IR1152 provides brown-out protection based on direct sensing of rectified AC input line. Information about the rectified AC input voltage is communicated to the BOP pin after scaling it down using a resistor divider network and filtering using a capacitor on BOP pin as shown below. This R/C network is essentially a voltage-division/averaging network. The sinusoidally varying rectified AC voltage is divided by the resistor divider and averaged by the capacitor and presented at the BOP pin as a DC level, $V_{BOP,\ AVG}$ along with some ripple, ΔV_{BOP}. The BOP pin R/C circuit is illustrated in Fig.5. The BOP pin voltage is illustrated in Fig.6.

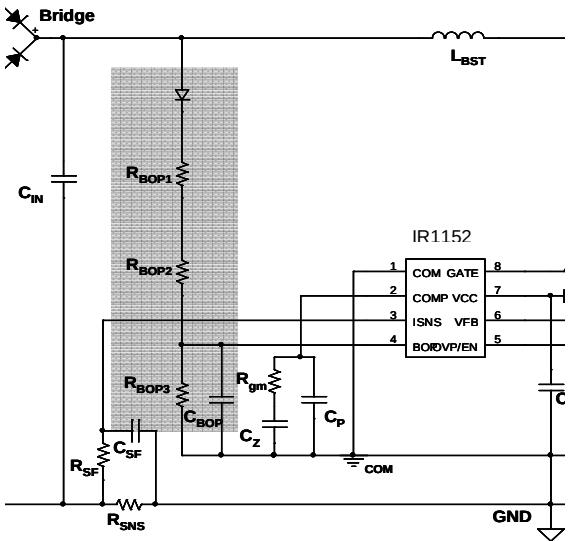

Fig 5: Brown-out protection circuit for IR1152

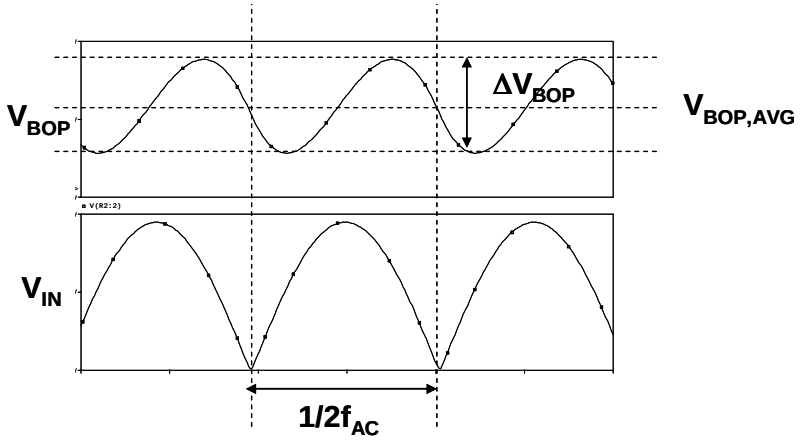

Fig 6: Voltage waveform on the BOP pin is comprises a DC level ($V_{BOP,AVG}$) and a ripple voltage (ΔV_{BOP})

The DC level $V_{BOP,AVG}$ is given by:

$$V_{BOP,AVG} = \frac{R_{BOP3}}{R_{TOT}} \cdot V_{ACAVG}$$

where

$$R_{TOT} = R_{BOP1}+R_{BOP2}+R_{BOP3}$$

$$V_{AC,AVG} = \frac{2}{\pi}\sqrt{2} \cdot V_{IN(RMS)}$$

Hence:

$$V_{BOP,AVG} = \frac{R_{BOP3}}{R_{TOT}} \cdot \frac{2}{\pi}\sqrt{2} \cdot V_{IN(RMS)}$$

Thus $V_{BOP,AVG}$ depends only on the resistor divider and the AC input voltage.

The ripple ΔV_{BOP} is given by the transfer function represented by the resistor divider and the capacitor:

$$T(s) = \frac{\Delta V_{BOP}}{V_{AC,PK}} = \frac{R_{BOP3}}{R_{TOT}} \cdot \frac{1}{1 + sC_{BOP} \cdot \frac{(R_{BOP1} + R_{BOP2})R_{BOP3}}{R_{TOT}}}$$

Thus:

$$|\Delta V_{BOP}| = \sqrt{2} \cdot V_{IN(RMS)} \cdot \frac{R_{BOP3}}{R_{TOT}} \cdot \frac{1}{\sqrt{1 + (\frac{\omega}{\omega_O})^2}}$$

where:

$$\omega = 2\pi \cdot (2 \cdot f_{AC})$$

$$\omega_O = \frac{R_{TOT}}{(R_{BOP1} + R_{BOP2}) \cdot R_{BOP3} \cdot C_{BOP}}$$

ΔV_{BOP} magnitude is related to C_{BOP} – bigger the capacitor, smaller the ripple.

During start-up, the IC is held in Stand-by mode when the BOP pin voltage, V_{BOP} is less than $V_{BOP(EN)}$=1.56V. Next, when the AC voltage is applied and the BOP pin voltage exceeds this threshold, the IC enters normal operation (assuming all other conditions for normal operation are satisfied). If it is assumed that the system is starting under no load, then the rectified AC voltage is essentially a DC voltage and the BOP pin voltage is also DC.

$$V_{BOP} = \frac{R_{BOP3}}{R_{TOT}} \cdot V_{AC,PK} = \frac{R_{BOP3}}{R_{TOT}} \cdot \sqrt{2} \cdot V_{IN(RMS)}$$

Under this condition, the AC voltage at which the IC becomes operational is given by:

$$\frac{R_{BOP3}}{R_{TOT}} \cdot \sqrt{2} \cdot V_{IN,ON(RMS)} > 1.56V$$

However, if the system is starting up under a loaded condition, then the rectified AC voltage is a varying sinusoidal function. In this case, the BOP pin voltage is as described before (DC level + superimposed ripple). In this case, the IC becomes operational when the maxima of V_{BOP} exceeds $V_{BOP(EN)}$=1.56V.

$$V_{BOP,MAX} = V_{BOP,AVG} + \Delta V_{BOP}/2 \ > \ 1.56V$$

Hence the exact AC voltage at which the IC becomes operational depends on the load condition at start-up. C_{BOP} must be big enough to ensure that ΔV_{BOP} is greater than the BOP hysteresis (1.56-0.76=0.8V) at the required minimum AC input voltage, should the system start-up under a loaded condition.

Once the IC becomes operational and starts boosting the DC voltage, then the rectified AC voltage will show sinusoidal variation. Subsequently, if the AC voltage is reduced then $V_{BOP,AVG}$ & ΔV_{BOP} both decrease in magnitude. When the minima of the BOP pin voltage encounters the Brown-out trip threshold V_{BOP}=0.76V then the IC enters brown-out fault mode.

$$V_{BOP,MIN} = V_{BOP,AVG} - \Delta V_{BOP}/2$$

When a Brown-out fault is encountered, the gate pulse is immediately terminated, the COMP pin is actively discharged, ICC current consumption falls to a few milli-amperes and the BOP pin voltage has to exceed $V_{BOP,EN}$ once again for the IC to restart.

The condition at which IC enters Brown-Out fault is then given by:

$$V_{BOP,MIN} \ < \ 0.76V$$

The high input impedance and low bias current (<1uA) of the BOP comparator allows a high impedance to be used for the BOP divider network. 5-10MΩ is an acceptable range. A standard 3MΩ, 1% tolerance resistor is selected for R_{BOP1} & R_{BOP2} for this converter. R_{BOP3} is selected based on $V_{AC,ON}$, the AC input voltage

at which the converter is expected to start-up. Assuming $V_{AC,ON}$=65VAC and no-load condition at start-up,

$$R_{BOP3} = \frac{V_{BOP(HI)}(R_{BOP1} + R_{BOP2})}{(\sqrt{2}.V_{AC,ON} - V_{BOP(HI)} - V_{Bridge})}$$

$$R_{BOP3} = \frac{1.56V(3M\Omega + 3M\Omega)}{(\sqrt{2}.65VAC - 1.56\text{V} - 2\text{V})}$$

$$R_{BOP3} = 105.9k\Omega$$

Next, assuming a target $V_{AC,OFF}$=55VAC, C_{BOP} has to be selected. First $V_{BOP,AVG}$ is calculated at $V_{AC,OFF}$:

$$V_{BOP,AVG} = \frac{\sqrt{2}.V_{AC,OFF}(R_{BOP3})}{(\pi/2).(R_{BOP1} + R_{BOP2} + R_{BOP3})}$$

$$V_{BOP,AVG} = \frac{\sqrt{2}.55V_{AC}.105.9k\Omega}{(\pi/2).(3M\Omega + 3M\Omega + 105.9k\Omega)}$$

$$V_{BOP,AVG} = 0.86V$$

Then, forcing $V_{BOP,MIN}$ (=$V_{BOP,AVG}$ - ΔV_{BOP}/2) = 0.76V, we can calculate the required ΔV_{BOP} at $V_{AC,OFF}$. At $V_{AC,OFF}$=55VAC, this yields

$$\Delta V_{BOP} = 2*(0.86-0.76) = 0.2V$$

In order to calculate C_{BOP}, we just have to force the magnitude of the transfer-function at f=2*f_{AC}=126Hz to be equal to 0.2V calculated above (maximum f_{AC} is the design condition that needs to be considered to ensure that the IC is guaranteed to terminate operation at $V_{AC,OFF}$. At a lower f_{AC}, when there is higher ripple, the IC will cease operation at a higher V_{AC}). Thus:

$$\left|\Delta V_{BOP}\right| = \sqrt{2} \cdot V_{AC,OFF} \cdot \frac{R_{BOP3}}{R_{TOT}} \cdot \frac{1}{\sqrt{1 + (\frac{\omega}{\omega_O})^2}} = 0.2V$$

where:

$$\omega = 2\pi \cdot (2 \cdot f_{AC})$$

$$\omega_O = \frac{R_{TOT}}{(R_{BOP1} + R_{BOP2}) \cdot R_{BOP3} \cdot C_{BOP}}$$

$$\frac{1}{\sqrt{1 + (\frac{\omega}{\omega_O})^2}} = 0.2V \times \frac{R_{TOT}}{R_{BOP3}} \times \frac{1}{\sqrt{2} \cdot V_{AC,OFF}} = 0.2V \times \frac{6.1059M\Omega}{0.1059M\Omega} \times \frac{1}{\sqrt{2} \cdot 55Vac} = 0.148$$

$$\omega = 2\pi \cdot (2 \cdot f_{AC}) = 2\pi \cdot (2 \cdot 63) = 791.68$$

ω_o is then calculated to be:

ω_o = 118

From ω_o, C_{BOP} is calculated:

$$C_{BOP} = \frac{R_{TOT}}{(R_{BOP1} + R_{BOP2}) \cdot R_{BOP3} \cdot \omega_O} = \frac{6.1059M\Omega}{6M\Omega \times 0.1059M\Omega \times 118} = 81nF$$

For the converter, we can choose the following:

R_{BOP1} = R_{BOP2} = 3Mohm

R_{BOP3} = 100kohm

C_{BOP}=100nF

Since selected R_{BOP3} is slightly less than what was calculated, $V_{AC,ON}$ will be slightly higher than 65VAC. Since selected C_{BOP} is slightly higher than what was calculated, $V_{AC,OFF}$ will be slightly lower than 55VAC.

3.3.5 Voltage Loop Compensation (COMP pin)

The voltage feedback loop monitors the DC bus voltage (V_{OUT}) via the V_{FB} resistor divider whose transfer function is $H_1(s)$. Comparison of the V_{FB} pin voltage and internal reference voltage of the IC by voltage error amplifier yields a control signal (V_m = V_{COMP}-$V_{COMP,START}$). The transfer function of the error amplifier and compensation network is $H_2(s)$. The IR1152 output voltage error amplifier is a trans-conductance type amplifier and output of the error amplifier is connected to the COMP pin. The control signal directly controls the magnitude of the boost inductor current (I_L), which is also the input current of the PFC converter. The transfer function between I_L and control signal V_m is given by $H_3(s)$. The power stage of the PFC converter along with DC bus capacitor, maintains a constant voltage (V_{OUT}) at the converter output where the system load draws energy from the converter. The power stage + DC bus capacitor + system load transfer function is given by G(s). The small-signal model of the voltage feedback loop is depicted below in Fig.7. The overall loop gain transfer function *T(s)* is given by:

$$T(s) = H_1(s).H_2(s).H_3(s).G(s)$$

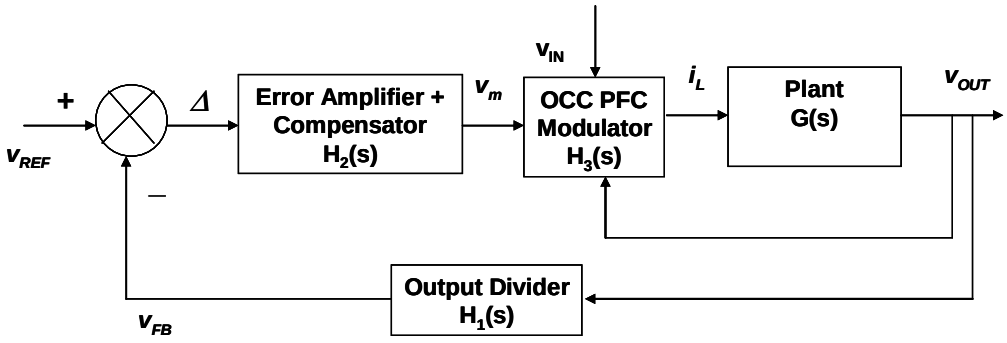

Fig.7: Small-signal modeling of the PFC voltage feedback loop

Voltage loop compensation is performed by adding R/C components between COMP and COM pins in order to:

i. Achieve the appropriate dynamic response characteristics during load/line fluctuations
ii. Ensure that the $2*f_{AC}$ ripple in V_{OUT} at steady state conditions, does not cause too much current distortion

In order to evaluate the overall loop gain transfer function *T(s)*, the small-signal transfer function of each of the blocks has to be evaluated first.

❖ Plant Gain, *G(s)*

The plant gain G(s) models the small signal variation in the DC bus voltage when a small perturbation occurs in the boost inductor current.

$$G(s) = v_{OUT}/i_L = (v_{OUT}/i_{CHG}).(i_{CHG}/i_L)$$

where the small signal parameters are italicized and i_L is the boost inductor current, v_{OUT} is the bus voltage and i_{CHG} is the current sourced at the output of the boost converter power stage (i.e. boost diode current).

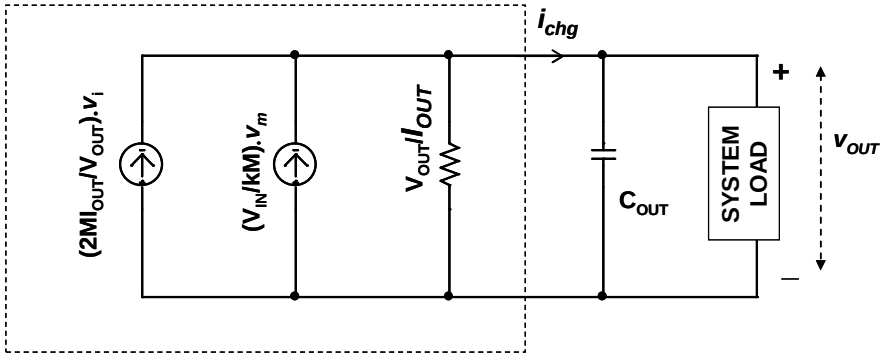

Fig.8: Small-signal model of PFC converter power stage

If the system load is a **Resistive Load**, the transfer function is:

$$\frac{v_{out}}{i_{chg}} = \frac{R_L/2}{1 + sC_{out}\frac{R_L}{2}}$$

In the power stage transfer function, this is represented by a pole:

$$f_{PS} = \frac{1}{2\pi \cdot C_{out}\frac{R_L}{2}}$$

For a **Constant Power Load**, the shunt impedance and the system load cancel each other out and the equivalent impedance is infinite, in which case the transfer function reduces to:

$$\frac{v_{out}}{i_{chg}} = \frac{1}{sC_{out}}$$

In the power stage transfer function, this is represented by a pole at the origin.

Under a **Constant Current Load**, since the impedance of a current source is infinitely high, the equivalent impedance is effectively just the shunt impedance:

$$\frac{v_{out}}{i_{chg}} = \frac{R_L}{1 + sC_{out}R_L}$$

In the power stage transfer function, this is represented by a pole:

$$f_{PS} = \frac{1}{2\pi \cdot C_{out}R_L}$$

Next *(i_{CHG}/i_L)* transfer function has to be evaluated. Assuming 100% efficiency, recognize that:

$$V_{IN}.I_L = V_{OUT}I_{OUT}$$

I_{OUT} is same as the DC component of the boost diode current (I_{CHG}). Hence

$$V_{IN}.I_L = V_{OUT}I_{CHG}$$

Applying linearization and small-signal analysis, for a given DC operating point defined by V_{IN} & V_{OUT} yields the relationship between i_{CHG} & i_L:

$$i_{CHG}/i_L = V_{IN}/V_{OUT}$$

Assuming a resistive load, the overall power stage transfer function can now be written as:

$$G(s) = \frac{V_{IN}}{V_{OUT}} \times \frac{R_L/2}{1 + sC_{out}\frac{R_L}{2}}$$

❖ OCC PFC Modulator, $H_3(s)$

In order to derive i_L/v_m, the One Cycle Control PWM modulator control law is employed:

$$G_{DC} \cdot R_S \cdot i_L = \frac{v_m}{M(d)}$$

where M(d) = V_{OUT}/V_{IN} for a given DC operating point defined by the DC bus voltage V_{OUT} and RMS input voltage V_{IN}. This ultimately yields

$$H_3(s) = \frac{i_L}{v_m} = \frac{V_{in}}{V_{OUT}R_S G_{DC}}$$

❖ Output voltage sensor Resistor-Divider, *$H_1(s)$*

The output divider scales the output voltage to be compared with the reference voltage in the error amplifier.

Therefore:

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2} + R_{FB3})V_{REF}}{R_{FB3}}$$

$$H_1(s) = \frac{V_{REF}}{V_{OUT}}$$

The uncompensated loop gain and phase is shown in Fig.9 for 85-264VAC at 350W load condition (assuming resistive load). This is simply the $H_1(s).H_3(s).G(s)$ transfer function product illustrating the pole due to the plant gain.

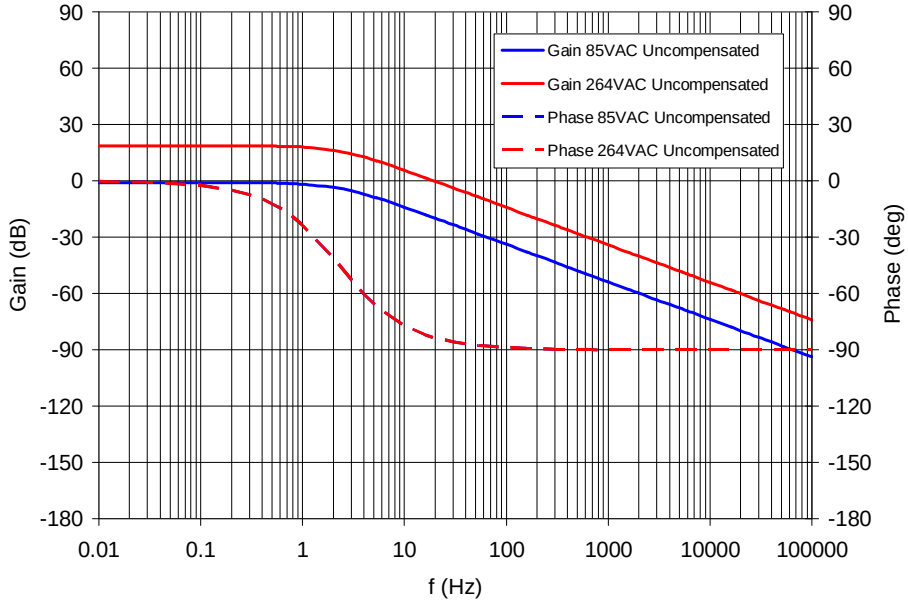

Fig.9 The uncompensated transfer function [=$H_1(s).H_3(s).G(s)$]

❖ Error Amplifier & Compensation, *$H_2(S)$*

The compensation scheme typically employed for a first-order, single-pole system aims to:

- add a pole at the origin in order to increase the low frequency gain and improve DC regulation
- add a low-frequency zero to boost phase margin near cross-over frequency and partially compensate the pole
- add a high-frequency pole to attenuate switching frequency noise and ripple effects

The above 3 requirements can be achieved in case of the transconductance type voltage error amplifier with the compensation scheme shown in Fig.10. However,

as mentioned earlier, for the PFC converter, the most important criterion for basing the selection of the compensation component values is the voltage loop bandwidth.

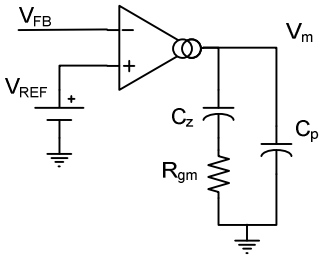

Fig10: Voltage Loop error amplifier compensation network

The error amplifier transfer function is given by:

$$H_2(s) = \frac{g_m \cdot (1 + sR_{gm}C_Z)}{s(C_Z + C_P + sR_{gm}C_ZC_P)}$$

where g_m is the transconductance of the voltage error amplifier. The compensation network adds a zero and a pole in the transfer function at:

$$f_{Z0} = \frac{1}{2\pi \cdot R_{gm} \cdot C_Z}$$

$$f_{P0} = \frac{1}{2\pi \cdot R_{gm} \frac{Cz \cdot Cp}{Cz + Cp}}$$

The gain and phase of the error amplifier + compensation transfer function is illustrated in Fig.11.

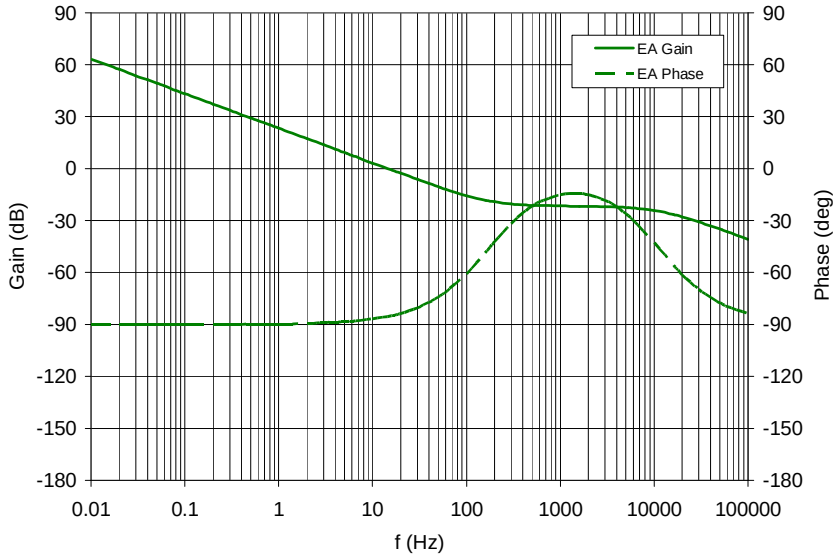

Fig.11: Error Amplifier + compensation transfer function characteristics

❖ Voltage Loop Compensation procedure

Step 1: Choose C_z based on soft-start time:

A soft-start time of 60ms is selected. Typical values range from 50ms to a few hundred ms, depending upon the application. The soft-start time represents the time needed by the controller to ramp V_{COMP} from zero to the maximum value. The system will take no more than 60ms to achieve near-regulation.

$$C_Z = \frac{t_{SS} \cdot i_{OVEA}}{V_{COMP(EFF)}(MIN)}$$

i_{OVEA} and $V_{COMP(EFF)}$(MIN) are taken from the datasheet.

$$C_Z = \frac{60ms \times 44\mu A}{4.7V} = 0.56\mu F$$

A standard value of 0.56uF can be selected for the converter for C_Z.

Step 2: Choose R_{gm} to ensure that $H_1(s).H_2(s)$ attenuation at $2xf_{AC}$ frequency is small enough to avoid current distortion:

The amount of $2xf_{AC}$ ripple on the output capacitor is calculated first. The minimum f_{AC} of 47Hz is considered here, since the ripple is the maximum at the lowest AC frequency. The peak-to-zero ripple V_{OPK} is given by:

$$V_{OPK} = \frac{P_{in,MAX}}{2\pi \cdot 2 \cdot f_{AC} \cdot C_O \cdot V_{out}}$$

$$V_{OPK} = \frac{380W}{2\pi \cdot 2 \cdot 47 \cdot 330\mu F \cdot 385V}$$

$$V_{OPK} = 5.1V$$

The peak-to-peak ripple in V_{OUT} is $2xV_{OPK}$. This ripple in V_{OUT} is reflected in the V_{COMP} voltage based on the attenuation provided by the resistor divider and error amplifier compensation network combined i.e. $H_1(s).H_2(s)$ at $2xf_{AC}$. The ripple in V_{COMP} i.e. ΔV_{COMP} has to be small compared with the value of the error amplifier output voltage swing ($V_{COMP,EFF}$). Typical values for $\Delta V_{COMP}/V_{COMP}$ range from 0.5% to 1%. 0.5% is recommended if current shaping has to be excellent while 1% is recommended for higher phase margin and low-oscillation response to load steps. 0.5% attenuation demands a (G_{VA}) of:

$$G_{VA} = \frac{V_{COMP(EFF)} \cdot 0.005}{2 \cdot V_{OPK}}$$

$$G_{VA} = \frac{4.7V \cdot 0.005}{2 \cdot 5.1V} = 0.0023$$
$$G_{VA} = -52.7dB$$

This is the required attenuation in $H_1(s).H_2(s)$ at $2xf_{AC}$ frequency.

$H_1(s)$, given by $V_{REF}/V_{OUT,}$ is next calculated:

$$H_1 = \frac{5V}{385V} = 0.013 = -37.7dB$$

The required attenuation from $H_2(s)$ alone at 2x47Hz is then given by:

$$G_{VA} - H_1 = -15dB$$

Since the error amplifier pole will be set at a much higher frequency than $2xf_{AC}$ (and consequently $C_z >> C_p$), the error amplifier transfer function at $2xf_{AC}$ can be approximated to:

$$H_2(s) \cong \frac{g_m \cdot (1 + sR_{gm}C_Z)}{sC_Z}$$

Since C_Z has already been determined, only R_{gm} needs to be calculated:

$$\left|H_2(j2\pi \cdot f_{AC})\right| = G_{VA} - H_1 = -15dB = 0.177$$

$$R_{gm} = \sqrt{\left(\frac{G_{VA} - H_1}{g_m}\right)^2 - \left(\frac{1}{2\pi \cdot 2 \cdot f_{AC} \cdot C_Z}\right)^2}$$

Substituting f_{AC}=47Hz, g_m=49µS, C_Z=0.56µF yields

$$R_{gm} = 2k\Omega$$

The location of the zero in the compensation scheme can now be estimated:

$f_z = 1/(2*\pi*R_{gm}.C_z) = 1/(2*\pi*2kohm*0.56\mu F) = 142Hz$

The location of the pole in the power stage transfer function (assuming a resistive load) is:

$f_{PS} = 1/(2*\pi*C_{OUT}*R_L/2) = 1/[2*\pi*330uF*(385V*385V/350W)/2] = 2.3Hz$

Since the location of zero is more than a decade away from that of the pole, it is likely that this compensation scheme may result in low phase margin. This is discussed more in “Phase Margin Discussion” in step 4.

Step 3: Choose Cp based on high-frequency pole location

The pole frequency should be chosen higher than the cross over frequency and significantly lower than the switching frequency in order to attenuate switching noise and switching frequency ripple in the output capacitor: typical value is 1/6 to 1/10 of the switching frequency. Choosing $1/6xf_{SW}$ (=0.166*66kHz=11kHz) for this converter:

$$f_{P0} = \frac{1}{2\pi \cdot R_{gm} \frac{Cz \cdot Cp}{Cz + Cp}} \cong \frac{1}{2\pi \cdot R_{gm} \cdot Cp}$$

$$C_p = \frac{1}{2\pi \cdot 2k\Omega \cdot 66kHz \cdot 0.166} = 7.32nF$$

Step 4: Estimate bandwidth & phase margin

The voltage loop response for 85VAC and 264VAC is plotted at full output power condition of 350W in Fig.12. At 85VAC/350W the cross-over frequency is 5Hz and phase margin is about 27°. At 264VAC/350W the cross-over frequency is 16Hz and phase margin is about 15°. This was anticipated considering the wide separation between the zero and the pole locations. In this converter, due to the low phase margin, the response to a load step can be oscillatory and may not be acceptable in some applications. At lighter load conditions, the phase margin will drop even further. However, there will be fast transient response. In the end the trade-off between transient response and phase margin should be considered.

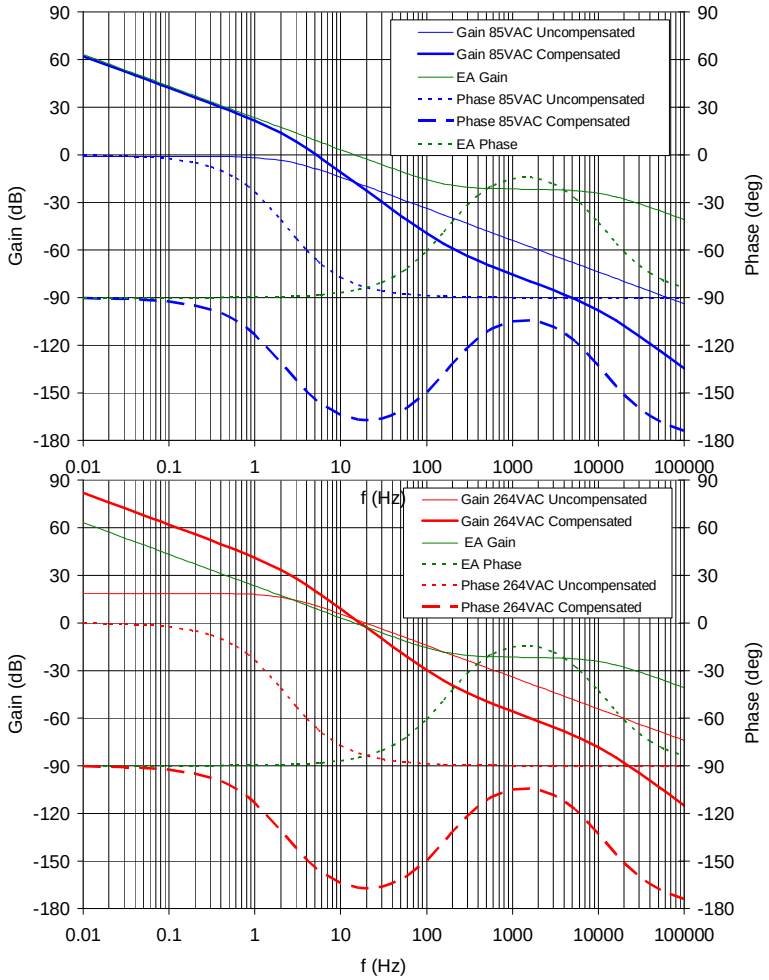

Fig.12: Overall Loop Gain at 85/264VAC & 350W (fast loop + low phase margin)

❖ Phase Margin Discussion:

The zero in the error amplifier compensation can provide phase boost to compensate the phase lag due to the power stage pole. If the zero is more than a decade away from the power stage pole there is minimal phase boost. The location of the zero can be brought closer to the power stage pole by increasing the value of C_z or R_{gm} or both. However, the trade-offs are as follows:

- Increasing C_z reduces the DC gain of the transfer function and slows down the loop response (more sluggish response to a load step)
- Increasing R_{gm} increases the low frequency gain of the error amplifier transfer function and hence the attenuation at $2xf_{AC}$ may be insufficient to meet the 0.5% requirement described earlier.

To illustrate the trade-offs, the following examples are presented with the goal of improving the phase margin:

- Option 1: Increase the soft-start time. For example, if the soft-start time is increased to 180ms (3x), then Cz=1.69uF, Rgm=3.49kohm, Cp=4.2nF. The cross-over frequency and phase margin are 2.6Hz & 47° at 85VAC and 9.5Hz and 33° at 264VAC as seen in Fig.13. Due to the higher C_z capacitor, the transient response behavior is likely to be more sluggish for this compensation arrangement.

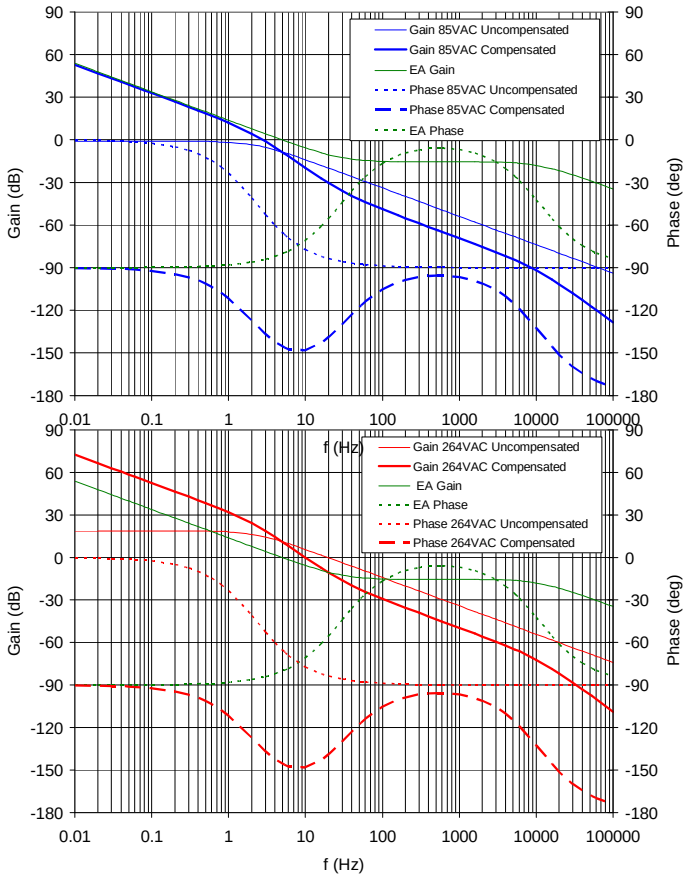

Fig.13: Overall Loop Gain at 85/264VAC, 350W (slow loop + high phase margin)

- Option 2: At the expense of current distortion due to increased $2*f_{AC}$ ripple in V_{OUT}, increase only the R_{gm} resistor while retaining the same soft-start time. This has the effect of placing the zero closer to the pole in the power stage. For example if H1(s).H2(s) attenuation at 2xfAC can be set at 1.5% instead of 0.5%. Then retaining C_z=0.56uF, we can recalculate R_{gm}=10kohm and recalculate Cp=1.4nF. The cross-over frequency and phase margin are 5Hz & 35° at 85VAC and 20Hz and 42° at 264VAC as seen in Fig.14. While this may cause some distortion (increased 3rd harmonic current), the EN61000-3-2 harmonic standards will still easily be met.

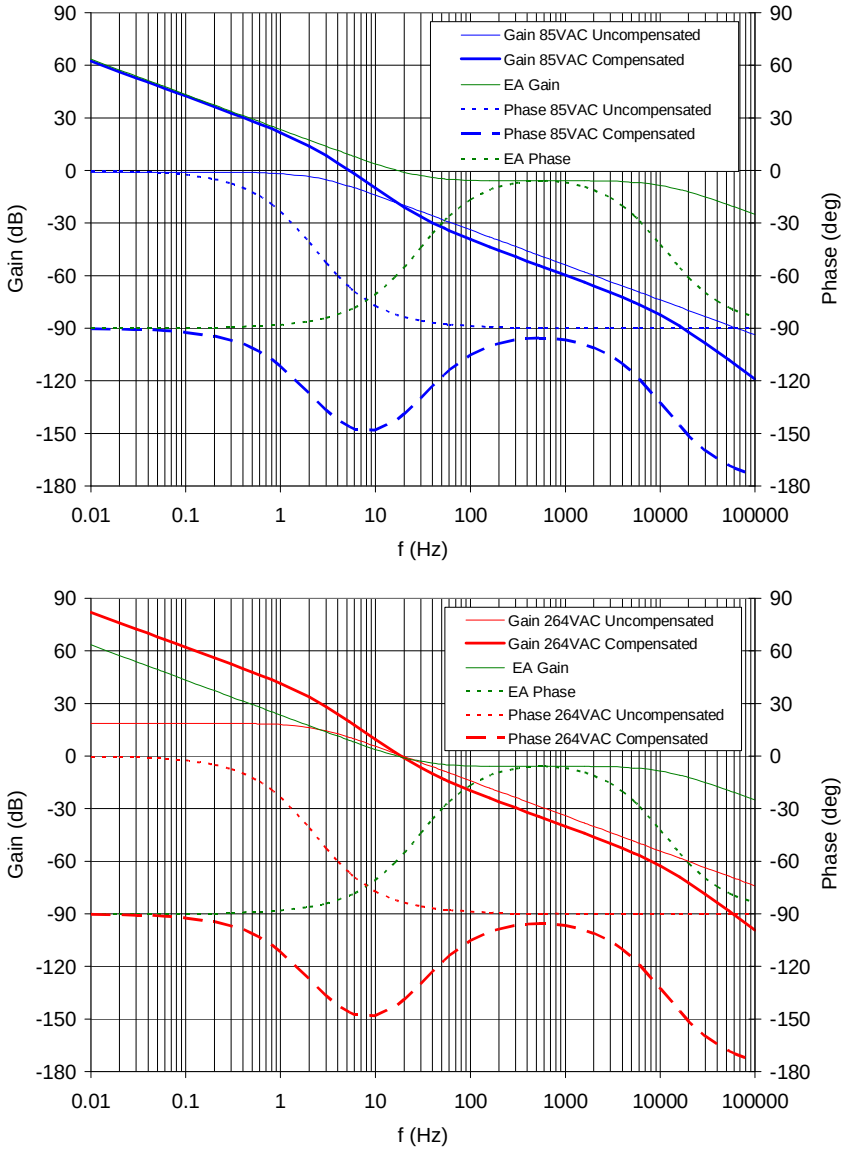

Fig.14: Overall Loop Gain at 85/264VAC, 350W (fast loop + high phase margin, but possibly increased current distortion)

- Option 3: This is the compromise approach between option 1 & 2 and is left to the user to pursue (for example using soft-start time=100ms & H1(s).H2(s) attenuation at $2xf_{AC}$ = 1%).

4. PFC Converter Physical Design & Layout Tips

4.1 Pin COM

Grounding is the most important layout consideration for PFC ICs. Some ICs even have separate power ground and signal ground pins for better noise immunity. Since IR1152 has only one ground pin, additional care is required during board layout. The parasitic inductance and capacitance in the power ground trace usually generates a lot of noise because of high RMS currents and 'dV/dt's & 'dI/dt's from switching loops. There is also the possibility of high common-mode currents that is to be considered for certain types of loads (such as motor drive inverters). This is illustrated in Fig.15. The control circuitry of the IC has to be shielded from this noise as much as possible.

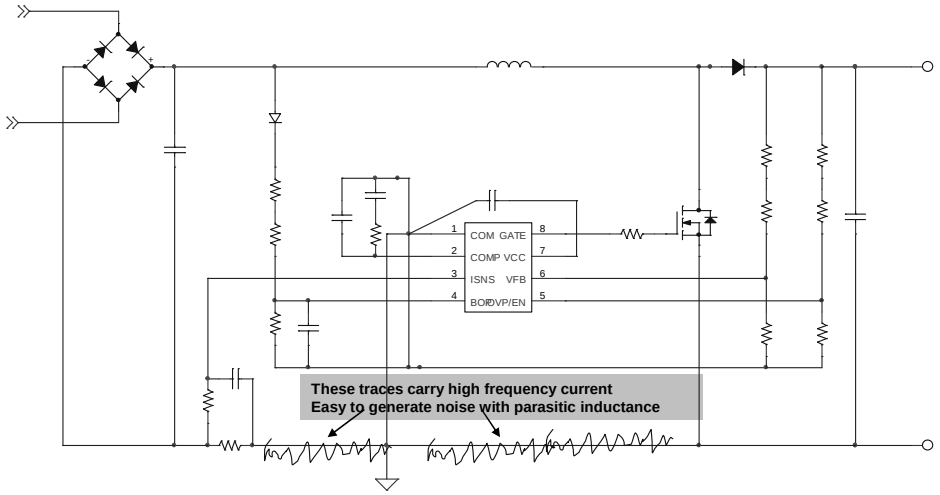

Fig.15: – Noise in power ground (BAD connection practice)

A few rules are listed below which can improve the system noise immunity.

- COM Rule 1: A STAR-connection is highly recommended in PFC converter layout for the power GND, IC COM & MOSFET source nodes. In the star-connection, the IC COM pin, the current sense resistor and source of PFC switch are connected at one single point as illustrated in Fig.16. If a ground plane is used, it is important to ensure that the ground plane does not conduct currents. So the ground plane is also connected to the STAR-connection point only.

In terms of the control circuitry, the best approach is to provide each control loop of the IC with a dedicated return path and have an independent star-connection

to IC COM pin. However, in reality, sometimes it is difficult to do so due to the limitation of PCB space and hence it is useful to apply some rules:

- COM Rule 2: Separate the VCC and Gate-drive loop return paths to COM from all other control circuit loops (The gate drive loop and VCC loop are the noisiest of all control circuit loops. Both carry high-frequency switching currents for turning the PFC switch on/off).
- COM Rule 3: V_{COMP} voltage is the control voltage for the feedback loop from which the oscillator of the IC is also derived. Hence the return path of the COMP loop is very important in IR1152. It is recommended to provide the COMP control loop with a dedicated return path to COM pin (as shown in Fig.18 in "Pin COMP" rules section next).
- COM Rule 4: VFB, OVP & BOP control loops can share the same return path to COM.
- COM Rule 5: The star connection point must be as close to the IC as physically possible.

These rules are illustrated in Fig.17.

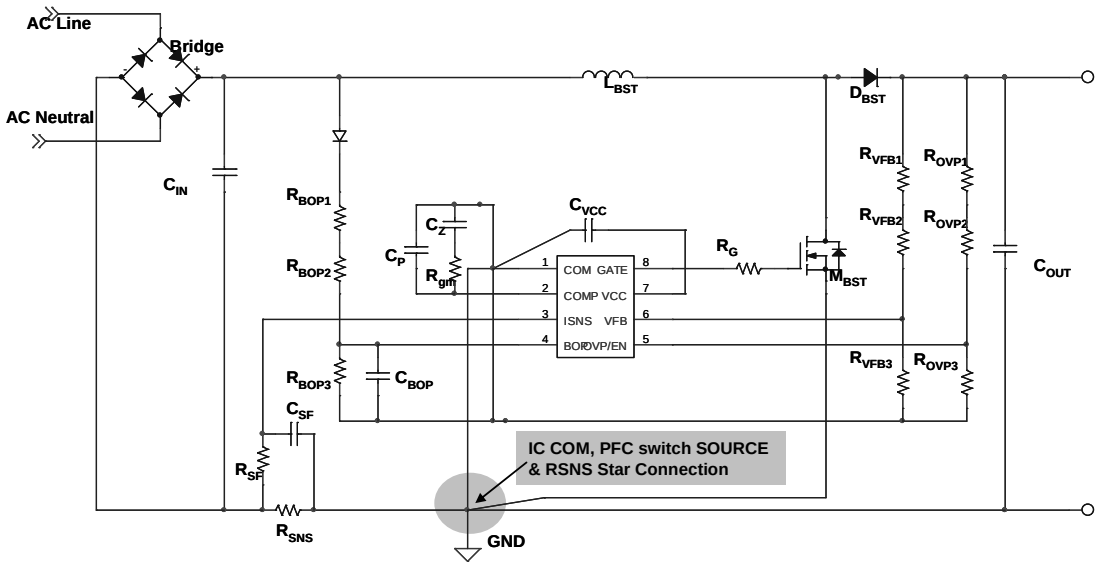

Fig.16: STAR-Connection for system ground, GND

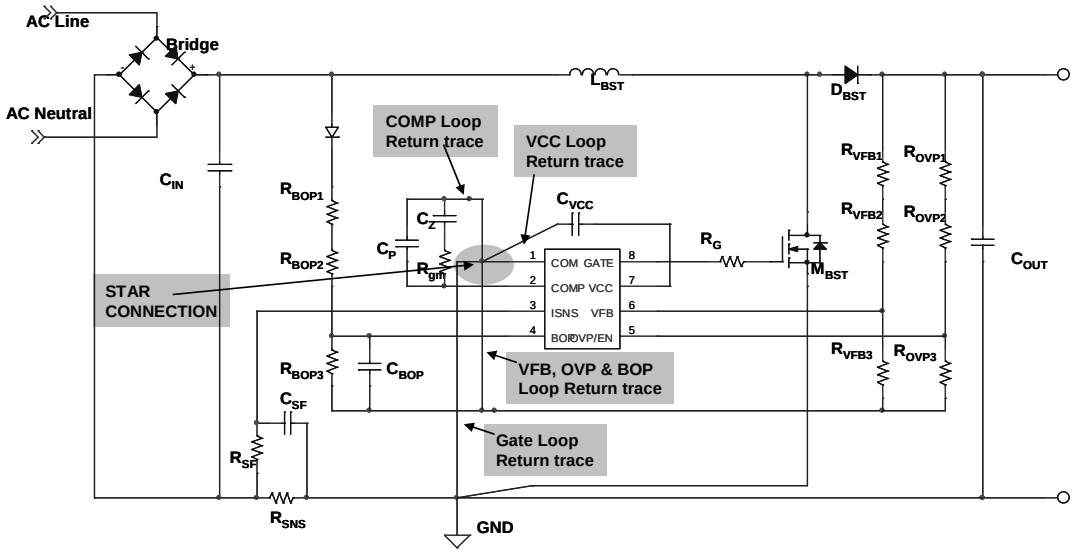

Fig.17: 3 IC control loops with STAR connection to COM

4.2 Pin COMP

The COMP pin is the most important control pin in IR1152. V_{COMP} voltage is the control voltage for the feedback loop from which the oscillator of the IC is also derived. It is very important to follow the 2 rules below to maintain a stable feedback loop and stable oscillator.

COMP RULE 1: Place the C_Z, C_P & R_{gm} components close to COMP pin.

COMP RULE 2: Keep the compensation loop of IR1152 fully independent from all other control circuit loops (don't share ground return race of COMP loop with other control loops)

It is for these reasons that the COMP is located right next to the COM pin to facilitate easy, isolated routing of the COMP control loop. These rules are illustrated in Fig.18 below.

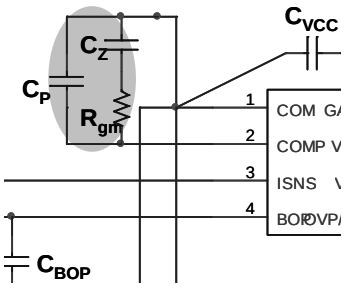

Fig. 18: Fully isolated COMP control loop

4.3 Pin ISNS

Current sensing is always tough in PFC converters, because the signal level is low while environment is noisy. Further, common mode currents tend to preferentially flow through the current sense line rather than the boost inductor line, because of the high-frequency impedance offered by the boost inductor. The ISNS pin also needs one-point connection to the negative side of current sense resistor through a current-limiting series resistor. If RC filtering is to be performed for VISNS, place the filter capacitor C_{SF} close to the current sense resistor (rather than close to the IC) as shown Fig.19 in order to filter the noise at the source.

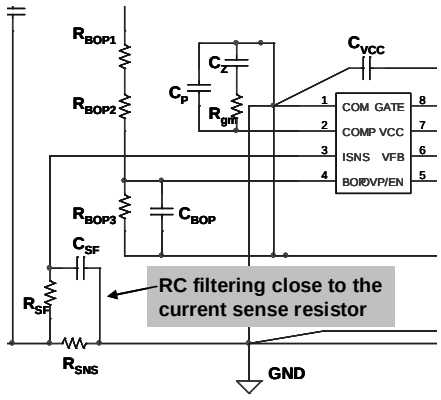

Fig.19: ISNS connection with RC filter close to the RSNS resistor

Use non-inductive resistor (metal strip or film type) for current sensing to avoid high di/dt transient noise. Do not use wirewound type resistor.

4.4 Pins BOP, OVP/EN & VFB

BOP pin will have a capacitor (100nF or so) tied between the pin & COM. So this pin is relatively noise immune. The OVP and VFB loops are very similar with option of using a stabilization capacitor of few hundred pF, if needed. These two pins will sense output voltage through resistor divider whose high side resistance is about 1-2Mohm & low side resistance is around few tens of kohm. This high impedance between these pins and COM makes them less immune to noise. So it is very important to route the VFB & OVP/EN traces & place the resistor divider components away from high dV/dt or high dI/dt power traces like Drain of MOSFET, Gate driver loop, current sense trace & boost inductor. As mentioned earlier, it is ok for VFB, OVP & BOP control loop return paths (to COM) to share the same trace, since the signals are near-DC on all these pins.

Recall that OVP pin also performs enable function which must be protected from spurious trigger. Adding a small capacitor to OVP pin is recommended. The capacitance cannot be too high since it will affect OVP response time. Normally a 50-100pF cap is good enough to reduce noise while not affecting OVP transient response.

4.5 Pin VCC

A 1uF V_{CC} decoupling capacitor (ceramic SMT capacitor with low ESR) should be placed between VCC & COM pins as close as possible to the IC to minimize the

loop inductance. The ideal location is right on top of the IC as shown in Fig.20. As long as this decoupling capacitor is placed close to the IC, the other bulk VCC capacitor (tens of uF, not shown in Fig.20) which is usually provided can be connected anywhere near the IC. Remember to separate the VCC loop return path (to COM) from the other control loops as it carries the high-frequency current supplying gate charge to drive the PFC switch.

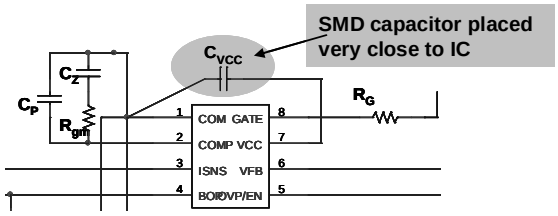

Fig. 20: Vcc decoupling capacitor placed right on top of the IC with tight routing

4.6 Pin Gate

IR1152 GATE output can drive the PFC switch directly or be used with a gate drive buffer. Minimize the length of gate drive loop to reduce the parasitic inductance, that can limit the peak current otherwise place the gate drive buffer close to the switching MOSFETs to achieve fast switching. Also, it's a good practice to choose a bigger gate turn-on resistor and slow down the turning-on speed of MOSFET in order to limit dI/dt & reverse recovery current peaks. Of course, the trade-off with turn-on switching losses must be considered.