Application Note AN-1139

Design of Secondary-Side Rectification using IR1168 Dual SmartRectifier™ Control IC

By Adnaan Lokhandwala

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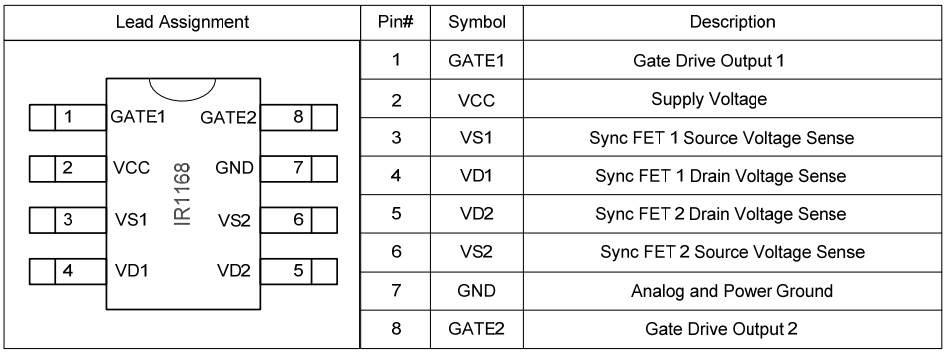
Introduction and Device Overview

IR1168 is a smart secondary-side driver IC designed to drive the two N-Channel power MOSFETs used as synchronous rectifiers in isolated DC-DC resonant converters. The IC can control one or more paralleled MOSFETs to emulate the behavior of Schottky diode rectifiers. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression which allow reliable operation in both fixed and variable frequency modes. The drain to source voltage of the MOSFET is sensed differentially to determine the level of the current and the device is turned on and off in close proximity of the zero current transition. The pinout for this 8 pin device is shown below.



Pin#	Symbol	Description
1	GATE1	Gate Drive Output 1
2	VCC	Supply Voltage
3	VS1	Sync FET 1 Source Voltage Sense
4	VD1	Sync FET 1 Drain Voltage Sense
5	VD2	Sync FET 2 Drain Voltage Sense
6	VS2	Sync FET 2 Source Voltage Sense
7	GND	Analog and Power Ground
8	GATE2	Gate Drive Output 2

Figure 1: IR1168 Dual SmartRectifier™ control IC pin assignment

The SmartRectifier™ Control Technique is based on sensing the voltage across the MOSFET and comparing it with two negative thresholds to determine the turn on and off transition for the device. A higher negative threshold, V_{TH2}, detects current through the body diode and hence, controls the turn on transition for the power device. Similarly, a second negative threshold, V_{TH1}, determines the level of the current at which the device turns off as shown below.

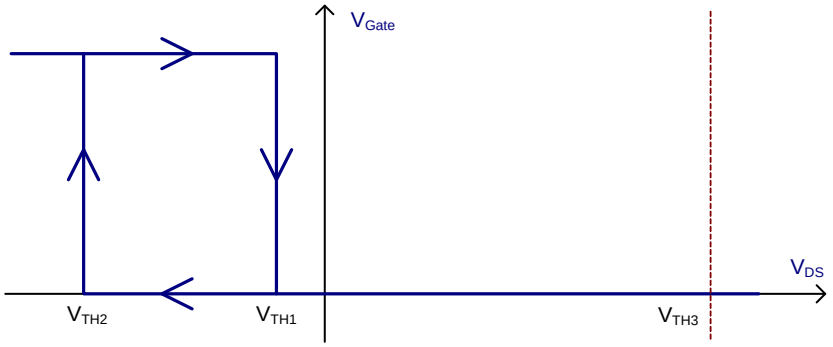


Figure 2: IR1168 Dual SmartRectifier™ control IC differential voltage sensing thresholds

When the power device is turned on, the instantaneous sensed voltage reduces to $R_{DSon} \cdot I_D$ and depending on the level of the device current, could fall below the turn off threshold and cause false device turn off. Additionally, the device turn on is also associated with some parasitic ringing between the transformer leakage inductance and device output capacitance. Hence, additional control logic has been incorporated to prevent false turn off and gate chattering when the device current transitions between its body diode and channel.

LLC Half-Bridge Converter Operation

The increasing popularity of the LLC resonant converter in its half-bridge implementation is due to its high efficiency, low EMI emissions and its ability to achieve high power density. This topology is also the most attractive topology for front-end DC bus conversion. It utilizes the magnetizing inductance of the transformer to construct a complex resonant tank with buck boost transfer characteristics in the soft-switching region. The typical power stage schematic for this topology with synchronous output rectification (low-side configuration) is shown below.

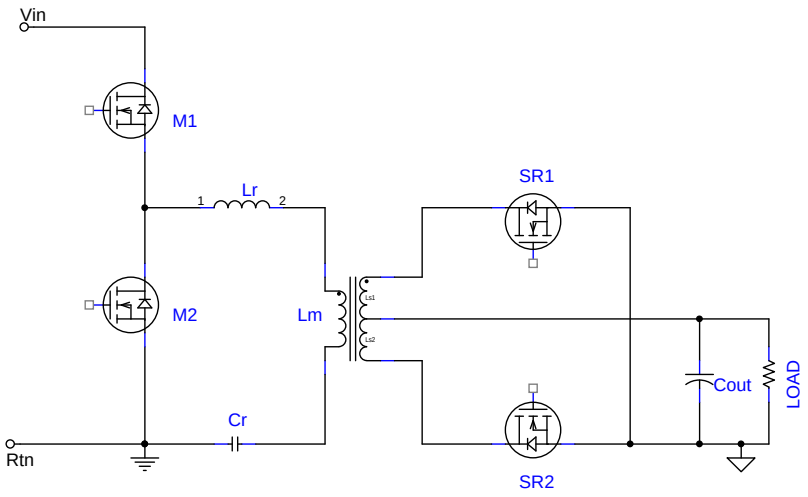


Figure 3: Typical schematic of a DC-DC half-bridge resonant converter with synchronous output rectification

Devices M1 and M2 operate at 50% duty cycle and the output voltage is regulated by varying the switching frequency of the converter. The converter has two resonant frequencies – a lower resonant frequency (given by L_m, L_r, C_r and the load) and a fixed higher series resonant frequency f_{r1} (given by L_R and C_R only). The two bridge devices can be soft-switched for the entire load range by operating the converter either above or below f_{r1}. This topology behaves very

similarly to a series resonant converter when it operates in the region above f_{r1}. The typical AC transfer characteristics[1] for a LLC tank resonant converter are shown in Figure 4.

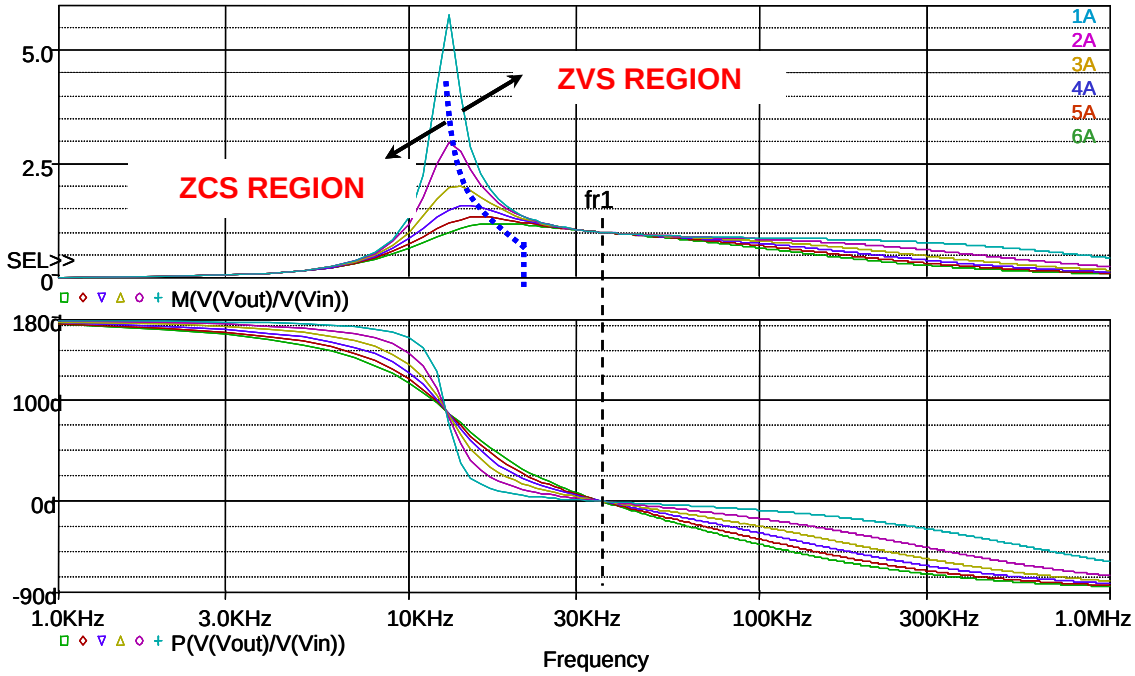


Figure 4: Typical frequency response of a LLC resonant converter

The characteristics of a LLC resonant converter can be divided into three regions according to 3 different modes of operation. The converter should be prevented from entering the ZCS region of operation. In the region above fr1, the converter operates very similar to a series resonant converter. In this operating region, Lm never resonates with resonant capacitor Cr; it is clamped by output voltage and acts as the load of the series resonant tank.

In the ZVS range below f_{r1}, the LLC resonant converter operation is more complex and can be divided into two time intervals. In the first time interval, Lr resonates with Cr and Lm is clamped by output voltage. When the current in the resonant inductor Lr resonates back to same level as the magnetizing current, Lr and Cr stop resonating. Lm now participates in the resonant operation and the second time interval begins. During this time interval, the resonant components change to Cr and Lm in series with Lr.

[1] For this AC analysis, only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to output. The transformer, rectifier and filter are replaced by an equivalent AC resistance, *Rac*.

Dual SmartRectifier™ Operation in Resonant Converters

The IR1168 Dual SmartRectifier™ IC can emulate the operation of the two secondary rectifiers by properly driving the Synchronous Rectifier (SR) MOSFETs. The rectifier currents in the two secondary legs are sensed using the power MOSFET R_{DSon} as a shunt resistance and the GATE pins of the MOSFET are driven depending on the level of the sensed voltage with respect to the 3 thresholds shown earlier in Figure 2.

The core of this device are the two high-voltage (200V), high speed comparators which differentially sense the drain to source voltage of the MOSFET, in order to determine the polarity and level of the device currents. Dedicated internal logic then manages to turn the power device on and off in close proximity of the zero current transition. This ensures accurate performance without the need of PLL or external timing sources. Additionally, internal blanking logic is used to prevent spurious gate transitions and guarantee operation in fixed and variable frequency operation modes. Typical waveforms are shown in Figure 5 below.

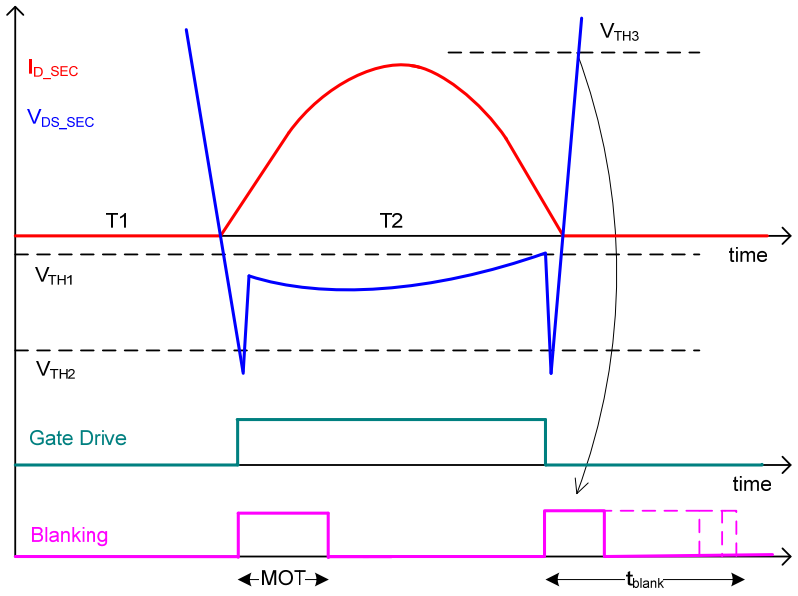


Figure 5: Typical operating waveforms showing MOT and t_{BLANK} functions

➢ *Turn On Phase*

When the conduction phase of the SR FET is initiated, current will start flowing through its body diode, generating a negative V_{DS} voltage across it. The body diode has generally a much higher voltage drop than the one caused by the MOSFET on resistance and therefore will trigger the turn-on threshold V_{TH2}. At that point, the IR1168 will drive the gate of MOSFET ON which will in turn cause the conduction voltage V_{DS} to drop down. This drop is usually accompanied by some amount of ringing, that can trigger the input comparator to turn off; hence, a fixed Minimum On Time (MOT) blanking period is used that will maintain the power MOSFET on for a minimum amount of time. The MOT also limits the minimum conduction time of the SR MOSFET and hence in this case, the maximum switching frequency of the converter.

➢ *Turn Off Phase*

Once the SR MOSFET has been turned on, it will remain on until the rectifier current will decay to the level where V_{DS} will cross the turn-off threshold V_{TH1}. Once the threshold is crossed and the GATE is turned off, the current will once again flow through the body diode causing the V_{DS} voltage to jump negative. Depending on the amount of residual current, V_{DS} may again trigger the turn on threshold; hence, to prevent false turn-on, V_{TH2} is blanked for an internally set blank time after V_{TH1} has triggered as shown in *Figure 5*. As soon as V_{DS} crosses the positive threshold V_{TH3}, this blanking time is terminated and the IC is ready for next conduction cycle. The turn off speed is more critical in this transition to avoid cross conduction on the primary side and reduce switching losses.

Please note that both MOT and the Blanking time logic are allowed only once per switching cycle; it is necessary that V_{DS} reaches V_{TH3} for them to be enabled again (therefore ready for the next switching cycle).

Typical System Schematics and Passive Components Nomenclature

The passive components needed for IR1168 operations are:

- C_{dc}: supply decoupling capacitor

Components not necessary but recommended are:

- R_{CC}: series resistor on supply capacitor
- $R_{g1,\ 2}$: synchronous MOSFET gate resistors

The supply voltage for the IC can be drawn directly from the converter's output when it falls within the recommended range for the IC. In all other cases, it is recommended to provide a dedicated supply through either:

- Auxiliary transformer winding
- Transformer main winding tap

Typical system implementations for IR1168 are shown below –

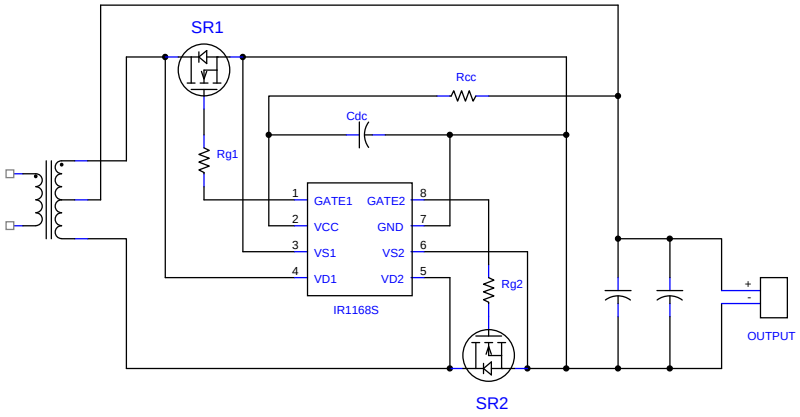


Figure 6: IC Supply derived directly from the converter output voltage

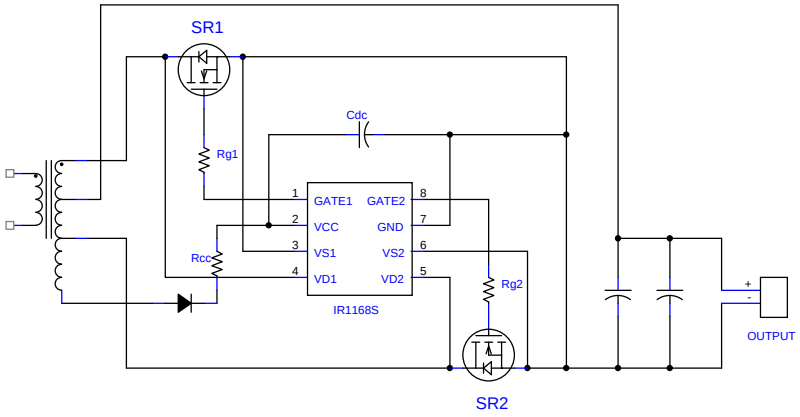


Figure 7: IC supply derived from an auxiliary winding on the power transformer

Detailed Design Procedure

Fundamental values to be captured on the system if not known by design are

1. Minimum ($f_{SW_{min}}$) and maximum ($f_{SW_{max}}$) switching frequency
2. Secondary minimum conduction time, also called Minimum On Time (MOT) in SmartRectifier™ terminology.
3. The maximum temperature of the environment in which the IR1168 IC will operate, $T_{IC_{amb}}$ (this is normally the maximum PCB temperature)
4. The available supply voltage V_{supply} . It can be the converter output voltage or a dedicated supply (auxiliary winding).

The following design procedure assumes that the synchronous MOSFET has been already identified as well as the above mentioned systems parameters. The basic idea behind this is the need to ideally approximate a rectifier behavior, having the voltage sense as a sole input to the controller.

a. IC current consumption calculation

First, from the selected synchronous MOSFET, the total gate charge Q_g and gate to drain charge Q_{gd} data have to be identified, together with the corresponding gate voltage V_{gs}. Because of the IR1168 mode of operations, the secondary device current initially flows through the SR body diode; therefore, the turn on gate characteristic doesn't include the Miller charge of the MOSFET. Figure 8 below shows how the regular gate characteristics (black) change when the switch is turned on at zero or slightly negative drain to source voltage (red).

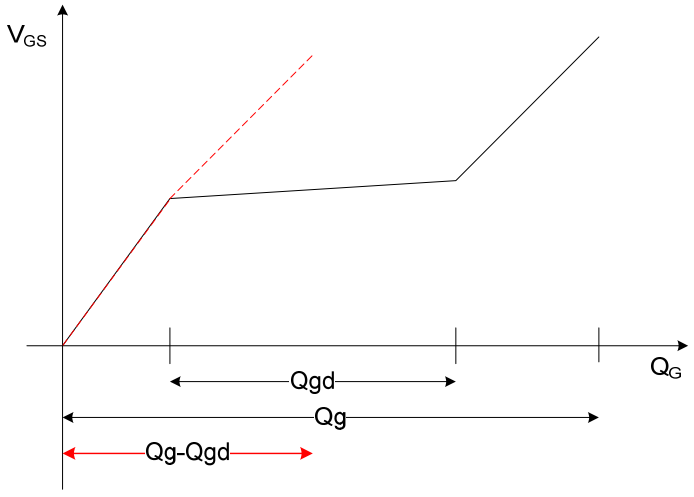


Figure 8: MOSFET gate characteristic when driven by SmartRectifier™ control

It is evident much less charge is required and the behavior can satisfactorily be modeled as a capacitor:

$$C_{sync} = \frac{Q_g - Q_{gd}}{V_{gs}}$$

If more parts are paralleled, the above capacitance must be multiplied with the number of devices. The maximum IC required current can then be calculated using the following equation:

$$I_{CC} = I_{QCC} + 2 \times f_{SW_{\max}} C_{sync} V_{g_{high}} + 1.18 \cdot 10^{-8} f_{SW_{\max}}$$

where $V_{g_{high}}$ is the IR1168 gate driver output voltage and f_{SWmax} is the converter maximum switching frequency as previously identified. The second term is entirely due to the two synchronous MOSFET gate drive while the third term accounts for the IC internal logic consumption in regular operations (the factor $1.18 \cdot 10^{-8}$ accounts for the frequency dependent current requirements for the internal logic). Notice this term is independent of the supply voltage of the IC.

b. Supply series resistor and gate resistor design, and thermal verification

IR1168 based synchronous rectification has the prerogative to turn the switch on and off at V_{DS} levels close to zero. Hence, the gate resistor does not have an impact on the transitions and can be designed on a different basis.

In order for the gate loop to be optimized, oscillations have to be avoided in regular operations. Assuming the total gate trace loop inductance (L_g) is known, (a first order estimation can be 1nH/mm of physical trace length), the minimum recommended gate resistor will be

$$R_{g_{loop}} > 2\sqrt{\frac{L_g}{C_{iss}}}$$

Where C_{iss} is the switch input capacitance (from MOSFET datasheet). It is evident how a good layout practice can dramatically reduce this requirement.

Now, let's consider the well known series RC network transient; the energy dissipated by the resistor is exactly equal to the energy stored in the capacitor. The IR1168 internal gate driver is of course always in series with the external gate resistor, which means they will linearly share the power dissipation.

First, let's calculate the energy stored in the gate capacitance of one of the two synchronous MOSFETs:

$$E_{g1} = \frac{1}{2} C_{sync1} V_{g_{high}}^2$$

The total power dissipated by the driver buffer AND the total gate resistance (for both gate drivers) will therefore be

$$P_{dr} = P_{dr1} + P_{dr2} = 2 f_{SW\max} E_{g1} + 2 f_{SW\max} E_{g2}$$

The driver buffer and the gate resistance will linearly share this power dissipation as described in the following relationship:

$$P_{R_{g1}} = \left(\frac{R_{g1}}{R_{g1} + R_{Source}} + \frac{R_{g1}}{R_{g1} + R_{Sink}} \right) \cdot \frac{P_{dr1}}{2}$$

Rearranging this last relationship

$$\frac{P_{R_{g1}}}{P_{dr1}} = \frac{1}{2} \left(\frac{R_{g1}}{R_{g1} + R_{Source}} + \frac{R_{g1}}{R_{g1} + R_{Sink}} \right)$$

Solving this equation with respect to $R_{g1,\ 2}$ (which includes the external gate resistor and the MOSFET internal gate resistance), it is possible to determine the percentage of the total driving power dissipated into the gate resistor as a function of its value. Notice on IR1168 datasheet, pull up (r_{up}) and pull down (r_{down}) resistances are defined. Also, for the above calculations, we use $R_{Sink} = r_{down}$ and $R_{Source} = 1.1 r_{up}$ in order to account for some extra energy dissipated for voltage clamping.

The final step is the thermal verification for the chosen value. Using the maximum junction to ambient thermal resistance, the maximum temperature (where ambient refers to the environment in which the IC will work, i.e. box, PCB etc.) and the IC maximum junction temperature, it is now possible to calculate the maximum allowable IC power dissipation.

$$P_{IC_{\max}} = \frac{T_{J\max} - T_{IC\_amb}}{R_{\vartheta JA}}$$

where, $R_{\theta JA}$=128ºC/W (from IR1168 datasheet).

Because $P_{Rg1,\,2}$ is known and supply current has already been calculated, this will imply to limit the maximum V_{CC} supply voltage for the IC (therefore the maximum input power for IR1168)

$$V_{CC_{\max}} = \frac{P_{IC_{\max}} + P_{R_{g1}} + P_{R_{g2}}}{I_{CC}}$$

The following charts show the maximum allowable V_{CC} vs. maximum switching frequency for different load capacitances (assuming T_{jmax}=125°C and T_{IC_amb}=55°C and 1Ω MOSFET internal gate resistor).

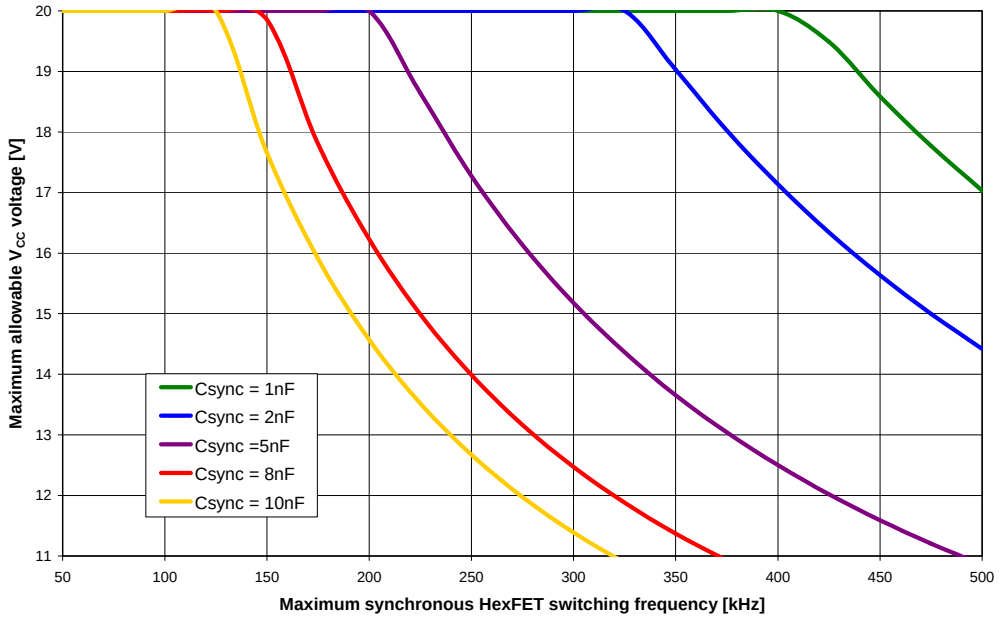


Figure 9: Max V_{CC} supply voltage vs. switching frequency with $R_{g1,\,2}$=3Ω

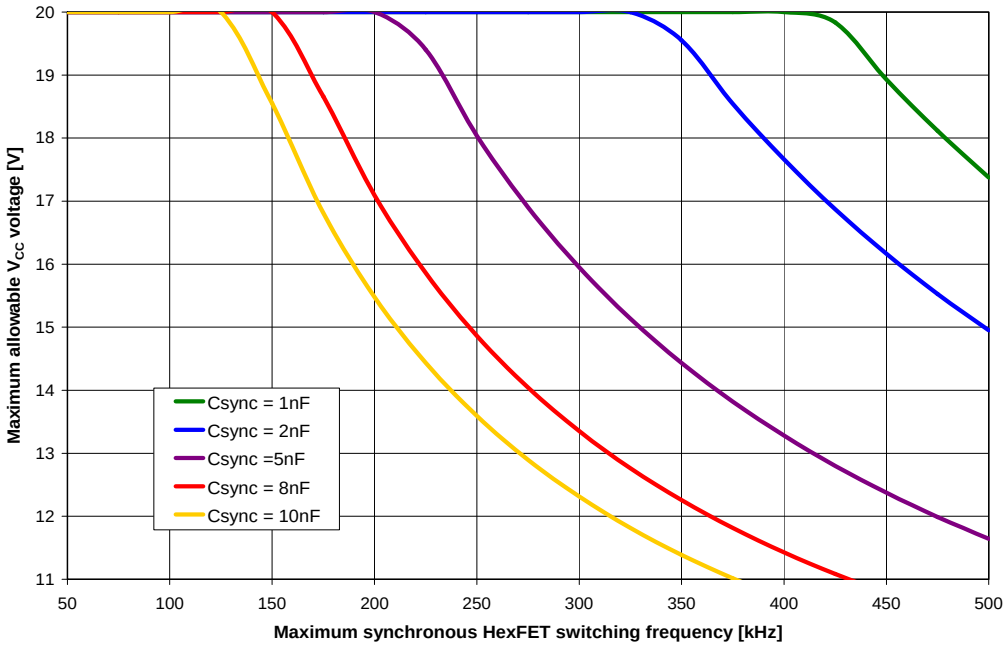


Figure 10: Max V_{CC} supply voltage vs. switching frequency with $R_{g1,\,2}$=4Ω

From the two above charts, it is clear how the supply voltage and gate resistor play a major role in the design trade off. In most commercial systems, the minimum gate resistor value for loop damping will satisfy the thermal requirements. If not, the procedure has to be iterated taking the following steps

Step 1: decrease the V_{CC} to the lowest possible value through a series resistor[2]:

$$R_{CC} = \frac{V_{supply} - V_{CC}}{I_{CC}}$$

If this allows V_{CC} to comply the thermal limit, then the gate resistor value can be kept as designed.

[2] It is worth mentioning the additional benefit of adding some series resistance to supply, which provides an enhanced filtering effect with the local decoupling capacitor. For systems powered from the output (no dedicated power through windings, etc.) this can result in smoother operations.

Step 2: Increase the gate resistor value. This can be of some effect if a small resistor value has been selected.

c. Decoupling capacitor

Several techniques are possible for decoupling capacitor sizing, depending on the converter topology and/or special requirements. The two most common cases relevant here are IR1168 powered directly from either the output or from a dedicated winding.

In the first case, in order to reduce the voltage ripple and possible noise, a good design practice is to use a series resistor on the supply (if not already used for thermal management reasons) and size the capacitor in order to obtain a low pass filter with a pole frequency a couple of octaves below the minimum operating switching frequency (this is not the stand-by operating frequency of the converter)

$$C_{dc\_\min} = \frac{2}{\pi \cdot f_{SW_{\min}} \cdot R_{CC}}$$

In case of operations through an auxiliary winding or winding tap, the decoupling capacitor should be sized in order to allow one switching period operation even in the absence of the main supply, with an acceptable voltage ripple ΔV_{CC}

$$C_{dc\_\min} = \frac{I_{CC}}{f_{SW_{\min}} \cdot \Delta V_{CC}}$$

Design example

System data:

- $f_{SW_{\max}} = 250kHz$
- $f_{SW_{\min}} = 50kHz$
- $T_{IC_{amb}} = 70^{o}C$
- Converter output voltage = 19V

Synchronous MOSFET: IRF7855PbF (60V/9.4mΩ max)

- $Q_g = 26nC \ @ \ V_{gs} = 10V$
- $Q_{gd} = 9.6nC \ @ \ V_{gs} = 10V$
- $C_{iss} = 1.56nF$

a. IC current consumption calculation

$$C_{sync} = \frac{Q_g - Q_{gd}}{V_{gs}} = 1.6nF$$

$$I_{CC} = I_{QCC} + 2 \times f_{SW_{\max}} C_{sync} V_{g_{high}} + 1.18 \cdot 10^{-8} f_{SW_{\max}} = 13.7mA$$

d. Supply series resistor and gate resistor design, and thermal verification
Assuming the total gate loop trace length is 15mm (0.6inch); $L_g \approx 15nH$

$$R_{g_{loop}} > 2\sqrt{\frac{L_g}{C_{iss}}} = 3.97\Omega$$

From IR1168 datasheet, driver pull down resistance r_{down} = 1.2Ω
Assume MOSFET internal gate resistance is 1Ω.
Hence, $R_g > 1.77\Omega$ Select $R_{g1,2} = 1.8\Omega$

Let's now verify the system thermally:

$$P_{dr1} = 2 f_{SW\max} E_g = 46.9mW$$

Therefore

$$P_{R_{g1}} = \left(\frac{R_{g1}}{R_{g1} + R_{Source}} + \frac{R_{g1}}{R_{g1} + R_{Sink}} \right) \cdot \frac{P_{dr1}}{2} = 19.9mW$$

Assuming an IC maximum junction temperature of 100ºC,

$$P_{IC_{\max}} = \frac{T_{J\max} - T_{IC\_amb}}{R_{\vartheta JA}} = 234mW$$

The maximum V_{CC} voltage can now be calculated as -

$$V_{CC_{\max}} = \frac{P_{IC_{\max}} + P_{R_g}}{I_{CC}} = 20V$$

The available supply voltage is below this value and hence, the IC supply can be directly generated from the converter output (series resistor recommended).

$$R_{CC} = 50\Omega$$

This resistor will dissipate a maximum of 9.4mW at $f_{SW_{\max}}$.

b. Decoupling capacitor

Since this system can be directly powered from the converter output, the filtering criterion is the preferred one for sizing the decoupling capacitor. Therefore,

$$C_{dc\_\min} = \frac{2}{\pi \cdot f_{SW_{\min}} \cdot R_{CC}} = 255nF$$

Select standard value $C_{dc} = 270nF$

Layout guidelines and examples

➢ *IC placement*

Due to the nature of the control, based on fast and accurate voltage sensing, it is highly recommended to layout the circuit in order to keep the IR1168 as close as possible to the two SR MOSFETs.

➢ *IC Decoupling Capacitor*

The key element to proper bypassing for the IC is the physical location of the bypass capacitor and its connections to the power terminals of the control IC. In order for the capacitor to provide adequate filtering, it must be located as close as physically possible to the V_{CC} and GND pins and connected through the shortest available path.

➢ *Differential Sensing for V_D/V_S*

IR1168 offers differential voltage sensing for both the synchronous MOSFETs. It is recommended to minimize the trace lengths and to keep them separated from the power ground as much as possible. For sensing optimization related to MOSFET package inductance, please refer to the appendix.

When a sensing resistor is used for current feedback in the rectifier power loop, it is highly recommended not to include it in the driving and sensing loops as shown in Figure 11 (this will cause some noise on the V_{CC} but will be filtered by the decoupling capacitor and R_{CC} series resistor).

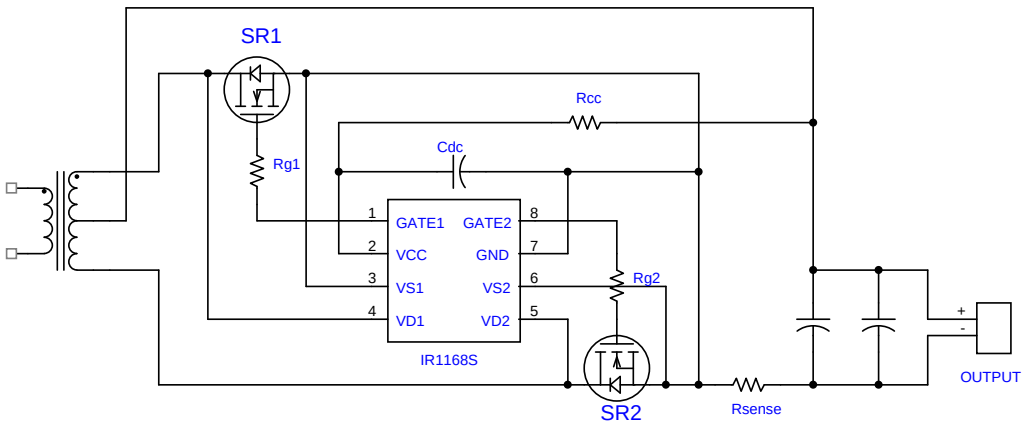


Figure 11: Output current sense resistor placement (if present)

➢ *Gate Drive Loop*

Minimizing the length of the gate drive loop will reduce the requirements for loop damping and would enhance system robustness. Once the layout is finalized, a "rule of thumb" estimation consists in measuring the physical loop trace length in assuming each millimeter (1mm = 39.37mils) accounts for 1nH. Other methods include measurement (low frequency RCL meters or current slope for a given voltage pulse) or FEM simulations.

➢ *Layout examples*

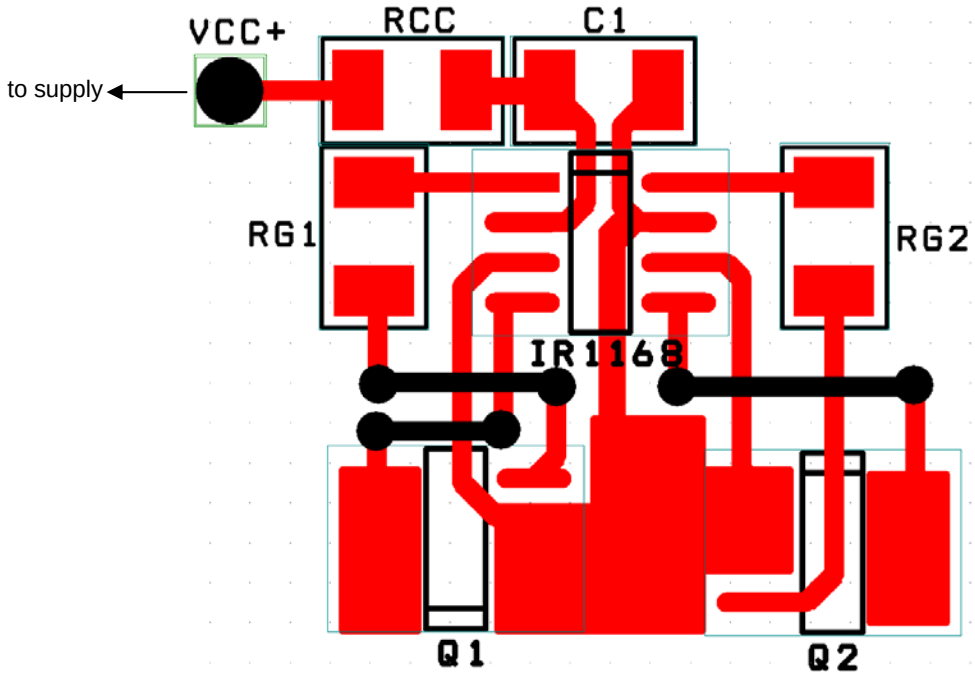


Figure 12: Single layer board, SO8 MOSFETs and surface-mount gate resistors

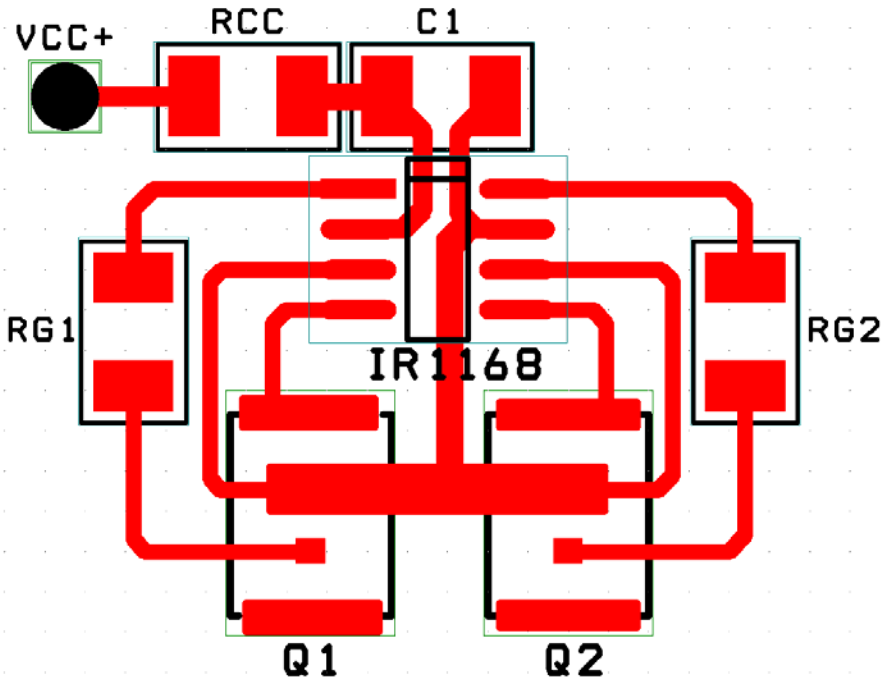


Figure 13: Single layer board, DFET MOSFETs and surface-mount gate resistors

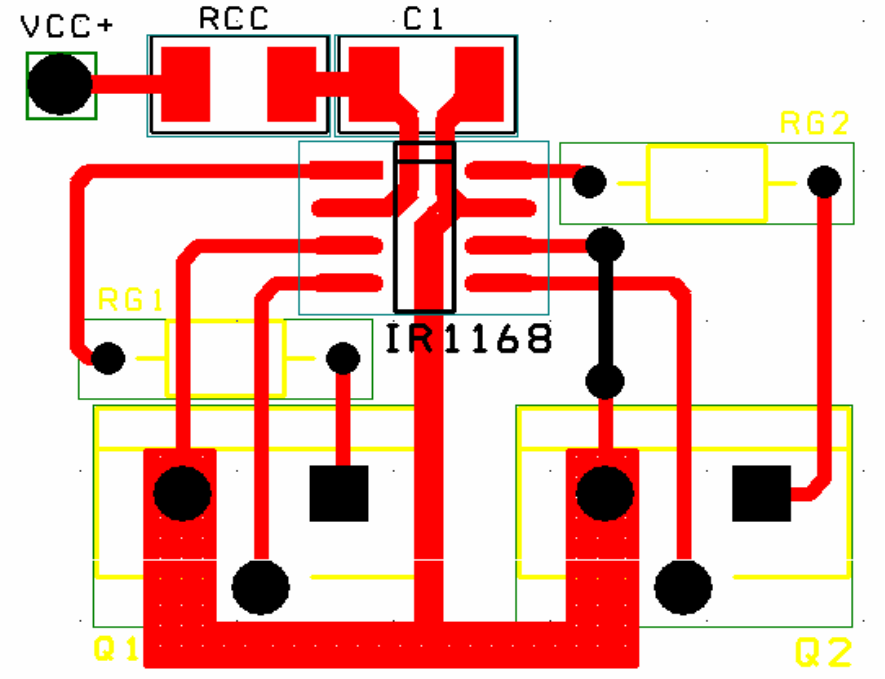


Figure 14: Single layer board, TO220 MOSFETs and through-hole gate resistors

Appendix

Symbols list

V_{TH1}: IR1168 turn-off threshold
V_{TH2}: IR1168 turn-on threshold
V_{TH3}: IR1168 periodic logic (reset) threshold
R_{AC}: Equivalent AC resistance for resonant tank AC analysis
R_{DSon}: synchronous rectifier MOSFET channel ON resistance
I_D: synchronous rectifier MOSFET drain current
V_{DS}: synchronous rectifier MOSFET drain to source voltage
MOT: IR1168 minimum ON time parameter
t_{blank}: IR1168 turn off blanking time
C_{dc}: IR1168 decoupling capacitor on Vcc
$R_{g1,\ 2}$: SR MOSFET gate drive loop resistance external to IR1168 IC
R_{CC}: supply voltage series resistor value (V_{supply} to V_{CC})
f_{SWmax}: converter maximum operating switching frequency
f_{SWmin}: converter minimum operating switching frequency
Q_g: SR MOSFET total gate charge
Q_{gd}: SR MOSFET gate to drain (Miller) charge
V_{gs}: SR MOSFET gate to source voltage
V_{ghigh}: IR1168 gate drive output voltage
I_{QCC}: IR1168 quiescent current
L_g: total gate loop parasitic inductance
C_{iss}: SR MOSFET input capacitance
$E_{g1,\ 2}$: Energy stored in the gate capacitance of each SR MOSFET
$P_{dr1,\ 2}$: Total power dissipated by the gate drive function for each SR MOSFET
R_{Source}: gate driver source resistance
R_{Sink}: gate driver sink resistance
$P_{Rg1,\ 2}$: Power dissipated in each gate resistor
P_{ICmax}: IR1168 IC maximum power dissipation
T_{IC_amb}: IC environment temperature (most cases is PCB temperature where IC is soldered)
$R_{\theta JA}$: IR1168 IC junction to ambient thermal resistance
V_{CC}: Supply voltage on IR1168 Vcc pin
I_{CC}: IR1168 IC supply current
V_{supply}: System available supply voltage for SR function
C_{dc_min}: minimum calculated decoupling capacitance
ΔV_{CC}: supply peak to peak ripple voltage on IR1168 V_{CC} pin

References

[1] IR1168 SmartRectifier™ control IC datasheet, International Rectifier, March 2008.

[2] "Design of Secondary Side Rectification using IR1167 SmartRectifier™ Control IC" International Rectifier Application Note AN1087, 2006.

[3] Adnaan Lokhandwala, Maurizio Salato & Marco Soldano "Dual SmartRectifier™ – DirectFET Chipset Solution Overcomes Package Induced Sensing Limitations Allowing High Performance Synchronous Output Rectification in LCD TV Power Supplies", Proceedings of PCIM China 2007.

[4] Adnaan Lokhandwala, Maurizio Salato & Marco Soldano "SmartRectifier™ control simplifies output synchronous rectification in DC-DC series resonant converters", Proceedings of PCIM Europe 2006.